Exercise 5-1: Consider the buffer shown below. Using the SCS MOSFET model to perform a large-signal analysis of their circuit according to the following steps.

(a) Assuming that the MOSFET operates in its saturation region, show that $v_{OUT}$ is related to $v_{IN}$ according to

$$v_{OUT} = \left[ \sqrt{\frac{2}{RK}} + 4(\frac{v_{IN} - v_T}{2} - \sqrt{\frac{2}{RK}}) \right]^2.$$ 

(b) Determine the range of $v_{IN}$ over which the assumption of saturated MOSFET operation holds.
Problem 5-1: Consider again the buffer described in Exercise 5-1. Perform a small-signal analysis of this circuit according to the following steps. Assume that the MOSFET operates in its saturation region. (Hint: See Example 33 on page 203 of the notes.)

(a) Draw the small-signal circuit model of the buffer.

(b) Show that the small-signal transconductance $g_m$ of the MOSFET is given by

$$g_m = K(V_{IN} - V_{OUT} - v_T)$$

where $V_{IN}$ and $V_{OUT}$ are the bias, or operating-point, input and output voltages respectively.

(c) Determine the small-signal gain of the buffer. That is, determine the ratio $v_{out}/v_{in}$.

(d) Determine the small-signal output resistance of the buffer. That is, determine the equivalent resistance of the buffer at the output port of its small-signal model with $v_{in} = 0$.

(e) Assume that $v_T = 1$ V, $K = 2$ mA/V$^2$, $R = 1$ k$\Omega$ and $V_S = 10$ V. Under this assumption, design the input bias voltage to satisfy the following two objectives. First, MOSFET operation must remain within the saturation region for $|v_{in}| \leq 0.25$ V. Second, the output resistance of the small-signal model must be minimized.

(f) Again assume that $v_T = 1$ V, $K = 2$ mA/V$^2$, $R = 1$ k$\Omega$ and $V_S = 10$ V. For $V_{IN} = 3$ V, compute the small-signal gain and output resistance.

Problem 5-2: This problem studies the relationship between the power consumed by a digital gate and the noise margin of that gate.

(a) Consider the two-input OR gate shown below. Using the switch-resistor MOSFET model also shown below, determine the maximum power dissipated by this gate and the logical inputs for which this dissipation occurs.

(b) Consider again the two-input OR gate shown above. For a given $R_D$, $V_{OL}$ can be lowered by decreasing $R_{ON}$. What is the relationship between $V_{OL}$ and $R_{ON}$? Determined the maximum power dissipated by the gate as a function of $V_{OL}$?
**Problem 5-3:** This problem studies the propagation delay of digital signals through the two circuits shown below. Circuit #1 involves two cascaded MOSFET inverters driven by the voltage $v_{IN}$. The output voltage of the first inverter is $v_{OUT}$. Circuit #2 is identical to Circuit #1 except that the first inverter in this circuit now drives two inverters at its output. In all parts of this problem, each MOSFET is characterized by the switch-resistor-capacitor model shown below.

(a) Within what voltage range must $v_T$ fall to guarantee that the first inverter in both Circuit #1 and Circuit #2 can both turn on and turn off the inverters which follow it? Assume that $v_T$ falls within this range.

(b) Now consider Circuit #1. Assume that $v_{IN}$ has been at 0 V for a very long time. Then, at $t = 0$, $v_{IN}$ increases past $v_T$. Determine $v_{OUT}$ for $t \geq 0$.

(c) At what time does $v_{OUT}$ pass by $v_T$? This delay approximates the fall time of the first inverter. (Fall time is actually defined as the time required for $v_{OUT}$ to reach $V_{OL}$ after $v_{IN}$ passes by $v_{IH}$, but that subtlety is ignored here.)

(d) Next, assume that $v_{IN}$ has been at $V_S$ for a very long time. Then, at $t = 0$, $v_{IN}$ decreases past $v_T$. Determine $v_{OUT}$ for $t \geq 0$.

(e) At what time does $v_{OUT}$ pass by $v_T$? This delay approximates the rise time of the first inverter. (Rise time is actually defined as the time required for $v_{OUT}$ to reach $V_{OH}$ after $v_{IN}$ passes by $v_{IL}$, but that subtlety is ignored here.)

(f) Now consider Circuit #2. Determine both the turn-on and turn-off delay of the first inverter in this circuit. Hint: adapt the analysis of Circuit #1 to the analysis of Circuit #2.

(g) Is the first inverter in Circuit #2 slower or faster than the first inverter in Circuit #1. Why?