Exercise 5-1: Consider the buffer shown below. Use the SCS MOSFET model to perform a large-signal analysis of this circuit according to the following steps.

(a) Assuming that the MOSFET operates in its saturation region, show that $v_{\text{OUT}}$ is related to $v_{\text{IN}}$ according to

$$v_{\text{OUT}} = \left[ \sqrt{2/RK} + 4(v_{\text{IN}} - v_T) - \sqrt{2/RK} \right]^2.$$

Answer:

By Ohm’s law,

$$v_{\text{OUT}} = i_D R$$

Substitute in the formula for the current source:

$$v_{\text{OUT}} = \frac{K}{2} (v_{\text{GS}} - v_T)^2 R$$

Substitute for $v_{\text{GS}} = v_{\text{IN}} - v_{\text{OUT}}$:

$$v_{\text{OUT}} = \frac{RK}{2} (v_{\text{IN}} - v_{\text{OUT}} - v_T)^2$$
Let \( v_o = v_{IN} - v_T \) and \( \alpha = \frac{2}{RK} \):

\[
\alpha \cdot v_{OUT} = v_o^2 - 2v_0v_{OUT} + v_{OUT}^2
\]

This can be solved using the quadratic formula to obtain:

\[
v_{OUT} = \frac{2v_o + \alpha \pm \sqrt{\alpha^2 + 4v_o\alpha}}{2} = v_{IN} - v_T + \frac{1}{RK} \pm \sqrt{\left(\frac{1}{RK}\right)^2 + (v_{IN} - v_T)\frac{2}{RK}}
\]

We will determine which root to use in part (b).

Check the formula given in the problem by expanding it algebraically:

\[
v_{OUT} = \frac{\sqrt{\alpha + 4v_o} - \sqrt{\alpha}}{2} = \frac{(\alpha + 2v_o) - 2\sqrt{\alpha^2 + 4v_o\alpha} + \alpha}{4} = \frac{2v_o + \alpha - \sqrt{\alpha^2 + 4v_o\alpha}}{2}
\]

(b) Determine the range of \( v_{IN} \) over which the assumption of saturated MOSFET operation holds.

**Answer:**

Two conditions must be met for the MOSFET to remain in saturation:

\[
v_{GS} \geq v_T \quad (1)
\]

\[
v_{DS} \geq v_{GS} - v_T \quad (2)
\]

In addition, we require that \( V_S \geq v_{OUT} \geq 0 \) and \( \frac{V_S}{R} \geq i_D \geq 0 \).

Condition (1) requires that \( v_{GS} = v_{IN} - v_{OUT} \geq v_T \). The minimum value of \( v_{OUT} \) is 0V \( (i_D = 0A) \). Then we require that \( v_{IN} \geq v_T \).

Note that condition (1) also requires that

\[
v_{IN} \geq v_{OUT} + v_T = v_{IN} + \frac{1}{RK} \pm \sqrt{v_{IN} - v_T + \left(\frac{1}{RK}\right)^2}
\]

\[
0 \geq \frac{1}{RK} \pm \sqrt{v_{IN} - v_T + \left(\frac{1}{RK}\right)^2}
\]

Thus we must take the negative root in the formula for \( v_{OUT} \):

\[
v_{OUT} = v_{IN} - v_T + \frac{1}{RK} - \sqrt{\left(\frac{1}{RK}\right)^2 + (v_{IN} - v_T)\frac{2}{RK}}
\]

Condition (2) requires that \( v_{DS} \geq v_{GS} - v_T \Rightarrow V_S - v_{OUT} \geq v_{IN} - v_{OUT} - v_T \). Then we require that \( V_S + v_T \geq v_{IN} \).

To be thorough, check that this value of \( v_{IN} \) will not cause \( v_{OUT} \) to exceed \( V_S \).

The maximum value of \( v_{OUT} \) is \( V_S \) \( (i_D = \frac{V_S}{R}) \).

\[
i_D = \frac{V_S}{R} = \frac{K}{2}(v_{GS} - v_T)^2
\]

\[
\Rightarrow v_{IN} = V_S + v_T + \sqrt{V_S^2 \frac{2}{RK}}
\]

Hence \( v_{OUT} \) will not exceed \( V_S \) while the MOSFET is in saturation.
Problem 5-1: Consider again the buffer described in Exercise 5-1. Perform a small-signal analysis of this circuit according to the following steps. Assume that the MOSFET operates in its saturation region and continue to use the SCS MOSFET model. (Hint: See Example 33 on page 203 of the notes.)

(a) Draw the small-signal circuit model of the buffer.

Answer:

\[ \begin{align*}
\text{Answer:} \\
\begin{array}{c}
\text{Draw the small-signal circuit model of the buffer.} \\
\text{Answer:}
\end{array}
\end{align*} \]

(b) Show that the small-signal transconductance \( g_m \) of the MOSFET is given by

\[ g_m = K(V_{IN} - V_{OUT} - v_T) \]

where \( V_{IN} \) and \( V_{OUT} \) are the bias, or operating-point, input and output voltages, respectively.

Answer:

Use the formula for the MOSFET large-signal current source (in saturation):

\[ i_D = \frac{K}{2} (v_{GS} - v_T)^2 \]

Expand this formula in a Taylor series for \( v_{GS} = V_{GS} + v_{gs} \) (Total Signal = LARGE-SIGNAL + small-signal),

\[ I_D + i_d = \left[ \frac{K}{2} (v_{GS} - v_T)^2 \right] + v_{gs} \left[ 2 \times \frac{K}{2} (v_{GS} - v_T) \right] + \frac{v_{gs}^2}{2} [K] + ... \]

where the bracketed terms are evaluated at the large-signal bias point \( v_{GS} = V_{GS} \).

Then \( I_D = \frac{K}{2} (V_{GS} - v_T)^2 \). Ignoring higher-order terms, \( i_d = g_m v_{gs} \) where

\[ g_m = K(V_{GS} - v_T) = K(V_{IN} - V_{OUT} - v_T) \] (4)

(c) Determine the small-signal gain of the buffer. That is, determine the ratio \( v_{out}/v_{in} \).

Answer:

Using small-signal equivalents, \( v_{out} = i_d R = g_m v_{gs} R = g_m (v_{in} - v_{out}) R \).

\[ \text{gain} = \frac{v_{out}}{v_{in}} = \frac{g_m R}{1 + g_m R} \] (5)

(d) Determine the small-signal output resistance of the buffer. That is, determine the equivalent resistance of the buffer at the output port of its small-signal model with \( v_{in} = 0 \).
Answer:

Connect $v_{in}$ to ground. Apply $v_{test}$ at the output and measure $i_{test}$. Note that $v_{test}$ and $i_{test}$ appear to be anti-associated variables, but they will be associated variables for the equivalent resistance we are measuring.

Using KCL,

$$i_d + i_{test} = \frac{v_{test}}{R}$$

Note that $i_d = g_m v_{gs} = g_m(-v_{in})$ when $v_{in}$ is grounded.

$$-g_m v_{test} + i_{test} = \frac{v_{test}}{R}$$

$$R_{out} = \frac{v_{test}}{i_{test}} = \frac{R}{1 + g_m R} \quad (6)$$

(e) Assume that $v_T = 1 \text{ V}, K = 2 \text{ mA/V}^2, R = 1 \text{ k}\Omega \text{ and } V_S = 10 \text{ V}$ Under this assumption, design the input bias voltage to satisfy the following two objectives. First, MOSFET operation must remain within the saturation region for $|v_{in}| \leq 0.25 \text{ V}$. Second, the output resistance of the small-signal model must be minimized.

Answer:

To minimize the output resistance for a fixed value of $R$, we need to maximize $g_m$.

$$g_m = K(V_{IN} - V_{OUT} - v_T)$$

Substitute in the formula for $V_{OUT}$:

$$g_m = K \left[ V_{IN} - \left( V_{IN} - v_T + \frac{1}{R}K \right)^\frac{1}{2} \sqrt{\left( \frac{2}{R}K \right)^2 + 4(V_{IN} - v_T)\frac{2}{R}K} \right] - v_T$$

$$g_m = K \left( \sqrt{\frac{1}{R}K} + (V_{IN} - v_T)\frac{2}{R}K - \frac{1}{R}K \right)$$

To maximize $g_m$, maximize $V_{IN}$.

Choose $V_{IN} = V_{IN\text{ max}} - v_{in\text{ max}} = V_S + v_T - v_{in\text{ max}} = 10\text{ V} + 1\text{ V} - 0.25\text{ V} = 10.75\text{ V}$

(f) Again assume that $v_T = 1 \text{ V}, K = 2 \text{ mA/V}^2, R = 1 \text{ k}\Omega \text{ and } V_S = 10 \text{ V}$. For $V_{IN} = 3 \text{ V}$, compute the small-signal gain and output resistance.

Answer:

Find $V_{OUT}$ using equation (3) (derived in Exercise 5-1).

$$V_{OUT} = 1\text{ V}$$
Find $g_m$ using equation (4).

$$g_m = \frac{2\text{mA}}{V}$$

Plug-and-chug using equations (5) and (6):

$$\text{gain} = \frac{2}{3}$$

$$R_{out} = 333.3\Omega$$
Problem 5-2: This problem studies the relationship between the power consumed by a digital gate and the noise margin of that gate.

![Diagram of a digital gate](image)

(a) Consider the two-input OR gate shown above. Using the switch-resistor MOSFET model also shown above, determine the maximum power dissipated by this gate and the logical inputs for which this dissipation occurs.

**Answer:**

One easy way to calculate the power dissipation is to calculate the equivalent resistance between $V_S$ and ground. Then we can use the formula:

$$P_{\text{power}} = \frac{V_S^2}{R_{\text{eq}}}$$

To find the maximum power dissipation, minimize $R_{\text{eq}}$.

For $\text{IN1} = \text{IN2} = \text{high}$, $\text{MID} = \text{low}$.

$\Rightarrow R_{\text{eq}} = R_D + R_{\text{ON}} \parallel R_{\text{ON}}$

For one input high and one input low, $\text{MID} = \text{low}$.

$\Rightarrow R_{\text{eq}} = R_D + R_{\text{ON}}$

For $\text{IN1}=\text{IN2}=\text{low}$, $\text{MID}=\text{high}$.

$\Rightarrow R_{\text{eq}} = R_D + R_{\text{ON}}$

Then the maximum power is dissipated when the inputs are both high.

$$P_{\text{max}} = \frac{V_S^2}{R_D + \frac{1}{2}R_{\text{ON}}}$$

(b) Consider again the two-input OR gate shown above. For a given $R_D$, $V_{\text{OL}}$ can be lowered by decreasing $R_{\text{ON}}$. What is the relationship between $V_{\text{OL}}$ and $R_{\text{ON}}$? Determine the maximum power dissipated by the gate as a function of $V_{\text{OL}}$?

**Answer:**

$V_{\text{OL}} = V_S \frac{R_{\text{ON}}}{R_D + R_{\text{ON}}} \quad \text{(using a voltage divider)}.$

With a little algebra, we obtain:

$$R_{\text{ON}} = R_D \frac{V_{\text{OL}}}{V_S - V_{\text{OL}}}$$

Using this value of $R_{\text{ON}}$, we obtain the formula:

$$P_{\text{max}} = \frac{V_S^2}{R_D + \frac{1}{2}R_D \frac{V_{\text{OL}}}{V_S - V_{\text{OL}}}} = \frac{V_S^2}{R_D} \left( \frac{2V_S - 2V_{\text{OL}}}{2V_S - V_{\text{OL}}} \right)$$
**Problem 5-3:** This problem studies the propagation delay of digital signals through the two circuits shown below. Circuit #1 involves two cascaded MOSFET inverters driven by the voltage $v_{IN}$. The output voltage of the first inverter is $v_{OUT}$. Circuit #2 is identical to Circuit #1 except that the first inverter in this circuit now drives two inverters at its output. In all parts of this problem, each MOSFET is characterized by the switch-resistor-capacitor model shown below.

(a) Within what voltage range must $v_T$ fall to guarantee that the first inverter in both Circuit #1 and Circuit #2 can both turn on and turn off the inverters which follow it? Assume that $v_T$ falls within this range.

**Answer:**
For $v_{IN} < v_T$, $v_{OUT} = 5V$. For $v_{IN} \geq v_T$, $v_{OUT} = V_S \frac{R_{ON}}{R_{ON} + R_D}$.

\[ \Rightarrow V_S \frac{R_{ON}}{R_{ON} + R_D} < v_T < 5V \]

(b) Now consider Circuit #1. Assume that $v_{IN}$ has been at 0 V for a very long time. Then, at $t = 0$, $v_{IN}$ increases past $v_T$. Determine $v_{OUT}$ for $t \geq 0$.

**Answer:**
We can find the initial and steady-state values of $v_{OUT}$ by assuming that the capacitances are acting as open-circuits. Immediately before $v_{IN}$ reaches $v_T$, $v_{OUT} = V_S = v_{high}$.
A sufficient time after $v_{IN}$ reaches $v_T$, $v_{OUT} = V_S \frac{R_{ON}}{R_{ON} + R_D} = v_{low}$.

To determine the time-varying behavior of the circuit, examine how the capacitances will be charged. The capacitor $C_{GS}$ in the second inverter must be charged through the resistors $R_D$ and $R_{ON}$ of the first inverter. This capacitor sees a Thevenin equivalent
resistance of $R_{ON} \parallel R_D$.

This immediately allows us to write down the formula for $v_{OUT}$:

$$v_{OUT}(t \geq 0) = v_{low} + (v_{high} - v_{low}) e^{-\frac{t}{\tau_{fall-1}}}$$

$$\tau_{fall-1} = (R_{ON} \parallel R_D) C_{GS}$$

(c) At what time does $v_{OUT}$ pass by $v_T$? This delay approximates the fall time of the first inverter. (Fall time is actually defined as the time required for $v_{OUT}$ to reach $V_{OL}$ after $v_{IN}$ passes by $v_{IH}$, but that subtlety is ignored here.)

**Answer:**

Substituting in $v_T$ for $v_{OUT}$ in the formula just derived:

$$v_T = v_{low} + (v_{high} - v_{low}) e^{-\frac{t}{\tau_{fall-1}}}$$

$$\ln \left( \frac{v_T - v_{low}}{v_{high} - v_{low}} \right) = -\frac{t}{\tau_{fall-1}}$$

$$t(fall\text{-}time) = \tau_{fall-1} \ln \left( \frac{v_{high} - v_{low}}{v_T - v_{low}} \right)$$

(d) Next, assume that $v_{IN}$ has been at $V_S$ for a very long time. Then, at $t = 0$, $v_{IN}$ decreases past $v_T$. Determine $v_{OUT}$ for $t \geq 0$.

**Answer:**

Note that the techniques used in part (b) will work here too. $v_{OUT}$ goes from $v_{low}$ to $v_{high}$. The first inverter is in the OFF state when the capacitor is charging, so the capacitor sees a Thevenin equivalent resistance of $R_D$.

$$v_{OUT}(t \geq 0) = v_{high} + (v_{low} - v_{high}) e^{-\frac{t}{\tau_{rise-1}}}$$

$$\tau_{rise-1} = R_D C_{GS}$$

(e) At what time does $v_{OUT}$ pass by $v_T$? This delay approximates the rise time of the first inverter. (Rise time is actually defined as the time required for $v_{OUT}$ to reach $V_{OH}$ after $v_{IN}$ passes by $v_{IL}$, but that subtlety is ignored here.)

**Answer:**

Substituting in $v_T$ for $v_{OUT}$ in the formula just derived:

$$v_T = v_{high} + (v_{low} - v_{high}) e^{-\frac{t}{\tau_{rise-1}}}$$
\[
\ln \left( \frac{v_T - v_{\text{high}}}{v_{\text{low}} - v_{\text{high}}} \right) = -\frac{t}{\tau_{\text{rise} - 1}}
\]

\[
t(\text{rise - time}) = \tau_{\text{rise} - 1} \ln \left( \frac{v_{\text{high}} - v_{\text{low}}}{v_{\text{high}} - v_T} \right)
\]

(f) Now consider Circuit #2. Determine both the rise time and fall time of the first inverter in this circuit. Hint: adapt the analysis of Circuit #1 to the analysis of Circuit #2.

**Answer:**
Note that the capacitors in the second and third inverters must charge through \( R_D \) and \( R_{\text{ON}} \) of the first inverter (recall the situation described in part (b)). Therefore, the Thevenin equivalent resistances used in parts (b) through (e) remain the same.
The capacitors in the second and third inverters are in parallel, so \( v_{\text{OUT}} \) will depend on \( C_{\text{eff}} = 2C_{GS} \) instead of \( C_{\text{eff}} = C_{GS} \).
This allows us to write down the required answers by inspection.

\[
\tau_{\text{fall} - 2} = (R_{\text{ON}} \parallel R_D)(2C_{GS})
\]

\[
\tau_{\text{rise} - 2} = R_D(2C_{GS})
\]

\[
t(\text{fall - time}) = \tau_{\text{fall} - 2} \ln \left( \frac{v_{\text{high}} - v_{\text{low}}}{v_T - v_{\text{low}}} \right)
\]

\[
t(\text{rise - time}) = \tau_{\text{rise} - 2} \ln \left( \frac{v_{\text{high}} - v_{\text{low}}}{v_{\text{high}} - v_T} \right)
\]

(g) Is the first inverter in Circuit #2 slower or faster than the first inverter in Circuit #1. Why?

**Answer:**
Written in this way, it is obvious that Circuit #2 is 2x slower than Circuit #1. The first inverter in Circuit #2 must charge 2x the capacitance whenever \( v_{\text{OUT}} \) changes.