An answer sheet is attached to the back of this exam. Please put your name on your answer sheet and on your exam book. Also, please circle the name of your recitation instructor and the time of your recitation on your answer sheet.

Do all of your work in your exam book, and then record your answers on your answer sheet. Hand in both your exam book and your answer sheet at the end of the exam period. You may keep the exam questions.

You are welcome to use one double-sided page of notes while taking this exam.

Good luck!
Problem 1  –  25 Points

This problem is concerned with Network A shown below, which has a single port. In Parts (A) and (B) of this problem, Network A stands alone. In Part (C), Network A is connected to Network B which has a nonlinear terminal relation that is described graphically.

(A) Consider Network A alone so that \( i_A = 0 \). Find the node voltages \( e_1 \) and \( e_2 \) with respect to ground.

(B) Find the Norton equivalent current \( I_N \) and resistance \( R_N \) of Network A when viewed from its port.

(C) Network A is connected to Network B which has the nonlinear terminal relation that is described graphically below. Given this connection, determine \( i_B \) under the assumption that \( V \) and \( I \) are both positive. Express \( i_B \) in terms of \( \alpha \), \( I_N \) and \( R_N \).
Problem 2  –  40 Points

This problem examines digital logic circuits in which logic values are represented by positive currents. Specifically, the logic value 0 is represented by a low-valued current, and the logic value 1 is represented by a high-valued current. The logic circuits are implemented with the current-controlled switch defined below. The switch opens when its labeled control current equals or exceeds the threshold current \( i_T \), and closes otherwise. The control current can be any current in the logic circuit. Note that the switch is imperfect, and has a nonzero off-state conductance, \( G_{off} \). Also, assume that \( i_T \) satisfies \( 0 < i_T < I_S \), where \( I_S \) is the supply current.

(A) Consider Circuit #1 which is formed with a current-controlled switch, a current supply, and a bypass conductor having conductance \( G_{BP} \). Sketch and clearly label a graph of \( i_{OUT} \) as a function of \( i_{IN} \) for \( 0 \leq i_{IN} \leq I_S \).

(B) Circuit #1 is to satisfy a static discipline defined by \( I_L \) and \( I_H \), where \( 0 < I_L < I_H < I_S \). That is, for both \( i_{IN} \) and \( i_{OUT} \), a valid logic 0 lies between 0 and \( I_L \), and a valid logic 1 lies between \( I_H \) and \( I_S \). In this case, within what current range must \( i_T \) lie, and what is the maximum acceptable value for \( G_{off} \)?

(C) Consider Circuit #2 with \( G_{off} = 0 \). Assume that \( i_{IN1}, i_{IN2} \) and \( i_{IN3} \) each equals 0 when representing the logic value 0, and \( I_S \) when representing the logic value 1. Derive a truth table for the input-output behavior of the circuit.

(D) Consider Circuit #2 again but with \( G_{off} > 0 \). Assume that all controlled switches open or close for all sets of input currents as found in Part (C). Determine the combination of inputs IN1, IN2 and IN3 that results in maximum power dissipation in the circuit.

(E) Consider Circuit #2 again with \( G_{off} > 0 \). What relation between \( G_{off}, G_{BP}, i_T \) and \( I_S \) is necessary and sufficient for all controlled switches to open or close for all sets of input currents as found in Part (C).
Current-Controlled Switch

Symbol: $i_C$

Model: $G_{OFF}$

Switch closed for $i_C < i_T$
Switch open for $i_C \geq i_T$

Circuit #1

$\text{IN} \rightarrow i \rightarrow \text{OUT}$

$i \rightarrow G_{BP} \rightarrow I_S$

Circuit #2

$\text{IN}_1 \rightarrow i_1 \rightarrow i_2 \rightarrow i_3 \rightarrow i_4 \rightarrow \text{OUT}$

$G_{BP} \rightarrow I_S$

$i_2 \rightarrow G_{BP} \rightarrow i_4$
Problem 3  –  35 Points

This problem studies the MOSFET amplifier shown below. For simplicity, assume that the threshold voltage of the MOSFET is zero. Therefore, the MOSFET behaves according to $i_D = \frac{K}{2} v_{GS}^2$ when operating in its saturation region, which is defined by $v_{DS} \geq v_{GS} \geq 0$.

(A) Assume that the MOSFET operates in its saturation region. Determine $v_{GS}$ as a function of $K$, $R$, $v_{IN}$ and $V_S$.

(B) Assume that the MOSFET operates in its saturation region. Determine $v_{OUT}$ as a function of $K$, $R$, $v_{IN}$ and $V_S$.

(C) Over what range of $v_{IN}$ will the MOSFET operate in its saturation region?

(D) Let $v_{IN} = V_{IN} + v_{in}$ where $V_{IN}$ and $v_{in}$ are the large-signal and small-signal components of $v_{IN}$, respectively. Similarly, let $v_{OUT} = V_{OUT} + v_{out}$ where $V_{OUT}$ and $v_{out}$ are the large-signal and small-signal components of $v_{OUT}$, respectively. Assume that the MOSFET operates in its saturation region and determine the small-signal gain of the amplifier, $v_{out}/v_{in}$, in terms of $K$, $R$, $V_{IN}$ and $V_S$.
Problem 1

(A) \( e_1 = \) \( e_2 = \)

(B) \( I_N = \) \( R_N = \)

(C) \( i_B = \)

Problem 2

(A)
(B) Ranges:

\[ < i_T < \quad G_{OFF} < \]

(C) Truth Table:

<table>
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<th>IN1</th>
<th>IN2</th>
<th>IN3</th>
<th>OUT</th>
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(D) \( \text{IN1} = \quad \text{IN2} = \quad \text{IN3} = \)

(E) Relation:

Problem 3

(A) \( v_{GS} = \)

(B) \( v_{OUT} = \)

(C) Range: \( \leq v_{IN} \leq \)

(D) \( \frac{v_{out}}{v_{in}} = \)