ERROR IN NOTES FOR LECTURE 1: MIDDLE LEFT $P_2$, $I_g$ THE GATE CURRENT IS MISLABELED AS $I_c$ BOTH IN THE SKETCH AND THE EQUATION BELOW WHICH SHOULD READ $I_g \neq 0$.

THE MOSFET IS THE ACTIVE ELEMENT (THE "VALUE") IN DIGITAL COMPUTER GATES:

![NAND Gate Diagram]

NAND GATE

![NOR Gate Diagram]

NOR GATE

WHAT ARE THE PRACTICAL CONSIDERATIONS IN CIRCUIT DESIGN AND OPERATION?

The voltage representing a boolean variable cannot be precisely 0 for the zero or "off" state nor precisely V (the supply voltage) for the "one" or on state. Some variation must be permitted.

Consider this possibility:

(V represents the input voltage of a gate)

<table>
<thead>
<tr>
<th>$V$</th>
<th>$V_{IH}$ (on or high)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OL}$ (off or low)</td>
<td></td>
</tr>
</tbody>
</table>

What if $V = V_{OL}$ what should be the response of the gate?

A better possibility:

![Threshold Voltage Diagram]

Clearly the threshold voltage of the FETs must fall in the forbidden region
The circuits or systems are designed so that the voltage representing a variable can never be in the forbidden region. If for some reason it is. So what? A failed design. Pink slip time!

Cascaded Gates.

\[ V_{\text{N}} \] represents noise

Unless \( V_{\text{N}} = 0 \), a signal could easily fall in the forbidden region. E.g., \( V_{\text{L}} + |V_{\text{N}}| \) or \( V_{\text{H}} - |V_{\text{N}}| \) would do.

Some margin for noise is acquired

\[ V_{\text{H}} \] is the lowest value of an input which will be read as a one.
\[ V_{\text{L}} \] is the highest value of an input which will be read as a zero.

\[ V_{\text{OH}} \] is the lowest value of an output which represents a one.
\[ V_{\text{OL}} \] is the highest value of an output which represents a zero.

The standard notation above is puzzling at first, but comes easiest when you recognize that a subscript \( O \) refers to an output - a sent signal while the subscript \( I \) refers to an input - a received signal.

Note that \( V_{\text{L}} - V_{\text{OL}} \) defines the maximum tolerable noise for a zero.

\[ V_{\text{L}} - V_{\text{OL}} \] is the zero noise margin

Similarly, \( V_{\text{OH}} - V_{\text{IH}} \) is the one noise margin

Note also that the permissible output signal ranges \( (V_{\text{H}} - V_{\text{OH}}) \) and \( (V_{\text{L}} - V_{\text{OL}}) \) are more tightly constrained than the range of noise-contaminated inputs which must be correctly read: \( (V_{\text{L}} - V_{\text{IH}}) \) and \( (V_{\text{H}} - V_{\text{OH}}) \).

The four critical levels \( V_{\text{OL}}, V_{\text{IL}}, V_{\text{IH}}, V_{\text{OH}} \) comprise the static discipline.
Thus a properly designed gate restores signal integrity.

Consider a numerical example:

- $V_{IN}$ (Volts)
- $V_{OL}$ (0.8 Volt)
- $V_{OH}$ (1 Volt)
- $V_{Z}$ (1.2 Volt)
- Noise margin:
  - One noise margin (1 Volt)
  - Forbidden region (1.2 Volts)

If the peak amplitude of the noise is less than 0.8 Volts, the buffer will operate properly in both states. If in the range 0.8 - 1.0 Volts the one state will operate properly, but the zero state might not.

Demo:

Noise source -> Variable gain ampl. -> Output

Noise source

$V_A$ vs $t$

$V_B$ vs $t$

Output vs $t$