Exercise 6.1: Consider the network shown below, which was studied earlier in Problem 2.4. Let \( v_{\text{IN}} = V_{\text{IN}} + v_{\text{in}} \), and \( v_{\text{D}} = V_{\text{D}} + v_{\text{d}} \), where \( V_{\text{IN}} \) and \( V_{\text{D}} \) are the large-signal components of \( v_{\text{IN}} \) and \( v_{\text{D}} \), respectively, and \( v_{\text{in}} \) and \( v_{\text{d}} \) are the small-signal components of \( v_{\text{IN}} \) and \( v_{\text{D}} \), respectively. Also, let \( i_{\text{D}} = I_{\text{D}} + i_{\text{d}} \), where \( I_{\text{D}} \) and \( i_{\text{d}} \) are the large-signal and small-signal components of \( i_{\text{D}} \), respectively. Assuming that \( V_{\text{IN}} \) is large enough so that \( V_{\text{D}} \gg V_{T} \), where \( V_{T} \) is the thermal voltage of the diode, show that \( v_{\text{d}} \approx v_{\text{in}} / (1 + RI_{\text{D}} / V_{T}) \). Hint: use a small-signal model.

Exercise 6.2: Find the inductance of the all-inductor network, and the capacitance of the all-capacitor network, shown below.
Problem 6.1: This problem studies the propagation delay of digital signals through the inverter shown below. Assume that the MOSFET in the inverter acts as a switch with on-state resistance $R_{ON}$. The inverter is loaded by a capacitor, having capacitance $C_G$, that models the combined input capacitance of the logic gates connected to its output. Assume that the inverter obeys the static discipline defined in part by $V_{OL}$ and $V_{OH}$.

(A) Assume that the MOSFET has been off for a very long time. At $t = 0$, $v_{IN}$ turns the MOSFET on. Determine $v_G(t)$ for $t \geq 0$.

(B) How long does it take $v_G(t)$ to pass by $V_{OL}$? This delay is the fall time of the inverter.

(C) Assume that the MOSFET has been on for a very long time. At $t = 0$, $v_{IN}$ turns the MOSFET off. Determine $v_G(t)$ for $t \geq 0$.

(D) How long does it take $v_G(t)$ to pass by $V_{OH}$? This delay is the rise time of the inverter.

(E) If more gates are connected to the output of the inverter will the delays found in Parts (B) and (D) become shorter or longer? Why?

(F) How can the fall and rise times be shortened via the design of $R_{PU}$? What limits the extent to which this design path may be followed?
Problem 6.2: In the circuit shown below, a Thevenin equivalent input, modeled by \( v_{IN} \) and \( R_{IN} \), is connected to a load, modeled by \( R_{LOAD} \), through a non-ideal 1:N step-up transformer. The non-ideal transformer comprises an ideal 1:N step-up transformer, modeled by two dependent sources, and an inductor. The inductor models magnetizing inductance. Such effects as winding resistance and leakage inductance, core loss, and inter-winding capacitance are ignored. To learn more about ideal transformers, see Section 9.3.4 in A&L. To learn more about non-ideal transformers, see Section 13:764d-e in A&L; this section is on the web.

(A) Focus on the right-hand side of the circuit, and determine \( i_2(t) \) in terms of \( v_1(t) \).

(B) Using the constitutive law for the inductor determine an integral expression that relates \( i_L(t) \) to \( v_1(t) \).

(C) Using the node method, determine an expression that relates \( v_1(t) \) to \( v_{IN}(t) \). In doing so, back substitute your results from Parts (A) and (B).

(D) Differentiate the expression found in Part (C) with respect to time to obtain a differential equation that can be solved for \( v_1(t) \), given \( v_{IN}(t) \) and an initial condition for \( v_1(t) \).

(E) Assume that \( i_L(t) = 0 \), and hence \( v_1(t) = 0 \) for \( t < 0 \). Further assume that \( v_{IN}(t) \) steps from 0 V to \( V_o \) at \( t = 0 \). Given these assumptions, determine \( v_1(t) \) and \( i_L(t) \) for \( t \geq 0 \).

(F) Determine \( v_{LOAD}(t) \) for \( t \geq 0 \).

(G) Why does \( v_{LOAD}(t) \) eventually go to zero?
Problem 6.3: At \( t = 0^- \), the networks shown below have zero initial state. That is, the capacitor voltage \( v(t) \) and the inductor current \( i(t) \) are both zero at \( t = 0^- \). At \( t = 0 \), the current source produces an impulse of area \( Q \), and the voltage source produces an impulse of area \( \Lambda \).

(A) Derive the differential equation that relates \( v(t) \) to \( I(t) \) and \( i(t) \) to \( V(t) \). Hint: consider using Thevenin and/or Norton equivalents to simplify the work.

(B) Find the capacitor voltage \( v(t) \) and the inductor current \( i(t) \) at both \( t = 0^+ \) and \( t = \infty \). One way to find the states at \( t = 0^+ \) is to integrate the corresponding differential equations from \( t = 0^- \) to \( t = 0^+ \) under the assumption that each state remains finite during that time; you should justify this assumption. Then, substitute the initial conditions at \( t = 0^- \) into the results to determine the states at \( t = 0^+ \). Try to determine the states at \( t = \infty \) through physical, rather than mathematical, reasoning.

(C) Next, find the time constant by which each state goes from its initial value at \( t = 0^+ \) to its final value at \( t = \infty \).

(D) Using the previous results, and without necessarily solving the differential equations directly, construct \( v(t) \) and \( i(t) \) for \( t \geq 0 \).

(E) Verify that the solutions to Part (D) are correct by substituting them into the differential equations found in Part (A).

\[
I(t) = Q\delta(t) \\
R_1 \\
\hspace{1cm} \text{+} \\
\hspace{1cm} v(t) \\
\hspace{1cm} - \\
\hspace{1cm} V(t) = \Lambda\delta(t) \\
R_2 \\
\hspace{1cm} \text{+} \\
\hspace{1cm} i(t) \\
R_2 \\
\text{+} \\
L
\]