Wireless Headphones

6.111 Final Project

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Analog to Digital...

...Digital to Analog
Specifications and Requirements

• No aliasing: at least 44-kHz sampling rate
• High resolution: at least 8 bit bits per sample
• Stereo: two samples per sampling period
• Wireless transmission rates: not too many bits per sample
Analog to Digital Conversion

A/D modules
1 word = 16x2 bits
1 chunk = 5 words

AD7656
Analog to Digital Converter

CONVST
BUSY
CS
DOUT
SCLK

I/O FSM and Stack

Sample FSM

Clock Divider

27-MHz

27-MHz

9-kHz

45-kHz

Sample
word

32
Digital to Analog Conversion

chunk-tick

Data Stack Controller

AD5063 Digital to Analog Converter
to op-amp

data-out

SCLK

D/A Modules

data-in

27-Mhz

45-kHz

45-kHz

27-Mhz

SCLK

45-kHz
COMPRESSSION
DECOMPRESSSION

Jessica N.
Codec – Big Picture

80 bits

<table>
<thead>
<tr>
<th>N5</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>N4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>N3</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>N2</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>N1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>diff5</th>
<th>s</th>
<th>diff4</th>
<th>s</th>
<th>diff3</th>
<th>s</th>
<th>diff2</th>
<th>s</th>
<th>first1</th>
<th>N1</th>
</tr>
</thead>
<tbody>
<tr>
<td>39</td>
<td>36</td>
<td>35</td>
<td>34</td>
<td>31</td>
<td>30</td>
<td>29</td>
<td>26</td>
<td>25</td>
<td>24</td>
</tr>
<tr>
<td>21</td>
<td>20</td>
<td>19</td>
<td>16</td>
<td>15</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
</tbody>
</table>

40 bits
Lossy vs. Lossless
Decompression

**state_shiftl**
- N1_in <= N1_in << (15 – first1)
- state <= state_N2

**state_set1**
- N1_in[15] <= 1
- state <= state_shiftr

**state_shiftr**
- N1_in <= N1_in >> (15 – first1)
- state <= state_set1

**state_N3**
- if (N3_sign == 0)
  - N3 <= N2 + N3_diff
  - else
  - N3 <= N2 – N3_diff
- state <= state_N4

**state_N4**
- if (N4_sign == 0)
  - N4 <= N3 + N4_diff
  - else
  - N4 <= N3 – N4_diff
- state <= state_N4

**state_N5**
- if (N5_sign == 0)
  - N5 <= N4 + N5_diff
  - else
  - N5 <= N4 – N5_diff
- state <= state_N4

**state_done**
- valid_out <= 1
Wireless

Nivedita C.
Wireless – Operation, Specifications and Requirements

- Hardware: Two CC2420 transceivers mounted on two evaluation boards
- All communication with chips implemented in Verilog
- Talk to chips via a Serial Peripheral (SPI) interface clocked at 10MHz
- All operations performed by writing or reading from 33 16-bit configuration registers and 15 8-bit command strobe registers
General Transceiver Block Diagram

FIFO Buffer

SPI Master

Configuration Mode

Transmit Mode

Receive Mode

begin_config

done_config

Config_ROM
8x24

config_data
24

begin_trans

done_trans

(125*4)

trans_packet

begin_rec

done_rec

rec_packet

(125*4)

success

Config_ROM
8x24

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Config_ROM
8x24

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(125*4)

trans_packet

begin_rec

done_rec

rec_packet

(125*4)

success

Config_ROM
8x24
Implementation Issues

- Data Throughput
  - Chipcon specs: max data rate ~250 kbps
  - Overhead: includes frame check sequences, may have to introduce error correction sequences
  - Assumes uninterrupted transmission
- Memory buffer sizes
  - The lower the data rate, the greater the required size of the buffers
- Dealing with two labkit clocks
  - Need to time interaction of two halves of the system properly
- Solution: Handshake/acknowledgement protocol between transmitter and receiver