A CMOS Bandgap Reference for Differential Signal Processing

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Abstract—**A switched-capacitor fully differential bandgap reference is presented that employs a standard double-poly CMOS process. It generates a differential reference voltage of 6.2 V with a standard deviation of about 24 mV and a typical temperature stability of 15.2 ppm/°C over an extended temperature range from −40 to +85°C. These performance results are obtained without using any trimming in mass production. The bandgap reference only occupies 730 mil^2 and dissipates 4.8 mW at ±5-V power supplies. A measured power supply rejection of about 90 dB until 500 kHz is the best ever reported at high frequency.**

I. Introduction

A KEY ELEMENT of analog-to-digital (A/D) and digital-to-analog (D/A) converters is a precise voltage reference with good temperature stability.

In bipolar technologies one of the most popular implementations uses the extrapolated energy bandgap voltage of silicon [1], [2]. Bandgap references using trimming techniques and curvature compensation achieving high performance have been reported [3]–[6].

In MOS technologies, early implementations of voltage references were based on the difference between the threshold voltages of enhancement- and depletion-mode MOS transistors [7]. Although this technique leads to a low temperature coefficient, as a solution it suffers in that the output voltage is poorly controlled because of its direct dependence on the dose of ion-implantation steps. Another solution exploits the gate voltage difference of two MOS transistors of the same type but having polysilicon gates with opposite doping and biased at identical drain currents [8]. The resulting voltage turns out to be close to the silicon bandgap. The shortcomings of this solution are the need for an extra mask for selective doping of the polysilicon and a resulting voltage with poor temperature stability.

The trend of higher system integration coupled with the constant development efforts to reduce device dimensions have made CMOS the clear choice for VLSI implementations. Analog and digital subsystems are required to coexist on the same die sharing the same device resources. In order to take advantage of the bandgap technique in mixed-mode systems [9], [10], the presence of the parasitic bipolar structure in every CMOS process has been exploited. Unless certain precautions are taken, these circuits suffer from the weaknesses encountered in CMOS circuits, e.g., high op-amp offset. Furthermore, the lack of access to the collector of the BJT's forces the sensing of the emitter instead of the collector currents, which in turn leads to errors caused by the finite current gains. The combination of these effects prevents the achievement of references with good accuracy and temperature stability.

An approach [11] that overcomes most of the limiting factor of the CMOS bandgap implementation uses offset cancellation techniques, base current and base resistance cancellation, and curvature compensation. Drawbacks of this solution are the required double trimming (one for the value of the absolute voltage of the uncompensated reference and the other for tailoring the value of the curvature-compensation term), and the need for a complex circuit to generate all the bias currents, thus consuming a large quantity of area and power.

Other approaches utilize MOS transistors in weak inversion to produce a bipolar-like behavior and CMOS-compatible lateral bipolar transistors, respectively [12]–[14]. Although these techniques avoid the limitation of the substrate BJT regarding the access to the collector, the resulting references have poor power supply rejection (PSR) at audio and above-audio frequencies, that is, from a few kilohertz to 100 kHz; thus it is better to find other solutions for applications where good PSRR is of great importance, such as telephony or audioprocessing systems.

Fully differential circuits are a solution for many of the problems presented by the coexistence of massive portions of digital circuitry and high-performance analog interfaces. Power supply coupling, substrate coupling, single supply operation, and high dynamic range are just a few of the challenges encountered in the VLSI design arena. Op amps, comparators, filters, and A/D and D/A converters are typical examples of circuits that can be implemented using differential techniques [15]–[17].

This paper describes the design of a fully differential CMOS bandgap reference having a very good PSRR with a range of up to a few hundred kilohertz. The design demonstrates that it is possible to implement both high-precision and temperature-stable bandgap voltage references without the use of any trimming in the mass production phase of the integrated circuit. As will be seen, it is sufficient to determine the correct value of the output voltage using a "trimming" procedure only during the design or the preproduction phases, for example, by exploiting the results of a test pattern. Although the lack of trimming for curvature compensation prevents the circuit in question from achieving ultimate performance levels [11], the savings in area and power coupled with the reduction of the production testing time result in a favorable trade-off in large production environments.

Manuscript received January 17, 1990; revised July 25, 1990.

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IEEE Log Number 9040724.

0018-9200/91/0100-0041$01.00 © 1991 IEEE

In Section II a conventional CMOS bandgap reference implementation with a brief review of its limitations is presented and the proposed switched-capacitor bandgap reference is introduced. A previously ignored limiting factor is also discussed. Section III contains a process sensitivity analysis of the output voltage. In Section IV PSRR degradation in fully differential voltage references is explained. Finally, in Section V, experimental results measured from more than 10 000 PCM codec chips (where this reference is used) are presented.

II. The Bandgap Reference

The operation of the bandgap voltage reference is based on the addition of two voltages: one with negative and the other with positive temperature coefficients (TC's), in order to obtain an ideally zero TC. The negative TC voltage is the emitter–base voltage of a bipolar transistor (BJT), and the positive TC voltage is the difference of two emitter–base voltages biased at different current densities. In a conventional CMOS process it is possible to use the parasitic substrate n-p-n or p-n-p transistors in the case of p-well and n-well, respectively (Fig. 1). These transistors, unlike conventional BJT's, have intrinsic limitations that can pose some problems in the development of high-performance voltage references. One example of a typical bandgap realization in a p-well process is shown in Fig. 2. In the same figure the various nonidealities are also shown. The effects of these nonidealities on the output voltage of the reference have been extensively analyzed in [11] and are reported here only as a quick reference:

$$V_{\mathrm{REF}} = V_{BE} + K(\Delta V_{BE} + V_{OS}) \tag{1}$$

$$V_{BE} = V_T \ln \frac{I_1}{I_{SS}} + V_T \ln \frac{1}{1+\dfrac{1}{\beta_1}} + r_b \frac{I_1}{A\beta_1} \tag{2}$$

$$\Delta V_{BE} = V_T \ln A + V_T \ln \frac{I_2}{I_1} + V_T \ln \frac{1+\dfrac{1}{\beta_1}}{1+\dfrac{1}{\beta_2}} + r_b\left(\frac{I_2}{\beta_2} - \frac{I_1}{A\beta_1}\right) \tag{3}$$

where V_{BE} is the emitter–base voltage of $Q1$, ΔV_{BE} is the difference between the emitter–base voltages of $Q2$ and $Q1$, V_{OS} is the op-amp input offset voltage, V_T is the thermal voltage kT/q, I_1 and I_2 are the emitter currents of $Q1$ and $Q2$, respectively, I_{SS} is the saturation current, β_1 and β_2 are the dc current gains of $Q1$ and $Q2$, respectively, r_b is the base resistance, and A is the area factor between $Q1$ and $Q2$.

The offset voltage is the main error source because it is amplified by $1 + R_2/R_1$, leading to a large variation in the output reference voltage and consequently to a very large degradation of its temperature stability. The output voltage of a bandgap reference is generally trimmed to a predetermined value in order to give an ideally zero variation of the output with respect to temperature. Therefore after the trimming operation, the resulting op-amp offset yields an erroneous value, which further triggers a TC error that can be very large (for example, with a typical amplification factor of 10 this error is about 26 ppm/°C per millivolt of offset

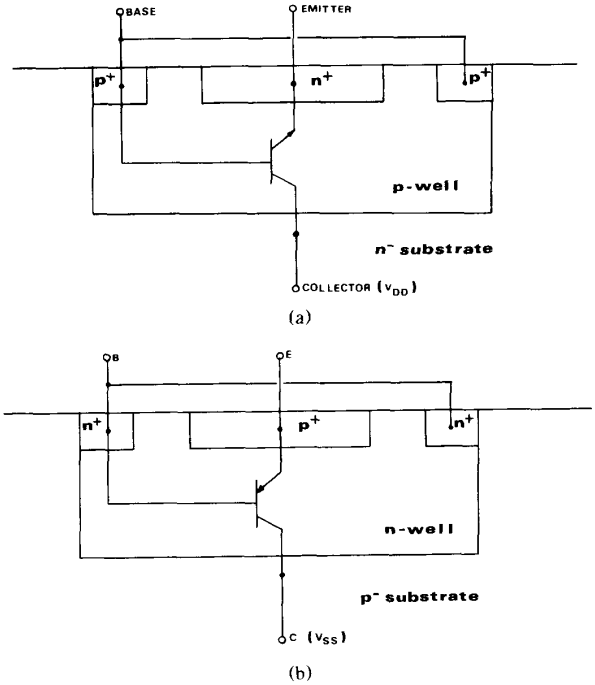


Fig. 1. (a) Substrate n-p-n transistor in a CMOS p-well process. (b) Substrate p-n-p transistor in a CMOS n-well process.

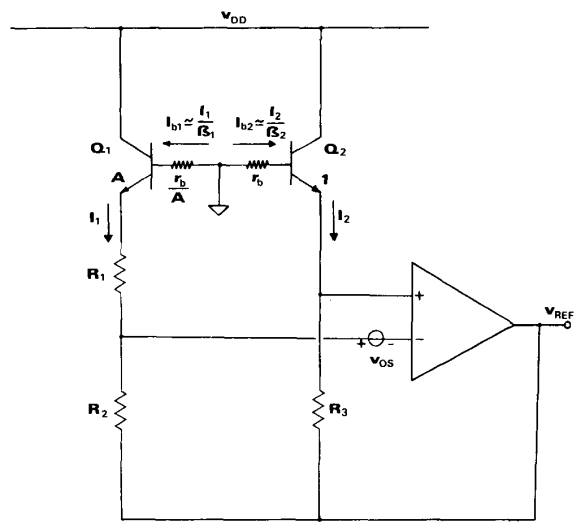


Fig. 2. Example of a conventional CMOS bandgap reference with associated nonidealities.

[11]). This error term must be cancelled to ensure good reproducibility in the output TC.

Fig. 3 depicts the solution utilized to remove the offset from the output voltage. In Fig. 3(a) the switched-capacitor bandgap reference is in the offset storage ϕ_1 phase while in Fig. 3(b) it is in the amplification and useful ϕ_2 phase. The charge injected by switches SW1 and SW2 into the summing node ideally results in a common-mode signal, thus the

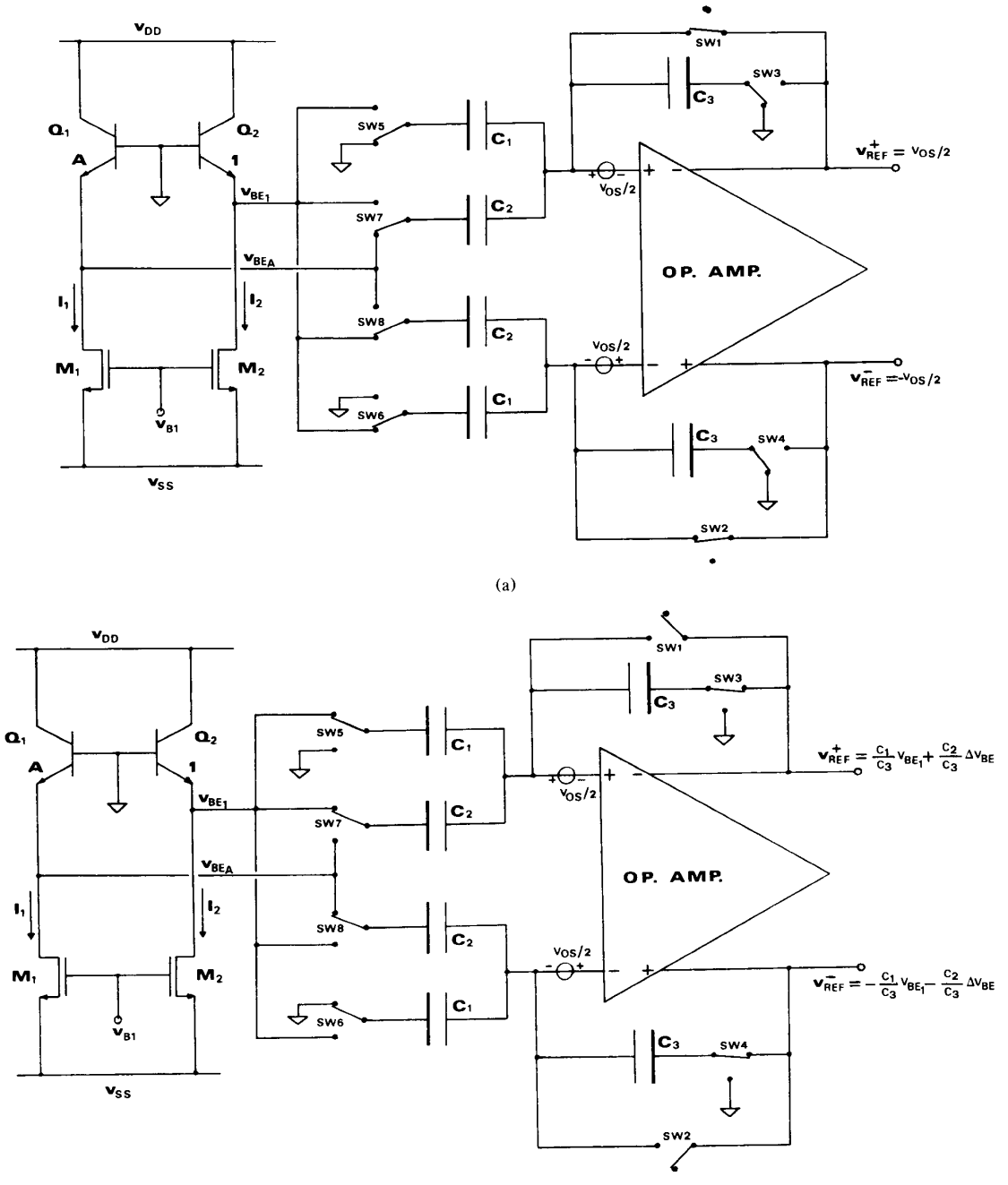


Fig. 3. Switched-capacitor bandgap reference. (a) Offset storage ϕ_1 phase. (b) Amplification ϕ_2 phase.

differential output voltage is not affected by this clock-related error term. A very small differential error may be present due to the mismatches of the switches, but as will be shown in the next section, this error is acceptable for our purposes.

A second error term comes from the different current values I_1 and I_2. In Fig. 3 this effect comes into play in conjunction with the offset between transistors $M1$ and $M2$ and cannot be eliminated by using any offset cancellation techniques. This term has always been neglected in previous bandgap reference implementations (where it arised from op-amp offset V_{OS}, shown in Fig. 2 for example) because it represents a fairly low error of about 1.3 ppm/°C per millivolt of offset on the TC of the output voltage, but assuming a 4σ value of 25 mV for the offset, it is better to find a solution in order to eliminate this error source.

Fig. 4 shows the relatively simple method utilized to eliminate this error source. The currents I_1 and I_2, which are mirrored from a PTAT biasing circuit, can of course be different because of the offset V_{OS_b} between the transistors $M1$ and $M2$, but the "cross-coupled" switching formed by $M3$–$M6$ assures that V_{BE1} and V_{BEA} are biased by the same current even at different phases. This along with the switching scheme of Fig. 3 allows the upper and the lower halves of the bandgap reference to only "see" the currents I_2 and I_1, respectively.

The complete circuit operation and the effect of offsets V_{OS} and V_{OS_b} on reference voltage can be explained in a better way by using charge balancing equations and considering separately the upper and lower halves of the scheme for reasons of symmetry. During ϕ_1

$$V_{\text{REF}}^{+} = \frac{V_{OS}}{2}$$

$$V_{\text{REF}}^{-} = -\frac{V_{OS}}{2}$$

$$V_{\text{REF}} = V_{\text{REF}}^{+} - V_{\text{REF}}^{-} = V_{OS}.$$

During ϕ_2

$$C_3\left(V_{\text{REF}}^{+} - \frac{V_{OS}}{2}\right) + (C_1 + C_2)\left(-V''_{BE1} - \frac{V_{OS}}{2}\right) = (C_3 + C_1)\left(-\frac{V_{OS}}{2}\right) + C_2\left(-V'_{BEA} - \frac{V_{OS}}{2}\right)$$

$$C_3\left(V_{\text{REF}}^{-} + \frac{V_{OS}}{2}\right) + C_1\frac{V_{OS}}{2} + C_2\left(-V''_{BEA} + \frac{V_{OS}}{2}\right) = C_3\frac{V_{OS}}{2} + (C_1 + C_2)\left(-V'_{BE1} + \frac{V_{OS}}{2}\right)$$

where $V'_{BE1}(V'_{BEA})$ and $V''_{BE1}(V''_{BEA})$ are the values of $V_{BE1}(V_{BEA})$ during ϕ_1 and ϕ_2, respectively, that is:

$$V'_{BE1} = V_T \ln \frac{I - g_{m_{1,2}}\frac{V_{OS_b}}{2}}{I_{SS}} = V_T \ln \frac{I}{I_{SS}} + V_T \ln\left(1 - \frac{g_{m_{1,2}}V_{OS_b}}{2I}\right)$$

$$V'_{BEA} = V_T \ln \frac{I + g_{m_{1,2}}\frac{V_{OS_b}}{2}}{10I_{SS}} = V_T \ln \frac{I}{10I_{SS}} + V_T \ln\left(1 + \frac{g_{m_{1,2}}V_{OS_b}}{2I}\right)$$

$$V''_{BE1} = V_T \ln \frac{I + g_{m_{1,2}}\frac{V_{OS_b}}{2}}{I_{SS}} = V_T \ln \frac{I}{I_{SS}} + V_T \ln\left(1 + \frac{g_{m_{1,2}}V_{OS_b}}{2I}\right)$$

$$V''_{BEA} = V_T \ln \frac{I - g_{m_{1,2}}\frac{V_{OS_b}}{2}}{10I_{SS}} = V_T \ln \frac{I}{10I_{SS}} + V_T \ln\left(1 - \frac{g_{m_{1,2}}V_{OS_b}}{2I}\right).$$

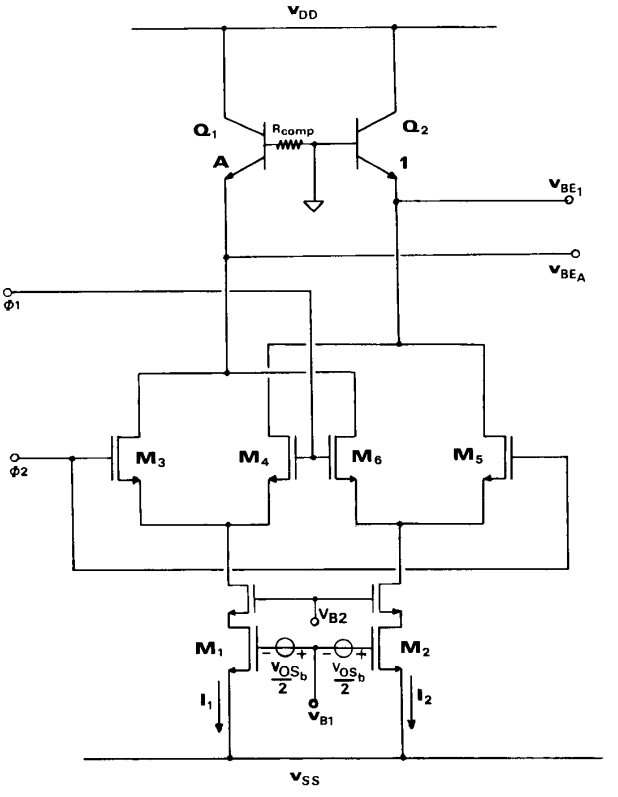


Fig. 4. Offset independent V_{BE} biasing circuit.

Note that in these V_{BE} expressions we consider infinite dc current gain and zero base resistance for simplicity. The effects of finite β and r_b on reference voltage will be considered later in this section.

Solving for V_{REF}^{+} and V_{REF}^{-}:

$$V_{\text{REF}}^{+} = \frac{C_1}{C_3}V''_{BE1} + \frac{C_2}{C_3}(V''_{BE1} - V'_{BEA}) = \frac{C_1}{C_3}V_T \ln \frac{I}{I_{SS}} + \frac{C_2}{C_3}V_T \ln A + \frac{C_1}{C_3}V_T \ln\left(1 + \frac{g_{m_{1,2}}V_{OS_b}}{2I}\right)$$

$$V_{\text{REF}}^{-} = -\frac{C_1}{C_3}V'_{BE1} - \frac{C_2}{C_3}(V'_{BE1} - V''_{BEA}) = -\frac{C_1}{C_3}V_T \ln \frac{I}{I_{SS}} - \frac{C_2}{C_3}V_T \ln A - \frac{C_1}{C_3}V_T \ln\left(1 - \frac{g_{m_{1,2}}V_{OS_b}}{2I}\right).$$

The differential output results in

$$V_{\mathrm{REF}} = 2\left(\frac{C_1}{C_3}V_T \ln\frac{I}{I_{SS}} + \frac{C_2}{C_3}V_T \ln A\right) + \frac{C_1}{C_3}V_T \ln\left[1-\left(\frac{g_{m_{1,2}}V_{OS_b}}{2I}\right)^2\right] = 2\left(\frac{C_1}{C_3}V_{BE} + \frac{C_2}{C_3}\Delta V_{BE}\right) + \epsilon(V_{OS_b}).$$

Consequently, only a very small error $\epsilon(V_{OS_b})$ on the absolute value of the reference output will be present and the error on the TC can be neglected (see Section III).

A third error source is given by the finite TC of the resistor that originates non-PTAT biasing currents I_1 and I_2. This represents a PTAT error term, which must be compensated for by choosing a slightly higher amplification factor, and a PTAT^2 error term which can be cancelled only by a curvature compensation circuit [11].

Curvature compensation requires a complex scheme for generating the various biasing currents needed [11] and a trimming circuit to precisely cancel the PTAT^2 term. We deliberately decided to accept this small error in order to save area and power. Moreover, by avoiding fuses or trimming techniques, it is possible to save part of the testing time in the mass-production phase for IC devices in which the reference is inserted.

With this in mind, we decided to determine the correct value of the output voltage, that is, the value leading to the lowest TC taking into account at the same time the PTAT error due to the resistor. This was done by using a "trimming" procedure only during the design phase in order to eliminate the need for costly trimming during mass production. Thus we exploited the results of a test pattern to find the optimum voltage value, which led to the determination of the required amplification factor.

Other error sources are the nonzero base resistance coupled with the base current and β mismatches of the substrate BJT's together with their temperature variations. These are very small error terms, and although very simple replication techniques [11] can be used to reduce them even more, obviously these circuits require additional die area to be implemented (for example, the duplication of both the bipolar transistors). Thus we decided instead to only include a lumped p-well resistor in series with the base of $Q1$ of value $((1+\beta_1)/(1+\beta_2)) - 1/A)r_b$ in order to compensate for the effect of the intrinsic base resistance, as shown in Fig. 4, and to exploit the fact that the β is practically constant over two decades of current so that the ΔV_{BE} error term due to the finite dc current gain can be neglected. Furthermore, the minimum β value of our process (i.e., 50), the β temperature coefficient, and the r_b value result in less than 1.5 ppm/°C for V_{BE} error terms given by $V_T \ln(1/(1+1/\beta_1))$ and $r_b I_1 / A\beta_1$ in (2). This is acceptable for our purposes.

Finally, the fact that the bandgap of silicon varies with T^2 as well as linearly with T leads to a further curvature term [18] which can only be compensated for by curvature-compensation techniques. For reasons already discussed, this bandgap reference does not utilize any of these techniques.

III. Process Sensitivity of the Bandgap Reference

A brief analysis of the sensitivity of the differential bandgap output to the main processing parameters is presented in this section starting with the reference voltage expression derived from Fig. 3:

$$V_{\mathrm{REF}} = V_{\mathrm{REF}}^{+} - V_{\mathrm{REF}}^{-} = 2(aV_{BE} + b\Delta V_{BE}) \tag{4}$$

where $a = C_1/C_3$ and $b = C_2/C_3$. Given an area factor of $A = 10$, an optimum amplification factor of 9.765 was experimentally determined. Thus, to accommodate for a differential reference requirement of 6.2 V, the a and b terms resulted in equaling 2.56 and 25.0, respectively.

• V_{BE} can be expressed as

$$V_{BE} \sim V_T \ln(\alpha I N_S) \tag{5}$$

where I is the emitter biasing current, N_S the p-well doping, and α a constant keeping the expression dimensionally correct. The change of V_{BE} due to current and p-well ion-implantation errors can be expressed as

$$dV_{BE} \approx V_T\left(\frac{dI}{I} + \frac{dN_S}{N_S}\right). \tag{6}$$

Moreover, considering the PTAT nature of emitter current, that is $I = \Delta V_{BE}/R$, results in the following:

$$\frac{dI}{I} \approx -\frac{dR}{R}. \tag{7}$$

Therefore, using (6) and (7) the following can be derived:

$$dV_{BE} \approx V_T\left(\frac{dR}{R} + \frac{dN_S}{N_S}\right). \tag{8}$$

The doping of the p-well can be controlled to $\pm 10\%$ and the error in poly-resistor value should be $\pm 30\%$.

In reality, this large resistor spread is typical for a process under development, while when a process is fixed or in mass production, the poly variation can be guaranteed to $\pm 10\%$.

The error in output voltage due to p-well dose and poly spreads is

$$dV_{\mathrm{REF}} \approx 2adV_{BE} = 26\ \mathrm{mV}. \tag{9}$$

• A second process uncertainty is given by V_{BE} mismatch. The maximum mismatch, measured on devices biased with the same current in different chip sites of several wafers, resulted in less than 0.2 mV. Thus the output voltage variation due to V_{BE} mismatch is

$$dV_{\mathrm{REF}} \approx 2(a+b)dV_{BE} = 11\ \mathrm{mV}. \tag{10}$$

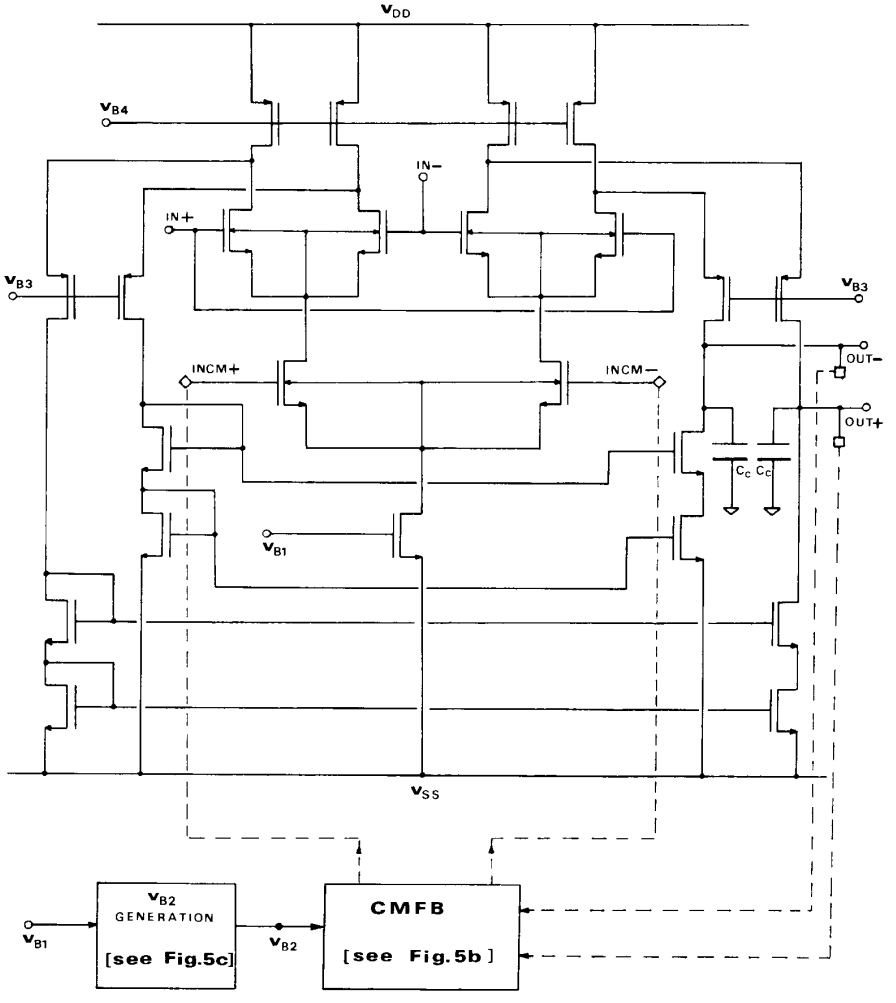
• A third error contributor comes from the offset between transistors $M1$ and $M2$ in Fig. 4, which leads the upper and the lower halves of the reference to "see" a difference ΔI into BJT biasing currents, as explained in Section II:

$$dV_{BE} \approx \frac{V_T}{2}\ln\left(1-\left(\frac{\Delta I}{I}\right)^2\right) = \frac{V_T}{2}\ln\left(1-\left(\frac{g_{m_{1,2}}V_{OS_b}}{2I}\right)^2\right). \tag{11}$$

Therefore the error in output voltage results in

$$dV_{\mathrm{REF}} \approx 2adV_{BE} = 0.43\ \mathrm{mV} \tag{12}$$

supposing $I = 25\ \mu\mathrm{A}$, $g_{m_{1,2}} = 100\ \mu\mathrm{A/V}$, and a maximum offset of 20 mV.



(a)

Fig. 5. Op-amp schematic: (a) core. (Continued on p. 47.)

•Another potential error factor is due to the charge mismatch between switches SW1 and SW2 of Fig. 3 in the amplification phase. If we consider that half the switch charge is injected into the op-amp inputs and model this effect by a capacitor C_{SW} (that is, a very simple model of charge sharing), it can be shown that

$$dV_{\mathrm{REF}} \approx \frac{1}{1+\dfrac{C_3}{C_{SW}}} \frac{\Delta C_{SW}}{C_{SW}} V_{\mathrm{clock}} = 1.5\ \mathrm{mV} \qquad (13)$$

if $W = 4\ \mu$m and $L = 4\ \mu$m for the reset switches, $C_3 = 1$ pF, and considering a maximum mismatch of 5%.

•Finally, the precision of the output voltage is directly related to the op-amp open-loop gain value and to the mismatch of capacitor ratio C_1 to C_2.

A simulated minimum open-loop gain of 40 000 leads to a 0.07% error on the output accuracy. By exploiting known techniques [19] to minimize systematic errors on capacitor ratios (array design with constant area-to-perimeter ratio, dummy-plate guard ring, etc.) and choosing geometries of $40 \times 40\ \mu\mathrm{m}^2$ for unit capacitor size, the mismatch is less than 0.1% [20]. These combined effects are reflected in a reference output change of about 0.17%.

The total relative error on the voltage value of the bandgap reference can be obtained from the last result and from (9), (10), (12), and (13):

$$\frac{\Delta V_{\mathrm{REF}}}{V_{\mathrm{REF}}} = \pm 0.81 \times 10^{-2}$$

which means an accuracy of about ± 0.07 dB in the worst case.

The degradation of TC due to process variations, assuming that (13) is independent from temperature in the first order, becomes approximately

$$\mathrm{TC}_{\mathrm{process}} \approx 20\ \mathrm{ppm/°C}$$

for a temperature range of -40 to $+85$°C. Therefore, considering that the absence of curvature correction leads to a

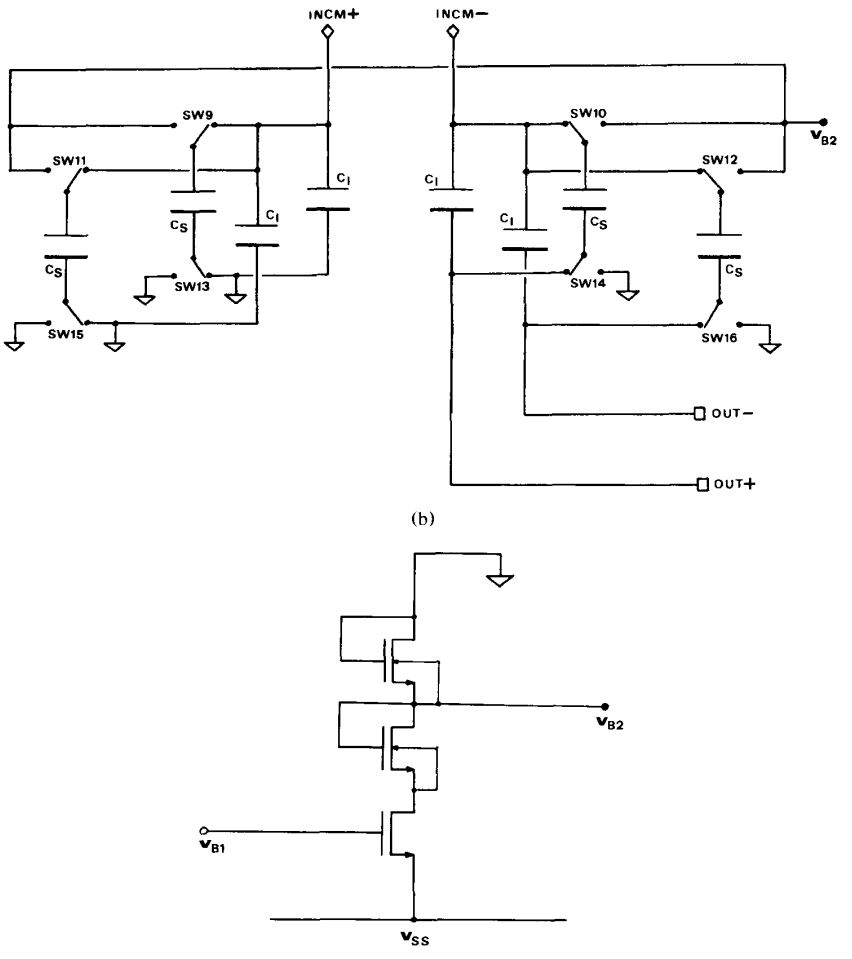


Fig. 5. Op-amp schematic: (b) CMFB circuit, and (c) biasing circuit for CMFB inputs.

TC of about 17 ppm/°C in the above temperature range, the worst possible TC of the proposed bandgap reference is:

$$TC_{ref} \approx 37 \text{ ppm/°C}$$

for a temperature range of -40 to $+85$°C.

These calculated results are quite satisfactory for PCM codec filter chips, where this reference is used, and for most high-performance audioprocessing IC's.

IV. Power Supply Rejection (PSR) of the Bandgap Reference

The biasing currents I_1 and I_2 present a very large PSR due to the choice of the poly resistor for determining the PTAT current. In addition, V_{BE_1} and V_{BE_A} of the parasitics BJT's are referred to ground producing a high decoupling of the power supply variations and noise. In fact, for frequencies much less than the f_t of the BJT's, the power supply noise coupling V_{E_n} is approximately given by

$$V_{E_n} \simeq \frac{1}{g_{m_{Q1,2}}}\left(g_{o_{Q1,2}}V_{S_n}^{+} + g_{o_{M1,2}}V_{S_n}^{-}\right)$$

where $V_{S_n}^{+}$ and $V_{S_n}^{-}$ are the power supply noise superimposed to V_{DD} and V_{SS}, respectively, $g_{m_{Q1,2}}$ is the BJT transconductance, and $g_{o_{Q1,2}}$ and $g_{o_{M1,2}}$ are the output conductances of C_1 and C_2 and the cascoded pair M_1 and M_2, respectively.

To analyze the V_{E_n} effect on the reference output during the useful phase ϕ_2, we can use charge balancing equations:

$$V_{\text{REF}_n}^{+}(t) = \frac{C_1}{C_3}V_{E_n}(t) + \frac{C_2}{C_3}V_{E_n}(t) - \frac{C_2}{C_3}V_{E_n}(t_1)$$

$$V_{\text{REF}_n}^{-}(t) = -\frac{C_1}{C_3}V_{E_n}(t_1) - \frac{C_2}{C_3}V_{E_n}(t_1) + \frac{C_2}{C_3}V_{E_n}(t)$$

$$V_{\text{REF}_n}(t) = \frac{C_1}{C_3}\left[V_{E_n}(t) + V_{E_n}(t_1)\right]$$

where $V_{E_n}(t_1)$ is the sampled value of V_{E_n} at the end of the ϕ_1 phase and $V_{E_n}(t)$ are the "continuous" values of V_{E_n} during the ϕ_2 phase.

Other power supply noise couplings at the bandgap output can only arise from switch and op-amp mismatches since the common-mode noise is rejected by the differential nature of the reference voltage processing.

The same charge-sharing model used in Section III can be exploited to estimate the contribution of the switches SW1 and SW2 to the power supply degradation during the amplification phase ϕ_2. Using (13) the PSR yields approximately 90 dB for a typical mismatch of 1% between the switches. Supply noise coupling due to the op amp can arise from the internal and common-mode feedback (CMFB) paths.

Fig. 5(a) shows the op-amp configuration used in the switched-capacitor bandgap reference. $IN\pm$ and $INCM\pm$ are the op-amp differential- and common-mode inputs, respectively. V_{B4}, V_{B3}, and V_{B1} are derived from the PTAT biasing circuit already mentioned in Section II.

Internal common-mode couplings can be eliminated or greatly reduced by employing supply-independent current sources, placing the input devices in an isolated well, and using a cascode or folded-cascode configuration in order to buffer the drain of the input transistors from power supply variations [21]. Another important advantage of cascode architecture is that it does not suffer from the degradation of the PSR at high frequencies because its compensation capacitors are connected to signal ground [22].

Thus the op-amp PSR is determined primarily by CMFB implementation. A dynamic CMFB circuit (Fig. 5(b)) was chosen because of its simplicity, higher degree of linearity, smaller area, and lower power consumption compared to its continuous counterparts. The two nonoverlapping phases are the same ones used for the differential reference generation shown in Fig. 3.

The amount of power supply noise coupled to the op-amp differential output can be analyzed as the combination of coupling from the power supplies to the common-mode output (that is, each output referred to ground) and the transformation of this into a differential signal by mismatch effects. To avoid common-mode noise on the outputs, the biasing voltage V_{B2} for $INCM\pm$ is referred to signal ground by exploiting the simple circuit shown in Fig. 5(c). Moreover, the duplication of the CMFB input allows for a considerable reduction in common-mode clock feedthrough or charge sharing due to the CMFB switches with superimposed power supply noise.

V. Experimental Results

A test chip containing the switched-capacitor fully differential bandgap reference was realized and a trimming procedure was applied to it in order to determine the correct value of the amplification factor leading to a minimum TC. Afterwards this chip was integrated as reference voltage for a complete PCM codec chip without the use of any further trimming. A self-aligned, double-poly, single-metal, 3.5-μm, Si-gate, p-well CMOS fabrication process was used.

A microphotograph of the bandgap circuit is shown in Fig. 6. The active area is about 730 mil^2 and power dissipation is typically 4.8 mW with $\pm$5-V power supplies.

Fig. 7 shows the output waveform of the switched-capacitor bandgap reference. A clock period of 125 μs was used, which gives to the ϕ_1 and ϕ_2 phases a logical "high" period of 7.8125 and 117.1875 μs, respectively, once the disoverlapping time is subtracted.

In Table I, statistical data from more than 10 000 PCM codec chips are presented. Temperature coefficients are given for an extended temperature range from -40 to $+85$°C and for $\pm$5-V$\pm$5% power supplies.

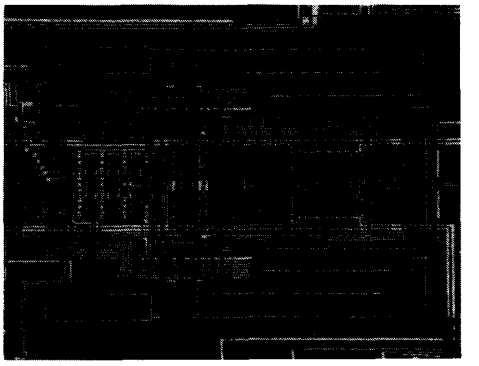


Fig. 6. Bandgap microphotograph.

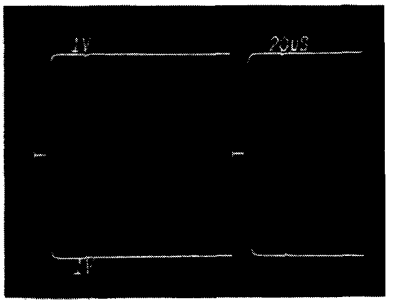


Fig. 7. Output waveform.

Fig. 8 shows a statistical plot of absolute accuracy reflecting a Gaussian distribution type with a standard deviation of about 0.034 dB. Aging variations (long-term stability) of absolute accuracy can be neglected (less than 0.006 dB after 1800 h).

Typical power supply rejections (defined as the ratio between noise signal coupled on the differential output and the 100-mV$_{rms}$ noise signal injected on each supply) versus frequency for both positive and negative supplies are shown in Fig. 9. Note that these PSR values are the best ever reported at high frequencies since they remain extremely high (i.e., greater than 90 dB) until 500 kHz.

The experimental setup used to measure the PSR of this switched-capacitor bandgap reference is described in the Appendix.

Table II summarizes the overall performance of the integrated bandgap reference.

VI. Conclusions

The switched-capacitor fully differential CMOS bandgap reference described in this paper was realized without the use of any trimming during mass production. In a temperature range of -40 to $+85$°C and with power supplies of $\pm$5 V$\pm$5%, it is capable of achieving a worst-case absolute accuracy and temperature drift of 0.11 dB and 40.3 ppm/°C, respectively.

Smaller area and lower power dissipation in comparison to previous solutions, combined with a very good power supply rejection even at high frequency, make this bandgap suitable

TABLE I
STATISTICS OF MEASURED ACCURACY AND TEMPERATURE COEFFICIENT OF 10865 SAMPLES (−40 to +85°C, ±5 V±5%)

	Mean	St. Deviation	Minimum	Maximum
Absolute accuracy (dB)	+0.002	0.034	−0.11	+0.095
Temperature coefficients (ppm)/°C	15		9.5	40.3

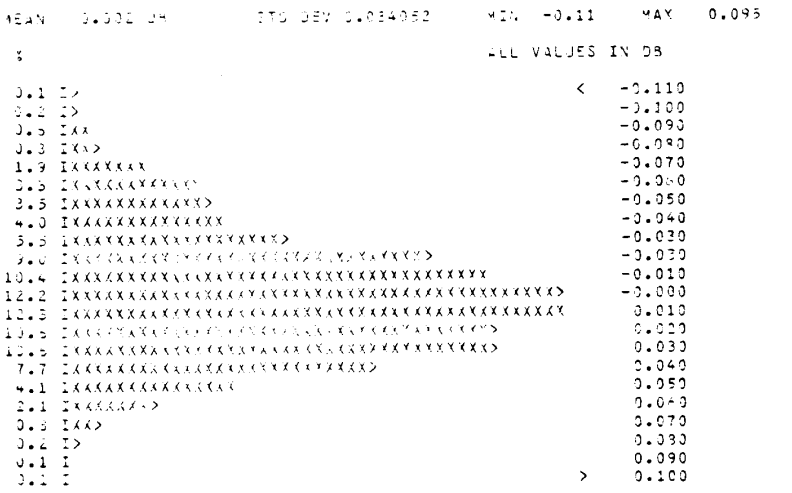


Fig. 8. Statistical plot of absolute accuracy.

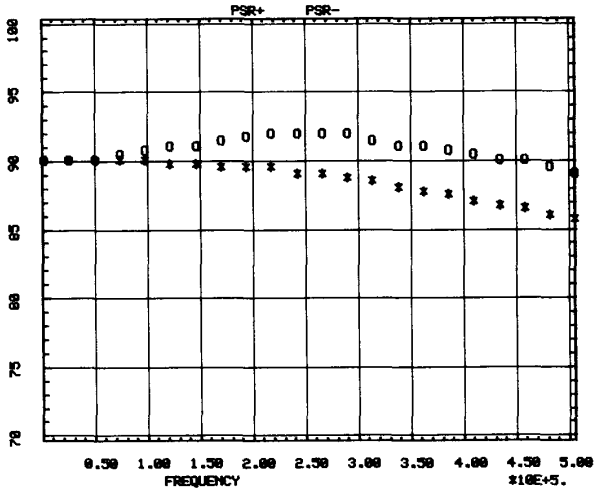


Fig. 9. PSR of the reference versus frequency for positive (upper trace) and negative (lower trace) supplies.

TABLE II
PERFORMANCE SUMMARY

V_{REF}	6.2-V differential at 27°C and ±5 V
TC	see Table I
Active area	730 mil^2
Power dissipation	4.8 mW at ±5 V
PSR+	⩾ 90 dB until 500 kHz
PSR−	⩾ 86 dB until 500 kHz
Output noise	320 μV_{rms} (500 kHz)

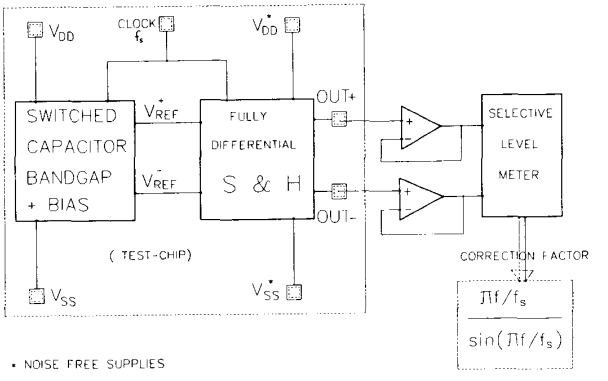


Fig. 10. Experimental setup for PSR measurements.

for high-precision mixed-mode integrated circuits using the fully differential approach.

APPENDIX
PSR MEASUREMENTS OF THE SWITCHED-CAPACITOR BANDGAP REFERENCE

The measurement of the PSR, for frequencies less than the Nyquist rate, was achieved by exploiting the scheme shown in Fig. 10. That is, a S/H circuit [23] was integrated in the same test chip with separated and noise-free power supplies in order to avoid deteriorating the PSR results. Sample and hold phases of the S/H are logically coincident with the ϕ_2 and ϕ_1 phases of the bandgap reference generation, respectively.

Typical PSR's of about 90 dB were obtained for both positive and negative supplies. These values are caused by switch mismatches and BJT output conductance since the

op-amp PSR is much higher than 90 dB at frequencies less than 4 kHz. At high frequencies, the PSR performance is expected to be degraded by internal op-amp mismatches.

The same scheme of Fig. 10 was also used to measure the PSR for frequencies higher than the Nyquist rate. This was done by injecting high-frequency sine waves into the power supplies and measuring the various aliased components in the Nyquist band. The positive PSR is about 90 dB while the negative PSR varies from 90 to 86 dB for frequencies less than 500 kHz.

Acknowledgment

The authors wish to thank C. Crippa and C. Dallavalle for their cooperation during the design and mass-production phases, and A. Calloni for the careful layout.

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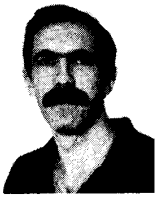

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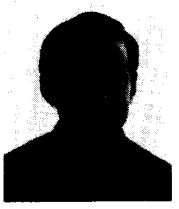

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