Lecture 13 - Digital Circuits (II)

MOS Inverter Circuits

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Reading assignment:

Howe and Sodini, Ch. 5, §5.3
Key questions

• What are the key design trade-offs of the NMOS inverter with resistor pull-up?
• How can one improve upon these trade-offs?
• What is special about a CMOS inverter?
1. NMOS inverter with resistor pull-up (cont.)

- $C_L$ pull-down limited by current through transistor [will study in detail with CMOS]
- $C_L$ pull-up limited by resistor ($t_{PLH} \sim RC_L$)
- pull-up slowest
Inverter design issues:

noise margins $\uparrow \Rightarrow |A_v| \uparrow \Rightarrow$

- $R \uparrow \Rightarrow RC_L \uparrow \Rightarrow$ slow switching
- $g_m \uparrow \Rightarrow W \uparrow \Rightarrow$ big transistor
  (slow switching at input)

Trade-off between speed and noise margin.

During pull-up, need:

- high current for fast switching,
- but also high resistance for high noise margin.

$\Rightarrow$ use current source as pull-up.
2. NMOS inverter with current-source pull-up

I-V characteristics of current source:

![I-V characteristics graph]

Equivalent circuit models:

- Large-signal model
- Small-signal model

- high current throughout voltage range: \( i_{SUP} \approx I_{SUP} \)
- high small-signal resistance, \( r_{oc} \).
NMOS inverter with current-source pull-up:

Transfer characteristics:

High $r_{oc} \Rightarrow$ high noise margin
Dynamics:

Faster pull-up because capacitor charged at constant current.
PMOS as current-source pull-up

I-V characteristics of PMOS:

Note: enhancement-mode PMOS has $V_{Tp} < 0$.

In saturation:

$$-I_{Dp} \propto (V_{SG} + V_{Tp})^2$$
Circuit and load-line diagram of inverter with PMOS current source pull-up:

PMOS load line for $V_{SG} = V_{DD} - V_B$

Transfer function:
Noise margin:

- compute $V_M = V_{IN} = V_{OUT}$
- compute $|A_v(V_M)|$

At $V_M$ both transistors saturated:

$$I_{Dn} = \frac{W_n}{2L_n} \mu_n C_{ox} (V_M - V_{Tn})^2$$

$$-I_{Dp} = \frac{W_p}{2L_p} \mu_p C_{ox} (V_{DD} - V_B + V_{Tp})^2$$

And:

$$I_{Dn} = -I_{Dp}$$

Then:

$$V_M = V_{Tn} + \sqrt{\frac{W_p}{\mu_p L_p}} (V_{DD} - V_B + V_{Tp}) \sqrt{\frac{\mu_n L_n}{W_n}}$$
Small-signal equivalent circuit model at $V_M$:

$$A_v = -g_{mn} \left( \frac{r_{on}}{r_{op}} \right)$$
NMOS inverter with current-source pull-up allows fast switching with high noise margins.

But... when $V_{IN} = V_{DD}$, there is a direct current path between supply and ground $\Rightarrow$ power consumption even if inverter is idling.

Would like to have current source that is itself switchable, i.e., it shuts off when input is high $\Rightarrow$ CMOS!
3. Complementary MOS (CMOS) Inverter

Circuit schematic:

\[ \text{V}_{IN} \quad \text{V}_{OUT} \quad \text{V}_{DD} \quad \text{CL} \]

Basic operation:

- \( V_{IN} = 0 \Rightarrow V_{OUT} = V_{DD} \)
  
  \[ V_{GSn} = 0 < V_{Tn} \Rightarrow \text{NMOS OFF} \]
  
  \[ V_{SGp} = V_{DD} > -V_{Tp} \Rightarrow \text{PMOS ON} \]

- \( V_{IN} = V_{DD} \Rightarrow V_{OUT} = 0 \)
  
  \[ V_{GSn} = V_{DD} > V_{Tn} \Rightarrow \text{NMOS ON} \]
  
  \[ V_{SGp} = 0 < -V_{Tp} \Rightarrow \text{PMOS OFF} \]

No power consumption while idling in any logic state.
Key conclusions

- In NMOS inverter with resistor pull-up: trade-off between noise margin and speed.
- Trade-off resolved using current-source pull-up: use PMOS as current source.
- In NMOS inverter with current-source pull-up: if $V_{IN} = HI$, power consumption even if inverter is idling.
- Complementary MOS: NMOS and PMOS switch alternatively $\Rightarrow$ no power consumption while idling.