Lecture 21 - Multistage Amplifiers (I)

Multistage Amplifiers

May 1, 2001

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Reading assignment:

Howe and Sodini, Ch. 9, §§9.1-9.3
Key questions

• How can one build a wide range of high-performance amplifiers using the single-transistor stages studied so far?

• What are the most important considerations when assembling multistage amplifiers:
  – regarding interstage loading?
  – regarding interstage biasing?
1. Introduction

Amplifier requirements are often demanding:

- must adapt to specific kinds of signal source and load,
- must deliver sufficient gain

Single-transistor amplifier stages are very limited in what they can accomplish ⇒ multistage amplifier.

Issues:

- What amplifying stages should be used and in what order?
- What devices should be used, BJT or MOSFET?
- How is biasing to be done?
\[ \square \] Summary of single stage characteristics:

<table>
<thead>
<tr>
<th>stage</th>
<th>( A_{vo}, G_{mo}, A_{io} )</th>
<th>( R_{in} )</th>
<th>( R_{out} )</th>
<th>key function</th>
</tr>
</thead>
<tbody>
<tr>
<td>common source</td>
<td>( G_{mo} = g_m )</td>
<td>( \infty )</td>
<td>( r_o/r_{oc} )</td>
<td>transconductance amp.</td>
</tr>
<tr>
<td>common drain</td>
<td>( A_{vo} \simeq \frac{g_m}{g_m+g_{mb}} )</td>
<td>( \infty )</td>
<td>( \frac{1}{g_m+g_{mb}} )</td>
<td>voltage buffer</td>
</tr>
<tr>
<td>common gate</td>
<td>( A_{io} \simeq -1 )</td>
<td>( \frac{1}{g_m+g_{mb}} )</td>
<td>( r_{oc}/[r_o(1+g_mR_S)] )</td>
<td>current buffer</td>
</tr>
<tr>
<td>common emitter</td>
<td>( G_{mo} \simeq g_m )</td>
<td>( r_\pi )</td>
<td>( r_o/r_{oc} )</td>
<td>transconductance amp.</td>
</tr>
<tr>
<td>common collector</td>
<td>( A_{vo} \simeq 1 )</td>
<td>( r_\pi + \beta(r_o/r_{oc}/R_L) )</td>
<td>( \frac{1}{g_m} + \frac{R_S}{\beta} )</td>
<td>voltage buffer</td>
</tr>
<tr>
<td>common base</td>
<td>( A_{io} \simeq -1 )</td>
<td>( \frac{1}{g_m} )</td>
<td>( r_{oc}/{r_o[1 + g_m(r_\pi/R_S)]} )</td>
<td>current buffer</td>
</tr>
</tbody>
</table>

\[ \square \] Key differences between BJT’s and MOSFETs:

**BJT**  
\[ I_B = \frac{I_C}{\beta} \gg I_G = 0 \]

\[ g_m = \frac{qI_C}{kT} > g_m = \sqrt{\frac{2W}{L}\mu C_{ox}I_D} \]

\[ r_o = \frac{V_A}{I_C} > r_o = \frac{1}{\lambda I_D} \]

**MOSFET**
2. CMOS multistage voltage amplifier

- Goals:
  - high voltage gain
  - high $R_{in}$
  - low $R_{out}$

- Good starting point: CS stage

\[
\begin{align*}
R_{in} &= \infty \\
A_{vo} &= -g_m\left(r_o//r_{oc}\right), \text{ probably insufficient} \\
R_{out} &= r_o//r_{oc}, \text{ too high}
\end{align*}
\]
\( \Box \) Add second CS stage to get more gain:

\[
\begin{align*}
\text{v}_{\text{out1}} &= \text{v}_{\text{in2}} - g_{m1} \left( r_{o1} // r_{oc1} \right) \text{v}_{\text{in1}} \\
\text{v}_{\text{out2}} &= -g_{m2} \left( r_{o2} // r_{oc2} \right) \text{v}_{\text{in2}}
\end{align*}
\]

- \( R_{\text{in}} = \infty \)
- \( A_{vo} = g_{m1} (r_{o1} // r_{oc1}) g_{m2} (r_{o2} // r_{oc2}) \)
- but \( R_{\text{out}} = r_{o2} // r_{oc2} \), still high

\( \Box \) Add CD stage at output:

\[
\begin{align*}
\text{v}_{\text{out}} &= \text{v}_{\text{in3}} - g_{m3} \frac{1}{g_{m3} + g_{mb3}} \text{v}_{\text{in3}} \\
&= -g_{mb3} + \frac{g_{m3}}{g_{m3} + g_{mb3}} \text{v}_{\text{in3}}
\end{align*}
\]

- \( R_{\text{in}} = \infty \)
- \( A_{vo} = g_{m1} (r_{o1} // r_{oc1}) g_{m2} (r_{o2} // r_{oc2}) \frac{g_{m3}}{g_{m3} + g_{mb3}} \), still high
- \( R_{\text{out}} = \frac{1}{g_{m3} + g_{mb3}} \), now small
3. BiCMOS multistage voltage amplifier

\[ A_{vo}(CE) > A_{vo}(CS) \] because \( r_o(BJT) > r_o(MOSFET) \) and \( g_m(BJT) > g_m(MOSFET) \) but...

CS stage is best first stage, since \( R_{in} = \infty \).

\[ \square \] Add CE stage following CS stage?

\[
\begin{align*}
\frac{R_{in2}}{R_{out1} + R_{in2}} & \approx \frac{R_{in2}}{R_{out1}} \approx \frac{r_{\pi2}}{r_{o1}/r_{oc1}} \ll 1 \\
\end{align*}
\]

Additional gain provided by CE stage more than lost in interstage loading.
Use two CS stages, but add CC stage at output:

\[
\begin{align*}
R_{out 2} &= r_{o2} \parallel r_{oc2}, \\
R_{in 3} &= r_{\pi 3} + \beta_3 (r_{o3} \parallel r_{oc3} \parallel R_L)
\end{align*}
\]

Interstage loading:

\[
\frac{R_{in 3}}{R_{out 2} + R_{in 3}} = \frac{r_{\pi 3} + \beta_3 (r_{o3} \parallel r_{oc3} \parallel R_L)}{r_{o2} \parallel r_{oc2} + r_{\pi 3} + \beta_3 (r_{o3} \parallel r_{oc3} \parallel R_L)}
\]

better than trying to use a CE stage, but still pretty bad.

Benefit is that \( R_{out} \) has improved:

\[
R_{out} = R_{out 3} = \frac{1}{g_{m3}} + \frac{R_{out 2}}{\beta_3} = \frac{1}{g_{m3}} + \frac{r_{o2} \parallel r_{oc2}}{\beta_3}
\]

Since, in general, \( g_m(BJT) > g_m(MOSFET) \), \( R_{out} \) could be better than CD output stage if \( r_{o2} \parallel r_{oc2} \) is not too large. Otherwise, CD stage output is better.
Better voltage buffer: cascade CC and CD output stages.

What is best order? Since $R_{in}(CD) = \infty$, best to place CD first:

Interstage loading:

\[
\frac{R_{in3}}{R_{out2} + R_{in3}} = 1
\]

\[
\frac{R_{in4}}{R_{out3} + R_{in4}} = \frac{r_{\pi4} + \beta_4(r_{o4} || r_{oc4} || R_L)}{g_{m3} + g_{mb3} + r_{\pi4} + \beta_4(r_{o4} || r_{oc4} || R_L)} \approx 1
\]

and excellent output resistance:

\[
R_{out} = R_{out4} = \frac{1}{g_{m4}} + \frac{R_{out3}}{\beta_4} = \frac{1}{g_{m4}} + \frac{1}{\beta_4(g_{m3} + g_{mb3})}
\]
4. BiCMOS current buffer

□ Goals:

- Unity current gain
- VERY low $R_{in}$
- VERY high $R_{out}$

Start with common-base stage:

\[
\begin{align*}
A_{io} &= -1 \\
R_{in} &= \frac{1}{g_m} \\
R_{out} &= r_{oc}/\{r_o[1 + g_m(r_{\pi}/R_S)]\}
\end{align*}
\]

Note that if $R_S$ is not too low, $R_{out} \simeq r_{oc}/(\beta r_o)$.

Can we further increase $R_{out}$ by adding a second CB stage?
**CB-CB current buffer:**

\[
\begin{align*}
i_{out} &= i_{in1} - i_{in2} \\&= (1 - \beta_1 \frac{r_{oc1}}{r_{oc2}}) i_{in1} \\&= \left(\left[\frac{g_{m2} r_{oc2}}{r_{oc1} + \beta_1 r_{oc1}}\right]\right) i_{in1} \\
\end{align*}
\]

Now

\[
R_{out} = R_{out2} = r_{oc2} / \left\{ r_{o2} \left[ 1 + g_{m2} (r_{\pi2} / R_{out1}) \right] \right\}
\]

Plugging in \( R_{out1} \simeq \frac{r_{oc1}}{(\beta_1 r_{o1})} \),

\[
R_{out} = r_{oc2} / \left\{ r_{o2} \left[ 1 + g_{m2} (r_{\pi2} / r_{oc1} / (\beta_1 r_{o1})) \right] \right\}
\]

But, since \( r_{\pi2} \ll r_{oc1} / (\beta_1 r_{o1}) \), then

\[
R_{out} \simeq r_{oc2} / \left[ r_{o2} (1 + g_{m2} r_{\pi2}) \right] \simeq r_{oc2} / (\beta_2 r_{o2})
\]

Did not improve anything! The base current limits the number of CB stages that improve \( R_{out} \) to just one.

Since CG stage has no gate current, cascade it behind CB stage.
CB-CG current buffer:

\[ R_{out} = R_{out2} = r_{oc2} / /[r_{o2}(1 + g_{m2}R_{out1})] \]

with \( R_{out1} \approx r_{oc1} / / (\beta_1 r_{o1}) \),

\[ R_{out} = r_{oc2} / /[r_{o2}g_{m2}(r_{oc1} / / \beta_1 r_{o1})] \]

Now \( R_{out} \) has improved by about \( g_{m2}r_{o2} \), but only to the extent that \( r_{oc2} \) is high enough...
5. Coupling amplifier stages

- **CAPACITIVE COUPLING**

Capacitors of large enough value behave as AC short, so signal goes through but bias is independent for each stage.

Example, CD-CC voltage buffer:

- **Advantages:**
  - can select bias point for optimum operation
  - can select bias point close to middle of rails for maximum signal swing

- **Disadvantages:**
  - to approximate AC short, need large capacitors that consume significant area
Direct coupling: share bias points across stages.

Example, CD-CC voltage buffer:

- Advantages:
  - no capacitors: compact

- Disadvantages:
  - bias point shared: constrains design
  - bias shifts from stage to stage and can stray too far from center of range
Solution: use PMOS CD stage:

![PMOS CD stage diagram]

Assumes $V_{BE} = 0.7\,\text{V}$
$V_{GS} = 1.5\,\text{V}$

Trade-off: $g_m(\text{PMOS}) < g_m(\text{NMOS}) \rightarrow$ lower gain
Summary of DC shifts through amplifier stages:

<table>
<thead>
<tr>
<th>Amplifier Type</th>
<th>Transistor Type</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>NMOS</td>
</tr>
<tr>
<td>Common Source/ Common Emitter (CS/CE)</td>
<td><img src="image" alt="NMOS Diagram" /></td>
</tr>
<tr>
<td>Common Gate/ Common Base (CG/CB)</td>
<td><img src="image" alt="NMOS Diagram" /></td>
</tr>
<tr>
<td>Common Drain/ Common Collector (CD/CC)</td>
<td><img src="image" alt="NMOS Diagram" /></td>
</tr>
</tbody>
</table>
Important difference in bias shift between stages in BJT and MOSFET amps:

• In BJT (for npn):

\[ V_{BE} \approx V_{BE, on} \]

rather independent of transistor size and current level.

• In MOSFET (for nMOSFET):

\[ V_{GS} = V_T + \sqrt{\frac{2I_D L}{\mu_n C_{ox} W}} \]

Can be engineered through bias current and transistor geometry.

Assumes \( V_{BE} = 0.7 \) V

\( V_{GS} = 1.5 \) V
Key conclusions

- To achieve amplifier design goals, several stages often needed.
- In multistage amplifiers, different stages used to accomplish different goals:
  - voltage gain: common-source, common emitter
  - voltage buffer: common-drain, common collector
  - current buffer: common-gate, common base
- In multistage amplifiers must pay attention to inter-stage loading to avoid unnecessary losses.
- In \textit{direct-coupled} amplifiers, bias is shared between adjoining stages:
  - must select compromise bias,
  - must pay attention to bias shift from stage to stage.