Lecture 26 - Differential Amplifiers (II)

and

6.012 Wrap-up

May 17, 2001

Contents:

1. Large-signal differential response of differential amplifier

2. Wrap-up of 6.012

Reading assignment:

Howe and Sodini, Ch. 11, §§11.6

Announcement:

Final exam: May 24, 9 AM-12 noon, Walker; open book, calculator required; entire subject under examination but emphasis on lectures #18-26.
Key questions

• Is it possible to use the differential amplifier concept to do logic?
1. Large-signal differential response of differential amplifier

Examine large-signal transfer function:

- if \( v_{I1} = v_{I2} \) \( \Rightarrow v_{O1} = v_{O2} \) \( \Rightarrow v_O = 0 \)

- if \( v_{I1} > v_{I2} \) \( \Rightarrow \) M1 more \( ON \) than M2 \( \Rightarrow i_1 > i_2 \) \( \Rightarrow v_{O1} < v_{O2} \) \( \Rightarrow v_O < 0 \)

- if \( v_{I1} \gg v_{I2} \) \( \Rightarrow \) M1 strongly \( ON \), M2 goes \( OFF \) \( \Rightarrow i_1 \approx I_{BIAS}, i_2 \approx 0 \) \( \Rightarrow \)

\[
    v_{O1} = v_{O1,min} = V_{DD} - I_{BIAS}R_D, \quad v_{O2} = v_{O1,max} = V_{DD}
\]

\[
    v_{OD,min} = -I_{BIAS}R_D
\]

- symmetric behavior for \( v_{I1} < v_{I2} \) and \( v_{I1} \ll v_{I2} \)
Saturating behavior for large differential input signals:

\[ v_{O1}, v_{O2} \]

\[ v_{O2} \]

\[ v_{O1} \]

\[ v_{ID} = v_{I1} - v_{I2} \]

\[ v_{ID,sat} - v_{ID,sat} \]

\[ V_{DD} - I_{BIAS} R_D \]

\[ V_{DD} \]

\[ v_{O, swing} = I_{BIAS} R_D \]

\[ -v_{ID,sat} \]

\[ 0 \]

\[ v_{ID,sat} \]

\[ v_{ID} = v_{I1} - v_{I2} \]

\[ v_{ID, sat} = v_{GS1} - v_{GS2} \]

With:

\[ v_{GS1} = V_T + \sqrt{\frac{I_{BIAS}}{W \mu C_{ox}}} \]

\[ v_{GS2} = V_T \]

Then:

\[ v_{ID, sat} = \sqrt{\frac{I_{BIAS}}{W \mu C_{ox}}} \]
For small $v_{ID}$, $v_O$ is linear in $v_I \Rightarrow$ differential amplifier

For large $v_{ID}$, $v_O$ saturates: once $v_{ID}$ is large enough, $v_O$ independent of $v_{ID} \Rightarrow$ logic inverter!

Can do logic with this:

- Logic $0 \leq -V_{ID,\text{sat}}$, logic $1 \geq V_{ID,\text{sat}}$
- regenerative if $V_O(\text{swing}) > V_{ID,\text{sat}}$

- not used with MOSFETs
- but, used with Si BJT’s: *Emitter-Coupled Logic* (ECL)
- and GaAs FETs: *Source-Coupled FET Logic* (SCFL).
Common-emitter differential pair:

![Common-emitter differential pair diagram]

Large-signal characteristics:

![Large-signal characteristics graph]
Differential input voltage to saturate amplifier:

\[ v_{ID,sat} = v_{BE1} - v_{BE2} = \frac{kT}{q} \ln \frac{i_C1}{I_{S1}} - \frac{kT}{q} \ln \frac{i_C2}{I_{S2}} \]

It transistors are well matched: \( I_{S1} = I_{S2} \), and:

\[ v_{ID,sat} = \frac{kT}{q} \ln \frac{i_C1}{i_C2} \]

If we consider amplifier saturated when \( i_{C1} \approx 100 \ i_{C2} \), then:

\[ v_{ID,sat} \approx 120 \ mV \]

For MOSFET, \( v_{ID,sat} \approx 0.5 - 1 \ V \).

Since \( g_m \) of BJT is high and \( v_{ID,sat} \) is small, ECL is very fast logic!

At any one moment in time \( \tau_P(ECL) < \tau_P(CMOS) \). But two trade-offs:

- power dissipation penalty: \( P_{dis}(ECL) \gg P_{dis}(CMOS) \) (there is large DC power consumption in ECL),
- area and density penalty: BJT size \( \gg \) MOSFET size.
2. Wrap up of 6.012

- The amazing properties of Si

- two types of carriers: electrons and holes [although can make good electronic devices with just one, i.e. MESFET; but can’t do CMOS without two]

- carrier concentrations can be controlled over many orders of magnitude and in short length scales by addition of dopants

- carrier concentrations can be controlled electrostatically

- carriers are fast:
  - electrons can cross \( L = 0.1 \ \mu m \) in about:
    \[
    \tau = \frac{L}{v_e} = \frac{0.1 \ \mu m}{10^7 \ cm/s} = 1 \ ps
    \]
  - high current density:
    \[
    J_e = qnv_e = 1.6 \times 10^{-19} \ C \times 10^{17} \ cm^{-3} \times 10^7 \ cm/s
    = 1.6 \times 10^5 \ A/cm^2
    \]
    \Rightarrow \text{high current drivability to capacitance ratio}

- extraordinary physical and chemical properties
The amazing properties of Si MOSFET

- ideal properties of Si/SiO₂ interface: can drive surface all the way from accumulation to inversion [not possible in GaAs, for example]

- performance improves as MOSFET scales down in size; as \( L, \ W \downarrow \):
  - current:
    \[
    I_D = \frac{W}{2L} \mu C_{ox} (V_{GS} - V_T)^2 \]
    unchanged
  - capacitance:
    \[
    C_{gs} = WLC_{ox} \downarrow \downarrow
    \]
  - figure of merit for device switching delay:
    \[
    \frac{C_{gs}V_{DD}}{I_D} = L^2 \frac{2V_{DD}}{\mu (V_{GS} - V_T)^2} \downarrow \downarrow
    \]

- No gate current.
- \( V_T \) can be engineered.
- MOSFETs come in two types: NMOS and PMOS.
- Easy to integrate.
The amazing properties of Si CMOS

- Rail-to-rail logic: logic levels are 0 and $V_{DD}$.
- No power consumption while idling in any logic state.
- Scales well.

As $L$, $W \downarrow$:

- Power consumption (all dynamic):

$$P_{diss} = fC_LV_{DD}^2 \propto fWLC_{ox}V_{DD}^2 \downarrow \downarrow$$

- Propagation delay:

$$t_P \propto \frac{C_LV_{DD}}{W \mu C_{ox}(V_{DD} - V_T)^2} \downarrow \downarrow$$

- Logic density:

$$Density \propto \frac{1}{A} = \frac{1}{WL} \uparrow \uparrow$$
All this is enabling the *electronics revolution*:

- *exponential growth* in complexity and functionality of integrated circuits [Moore’s Law]
- *exponential decrease* in power per function and cost per function of integrated circuits
- profound penetration of IC technology into all aspects of human society
Circuit design lessons from 6.012:

1. Importance of optimum level of abstraction:

- device physics equations, \( i.e. \):
  \[
  I_D = \frac{W}{2L} \mu C_{ox} (V_{GS} - V_T)^2, \quad etc.
  \]

- device equivalent circuit models, \( i.e. \):

- device SPICE models, \( i.e. \):
2. Many considerations in circuit design:

- multiple performance specs:
  - in analog systems: gain, bandwidth, power consumption, swing, noise, etc.
  - in digital systems: propagation delay, power, ease of logic synthesis, noise, etc.

- need to be immune to temperature variations and device parameter variations (i.e.: differential amplifier)

- must choose suitable technology: CMOS, BJT, CBJT, BiCMOS, etc.

- must avoid costly components (i.e.: resistors, capacitors)

3. Trade-offs:

- gain-bandwidth trade-off in amplifiers (i.e.: Miller effect)

- performance-power trade-off (i.e.: delay in logic circuits, gain in amplifiers)

- performance-cost trade-off (cost=design complexity, Si area, more aggressive technology)

- accuracy-complexity trade-off in modeling
Exciting times ahead in Si IC technology:

- **analog electronics** (since \(\sim 50's\)): amplifiers, mixers, oscillators, DAC, ADC, etc.
- **digital electronics** (since \(\sim 60's\)): computers, microcontrollers, random logic, DSP
- **solid-state memory** (since \(\sim 60's\)): dynamic random-access memory, non-volatile RAM
- **energy conversion** (since \(\sim 70's\)): solar cells, photodetectors
- **power control** (since \(\sim 70's\)): "smart" power
- **communications** (since \(\sim 80's\)): VHF, UHF, RF front ends, modems, fiber-optic systems
- **sensing, imaging** (since \(\sim 80's\)): CCD cameras, CMOS cameras, many kinds of sensors
- **micro-electro-mechanical systems** (since \(\sim 90's\)): accelerometers, movable mirror displays
- **biochip** (from \(\sim 2000\)): DNA sequencing, \(\mu\)fluidics
- **vacuum microelectronics** (from \(\sim 2000?\)): field-emitter displays
- ???? (microreactors, microturbines, etc.)
Exciting times ahead in circuit design too:

- Numbers of transistors available outstrips ability to design by 3 to 1!
- Operational frequency of logic, analog, and communications circuits increasing very fast.
- Operational voltage shrinking quickly.
- New device technologies: GaAs HEMT, InP HBT, etc.
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