Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science

6.002 – Electronic Circuits

Final Exam
Spring 1995

- This exam has five problems. They are all of equal weight.
- A set of five answer sheets is attached to the back of this exam. Please put your name on your answer sheets and on your exam book. Also, please circle the name of your recitation instructor and the time of your recitation on the first answer sheet.
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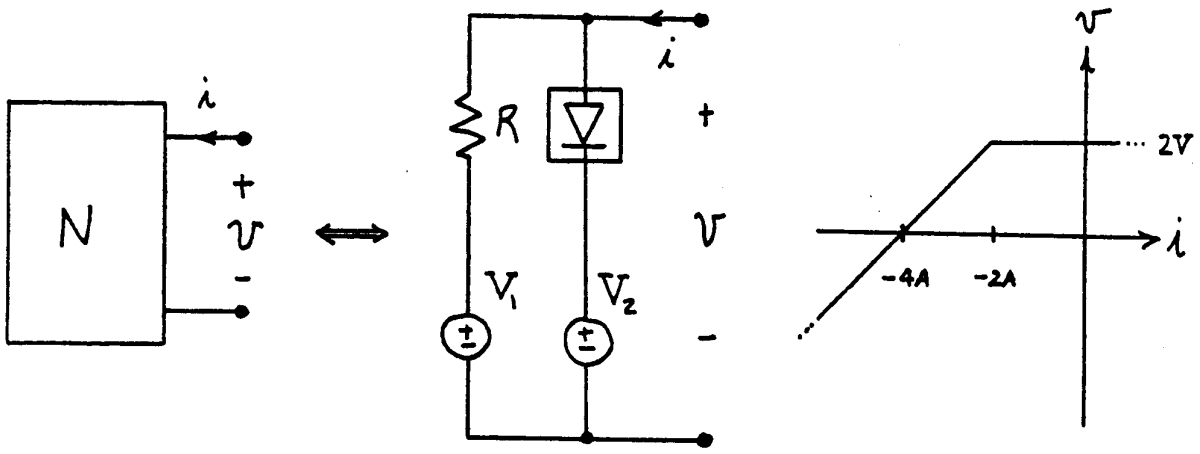
Problem 1

Shown below is a network which is constructed from one resistor, two voltage sources and one ideal diode. The network has a single port. Its i–v relation at that port is also given below.

(A) Determine the numerical values of R, V_1 and V_2.

(B) A 2-Ω resistor is connected across the network port as shown below. For this connection, determine the numerical values of i and v.

(C) A 1-F capacitor is connected across the network port through a switch as shown below. Prior to $t = 0$, the switch is open and the capacitor is discharged. At $t = 0$, the switch closes. For this connection, determine a numerical expression for $v(t)$ for $t \geq 0$.



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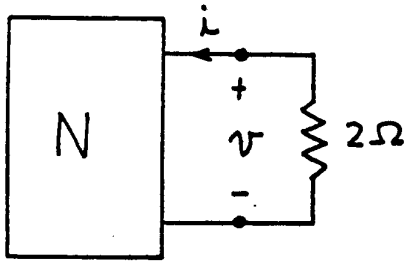

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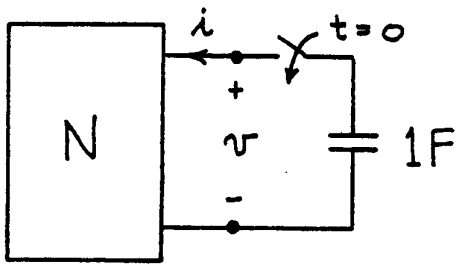


Problem 2

In the network shown below, the switch is initially open, and the inductor current i and capacitor voltage v are both initially zero. At $t = 0$, the switch closes, and remains closed for $0 \leq t \leq \pi\sqrt{LC}$. At $t = \pi\sqrt{LC}$, the switch opens. Note that the diode in the network is ideal.

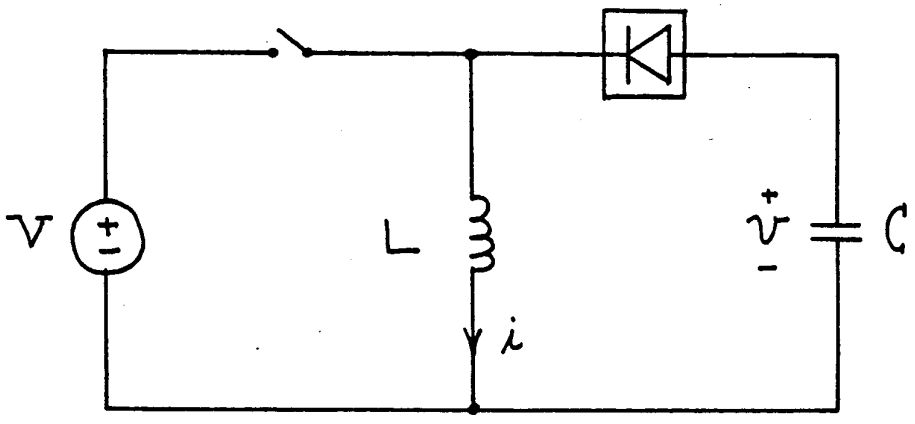
(A) Determine the inductor current i and the capacitor voltage v for the period of time during which the switch is closed, that is, for $0 \leq t \leq \pi\sqrt{LC}$.

(B) Determine the inductor current i and the capacitor voltage v after the switch opens. Do so for $\pi\sqrt{LC} \leq t \leq 2\pi\sqrt{LC}$.

(C) Graph $i(t)$ and $v(t)$ for $0 \leq t \leq 2\pi\sqrt{LC}$ on the axes provided on the answer sheet, and clearly label the graph. If the current and/or voltage is constant, then label the constant. Otherwise provide the appropriate functional dependence.

(D) Determine the energy stored in the inductor at $t = \pi\sqrt{LC}$ and at $t = 2\pi\sqrt{LC}$.

(E) At $t = 2\pi\sqrt{LC}$ the switch closes again. It remains closed until $t = 3\pi\sqrt{LC}$, at which time it opens. It remains open thereafter. Determine the inductor i current and capacitor voltage v at $t = 4\pi\sqrt{LC}$.



Problem 3

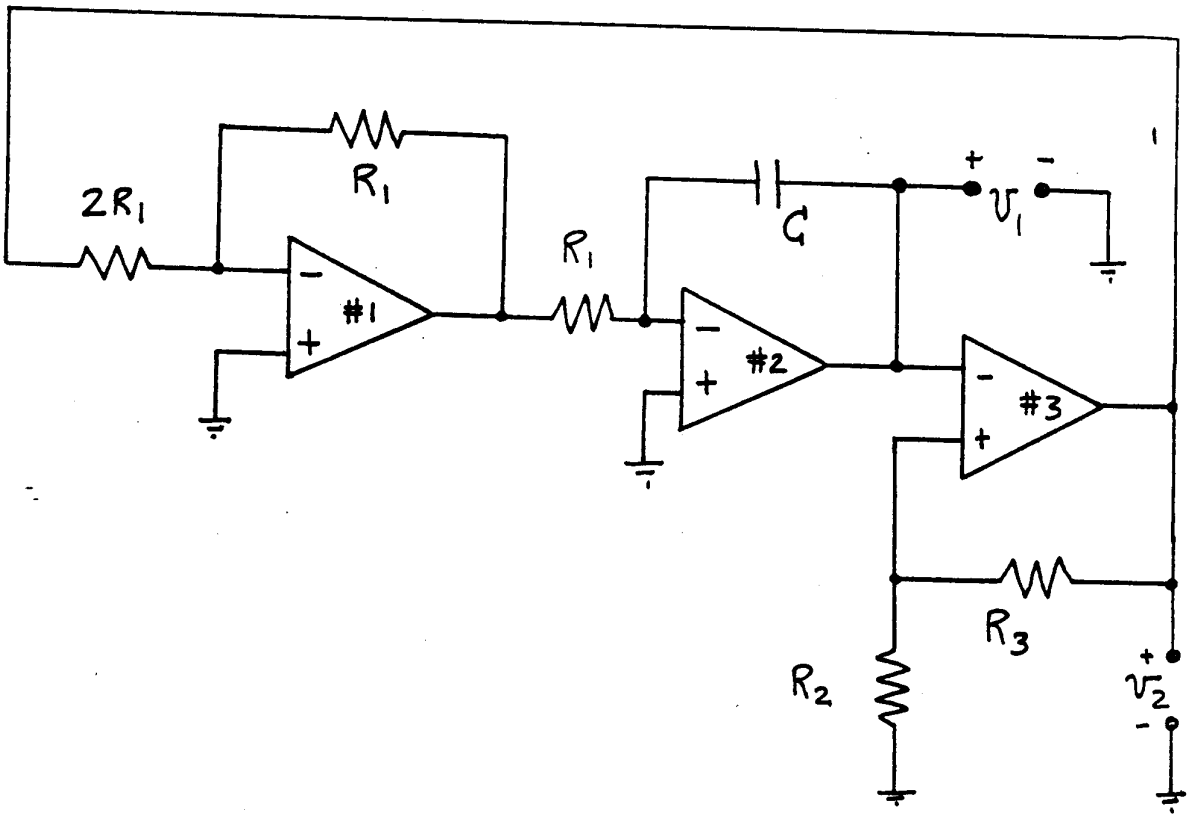
The circuit shown below is a free-running oscillator which produces a square-wave output at v_2. All op-amps in the oscillator are ideal except that they saturate at the power supply voltages $\pm V_S$. Note, however, that the power supply connections to the op-amps are not shown for simplicity.

(A) Consider Op-Amps #1 and #2. Determine v_1 as a function of v_2.

(B) Consider Op-Amp #3, which is always saturated. Determine the value of v_1 at which v_2 switches from $+V_S$ to $-V_S$, and the value of v_1 at which v_2 switches from $-V_S$ to $+V_S$.

(C) Graph v_1 and v_2 together over one period on the axes provided on the answer sheet, and clearly label the graph.

(D) Determine the period over which the oscillator oscillates.



Problem 4

The circuit shown below functions as a common-emitter amplifier. It is constructed with two identical NPN transistors, Q1 and Q2, arranged as a Darlington Pair. The large-signal and small-signal models for the NPN transistors are also shown below.

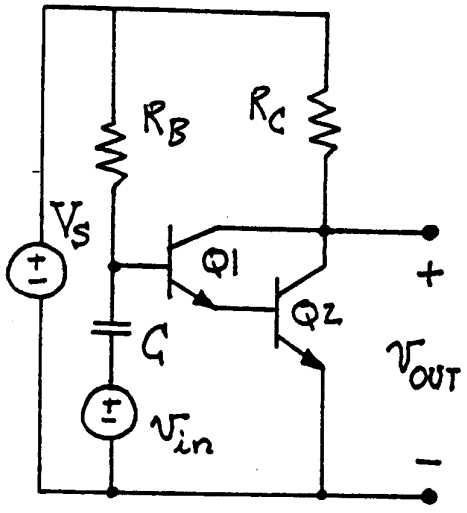
(A) Using the large-signal transistor model, determine the absolute maximum and minimum values of v_{OUT}.

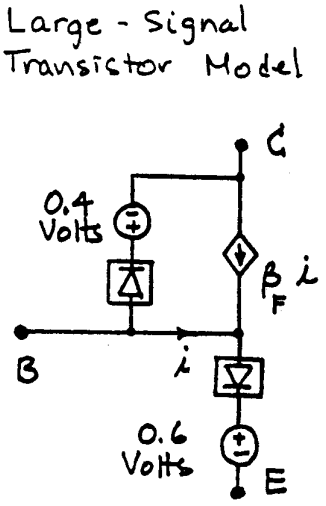
(B) In terms of V_S, R_C and the parameters of the large-signal transistor model, determine R_B such that v_{OUT} is biased midway between its maximum and minimum values. *Assume this biasing from here on.*

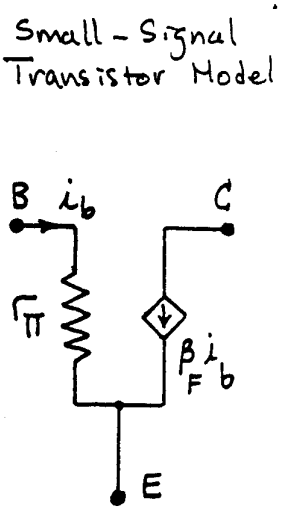
(C) In terms of V_S, R_C and the parameters of the large-signal transistor model, determine the bias current through R_C.

(D) Again in terms of V_S, R_C and the parameters of the large-signal transistor model, determine r_{π_1} and r_{π_2}. Note the definition of transistors Q1 and Q2; they may have different values of r_π.

(E) Let the small-signal input v_{in} take a step from 0 volts to v^*. In terms of C, R_B, R_C, r_{π_1}, r_{π_2} and β_F, determine v_{out}, the small-signal component of v_{OUT}.







Problem 5

In this problem the op-amp is ideal except for a finite voltage gain A, as shown in the op-amp model below. Additionally, the transistors are to be modeled with the large signal models shown below.

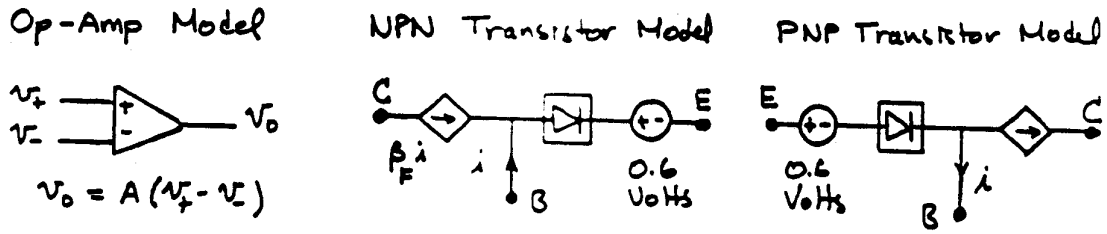
(A) Consider Circuit #1. Graph v_C as a function of v_B on the axes provided on the answer sheet, and clearly label the graph. Assume that $|v_B| < V_S$.

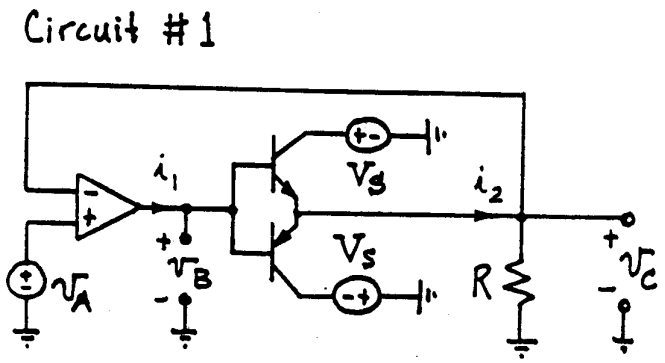
(B) Consider Circuit #1 again. Graph i_2 as a function of i_1 on the axes provided on the answer sheet, and clearly label the graph.

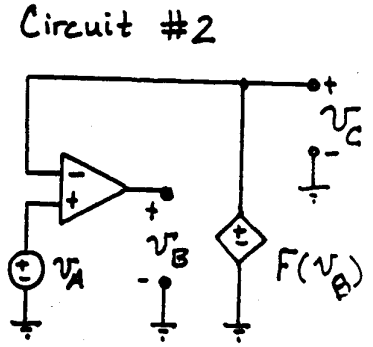
(C) Now consider Circuit #2. Derive an implicit expression which relates v_A and v_C. Assume that F is a known function.

(D) Consider Circuit #1 again. Combine the results from (A) and (C), and graph v_C as a function of v_A on the axes provided on the answer sheet. Clearly label the graph. Assume that $|v_A| < V_S$.

(E) In view of the previous results, what is the function of Circuit #1?







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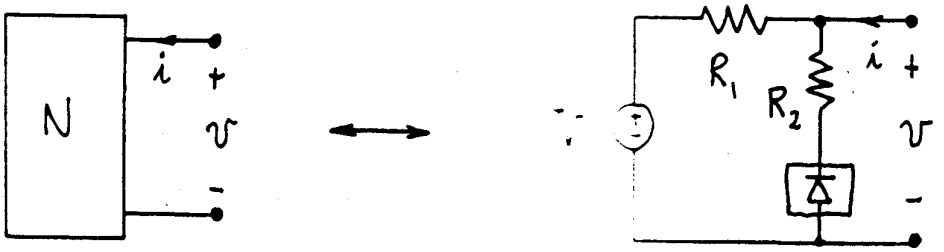
Problem 1

This problem is concerned with the network N shown below. The network has one port, and is constructed from one voltage source, two resistors, and one ideal diode. For Parts A and B of this problem, the voltage source is constant and positive; for Part C of this problem, it varies with time.

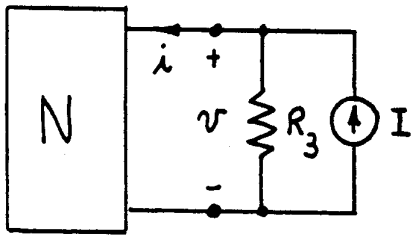
(A) Assume that V is constant and positive. Draw and clearly label the i–v relation for the network as measured at its port. As a minimum, label all intercepts and slopes.

(B) The network is connected to a Norton equivalent network, as shown below. Assume that both V and I are constant and positive. Determine i and v for this connection.

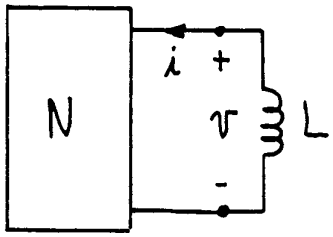
(C) Finally, the network is connected to an inductor, as shown below, and V is allowed to vary in time. Assume that $V(t)$ is the pulse shown below, and that $i(0) = 0$. Determine $i(t)$ for $t \geq 0$.

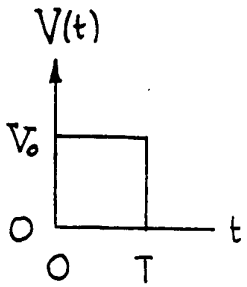


Part (B)



Part (C)





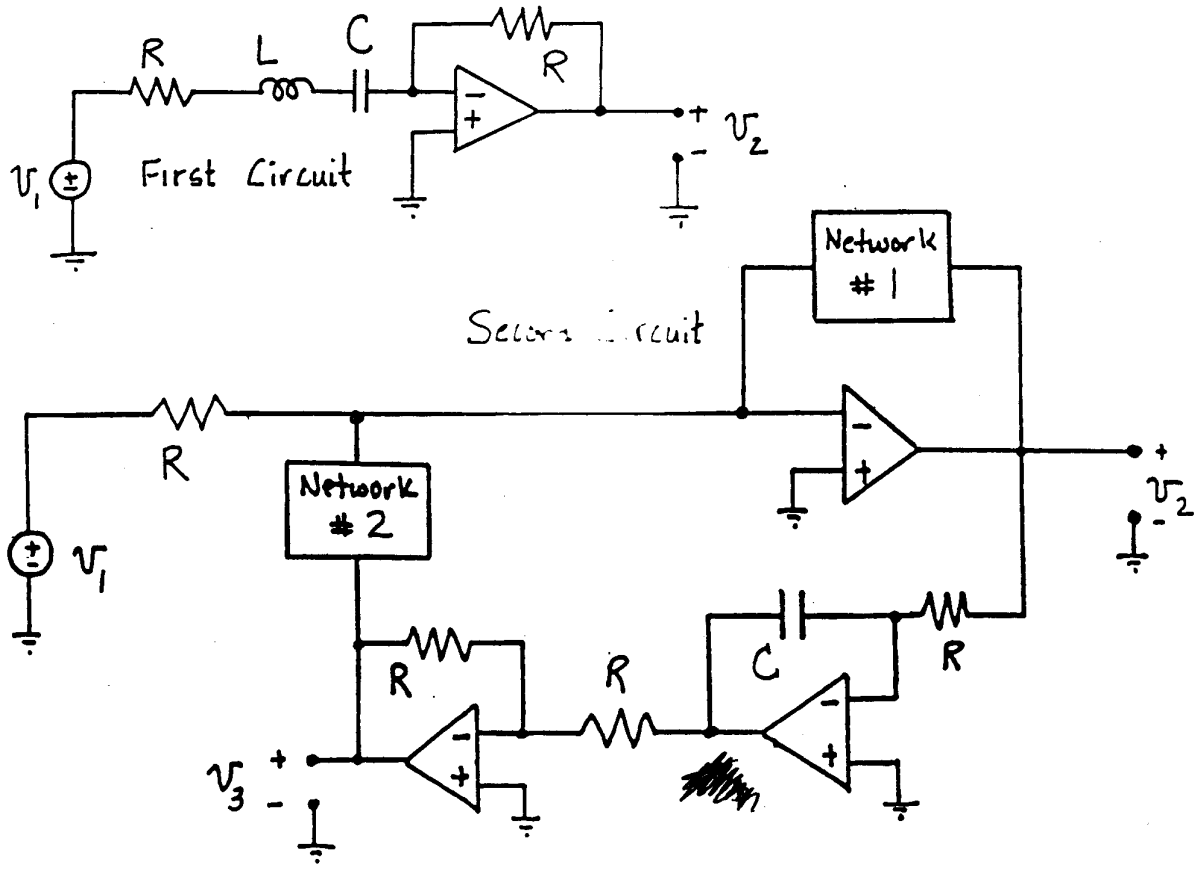
Problem 2

Two op-amp circuits are shown below. The first circuit contains an inductor, which is in general undesirable. The second circuit contains two unknown networks, which may each contain only resistors and capacitors. The unknown networks are to be designed so that the second circuit exhibits the same input-output behavior as the first. All op-amps are ideal.

(A) For the first circuit, find a differential equation which relates v_2 to v_1.

(B) For the second circuit, find v_3 in terms of v_2.

(C) Design the two unknown networks in the second circuit so that the differential equation relating v_2 to v_1 in the second circuit is the same equation found in Part A. Draw both networks, and clearly label the values of their components in terms of R, L, and C.



Problem 3

This problem is concerned with the three-stage circuit shown below. All diodes in the circuit must be modeled with exponential functions, as indicated below. The op-amps, however, are all ideal. Finally, assume that $|v_0| \gg v_T$ and that $|v_0| \gg RI_S$.

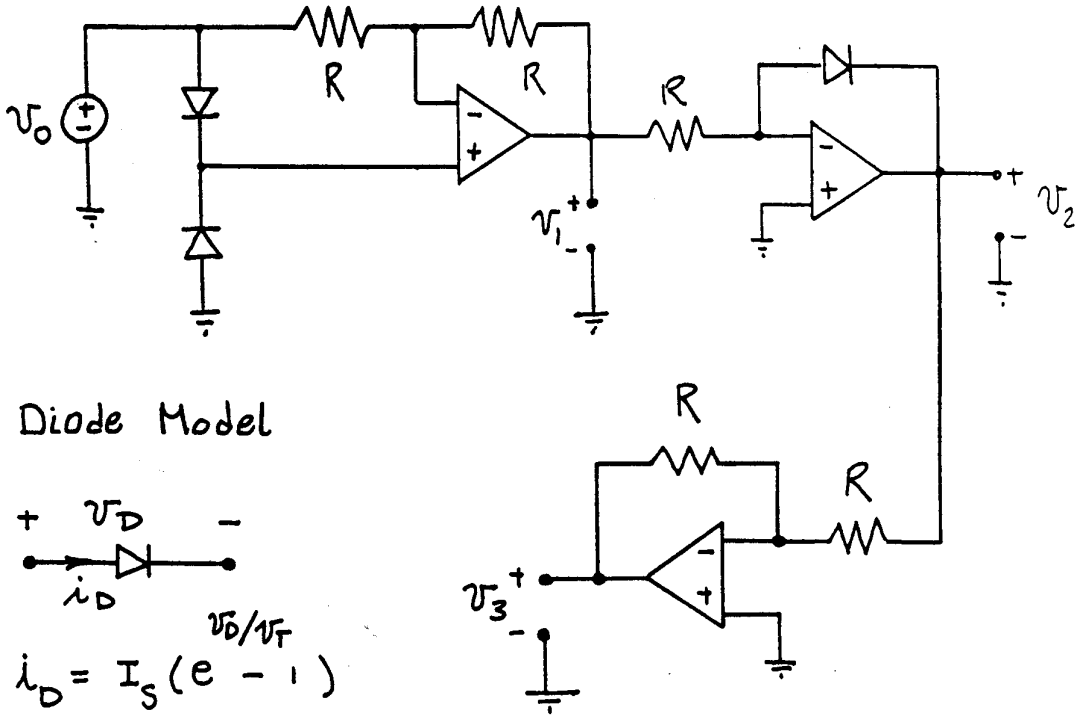
(A) Determine v_1 as a function of v_0.

(B) Determine v_2 as a function of v_1.

(C) Determine v_3 as a function of v_2.

(D) Combine the prior results to determine v_3 as a function of v_0.

(E) What function does the circuit perform?



Diode Model

$$i_D = I_S(e^{v_D/v_T} - 1)$$

Problem 4

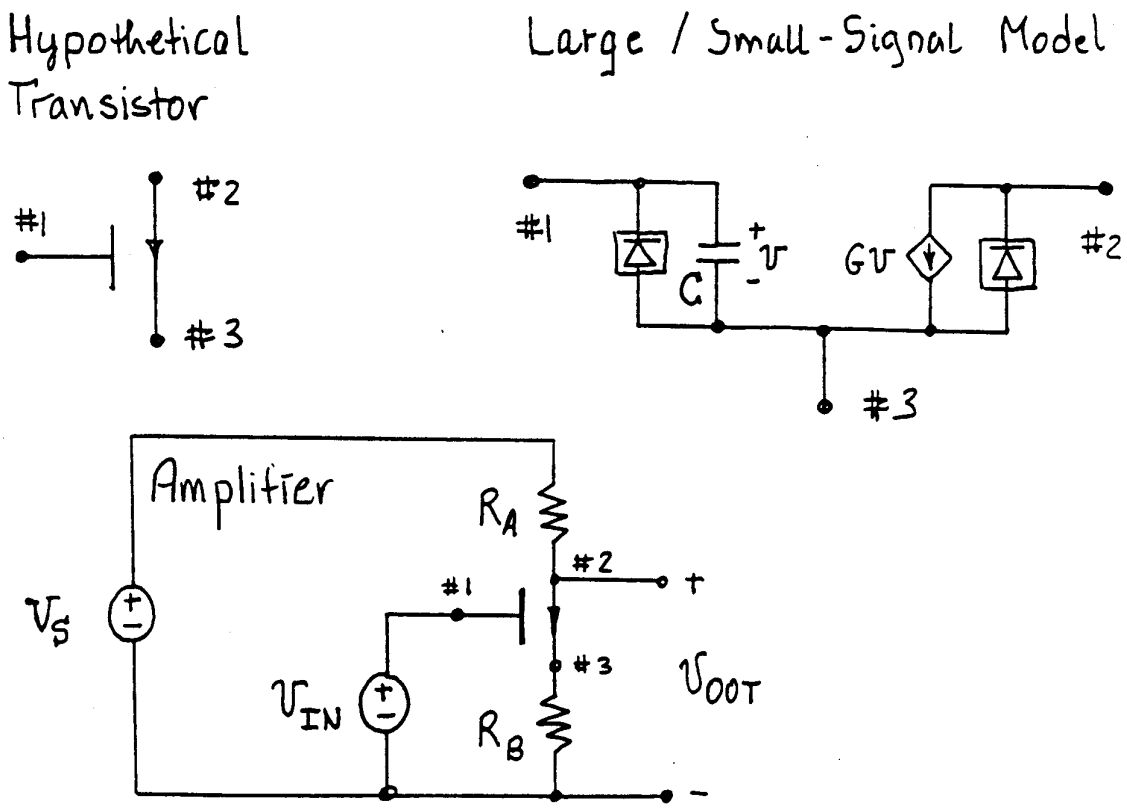
A hypothetical three-terminal transistor is defined below. Its large-signal and small-signal models are identical, and the joint model is also given below. Note that the diodes in the model are ideal. Finally, the transistor is used in the amplifier shown below.

(A) Determine the maximum and minimum values for v_{OUT}.

(B) For this part only, assume that $C = 0$. Draw and clearly label v_{OUT} as a function of v_{IN}. As a minimum, label all intercepts and slopes.

(C) Determine v_{OUT} for $v_{IN} = V_B + V_S \cos \omega t$, where V_B, V_S and ω are constants. Assume that v_{OUT} never reaches the extreme values found in Part A.

(D) Using reasonable approximations, determine the range of ω over which the answer to Part C is equivalent to the answer to Part B.



Problem 5

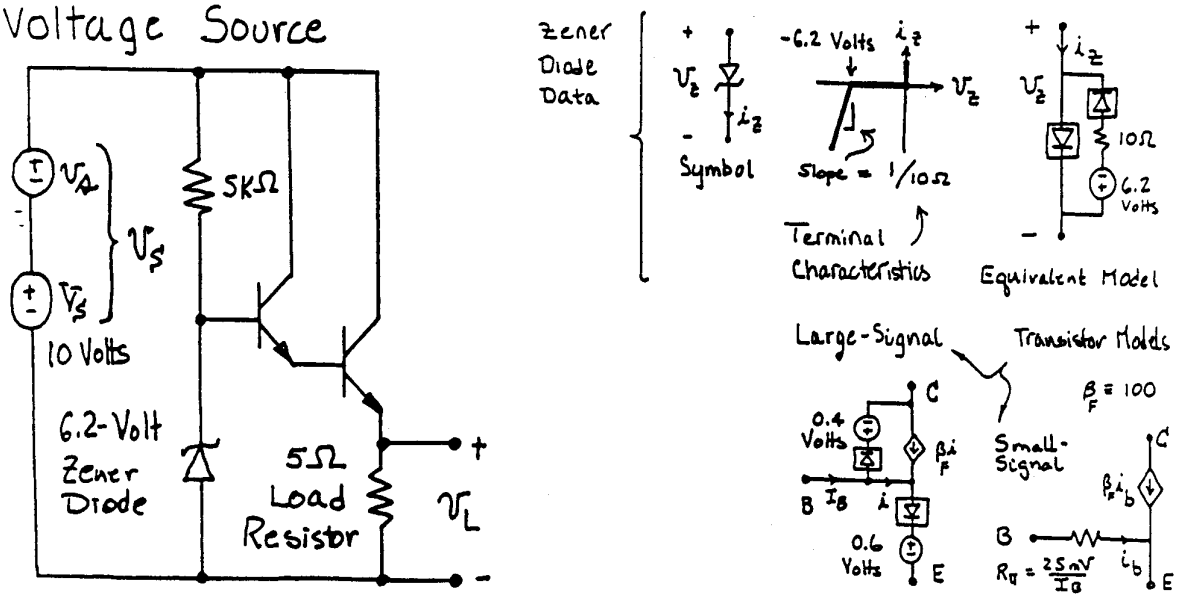
A zener diode, which acts as a nearly perfect voltage reference when reverse biased, can be combined with two transistors, a resistor and a noisy voltage supply to form a good voltage source as shown below. Here, the 5-Ω resistor models the load for the voltage source, and the Darlington transistor configuration is used to provide a high-current output. The terminal characteristics and equivalent model of the zener diode, and the large-signal and small-signal transistor models are also shown below.

V_S and v_s are the large-signal and small-signal components of the supply voltage v_S, respectively. V_L and v_l are the large-signal and small-signal components of the load voltage v_L, respectively. The noise in the voltage supply is modeled by v_s which satisfies $v_s \ll V_S$, and is in turn responsible for the presence of v_l within v_L.

(A) Assume that $v_s = 0$. Using the large-signal transistor model, determine V_L; use reasonable engineering approximations.

(B) Now assume that $v_s \neq 0$. Using the small-signal transistor model, determine the small-signal model for the overall voltage source and load from which v_l can be found as a function of v_s.

(C) Using the overall small-signal model from Part B, find the ratio v_l/v_s; use reasonable approximations.



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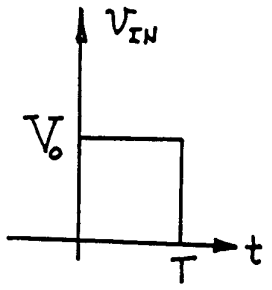
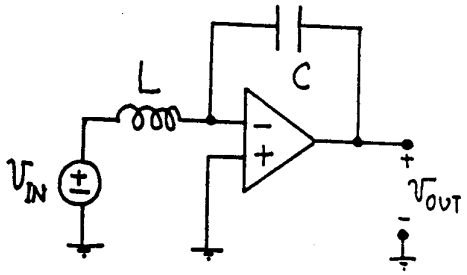
Problem 1

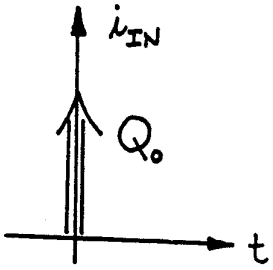
For the following four networks, neatly sketch and clearly label v_{OUT} for $t \geq 0^+$ given the specific input shown for each network. All network states are zero at $t = 0^-$, and all diodes and op-amps are ideal. For those portions of v_{OUT} that are not constant, provide an expression for v_{OUT} as part of your sketch.

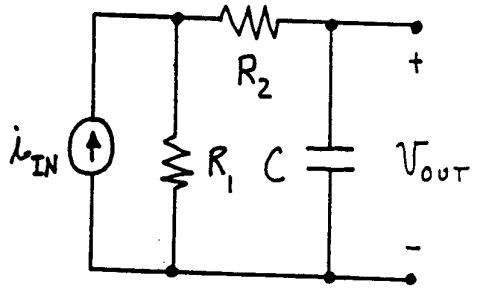
Network #1



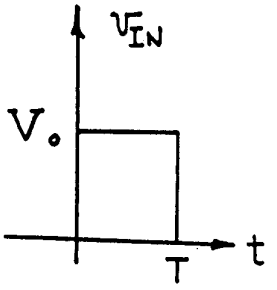


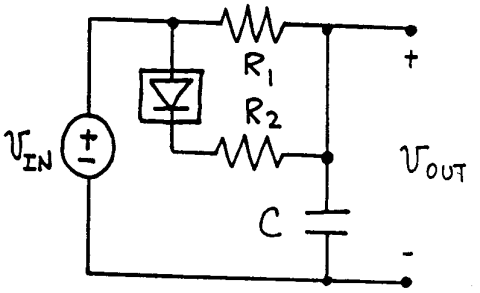
Network #2



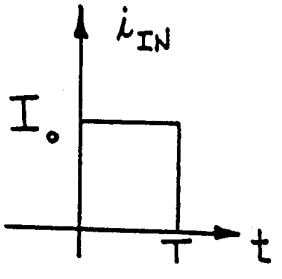


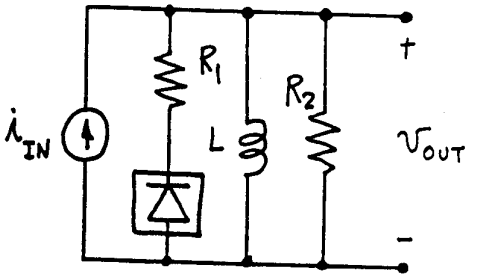
Network #3





Network #4





Problem 2

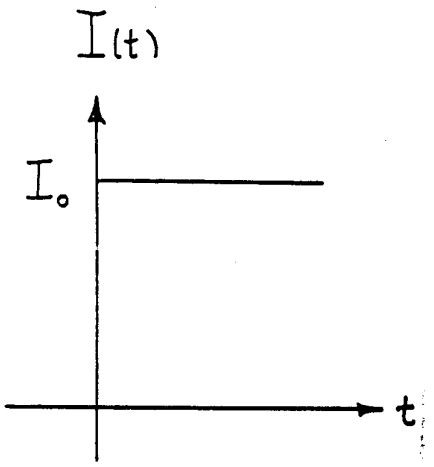
This problem is concerned with the three networks shown below. Network #2 is identical to network #1 except for the addition of an ideal diode. Network #3 is identical to Network #2 except for the addition of a switch which is initially closed. All network states are zero at $t = 0$, and all networks are driven by the same current step.

(A) For Network #1, determine $i(t)$ and $v(t)$ for $t \geq 0$.

(B) For Network #1, neatly sketch and clearly label $i(t)$ and $v(t)$ for $0 \leq t \leq 4\pi\sqrt{LC}$.

(C) For Network #2, neatly sketch and clearly label $i(t)$ and $v(t)$ for $0 \leq t \leq 4\pi\sqrt{LC}$.

(D) Consider Network #3. At $t = 2\pi\sqrt{LC}$ the switch opens, and then at $t = 3\pi\sqrt{LC}$ the switch closes. Determine $i(t)$ and $v(t)$ evaluated at $t = 4\pi\sqrt{LC}$.



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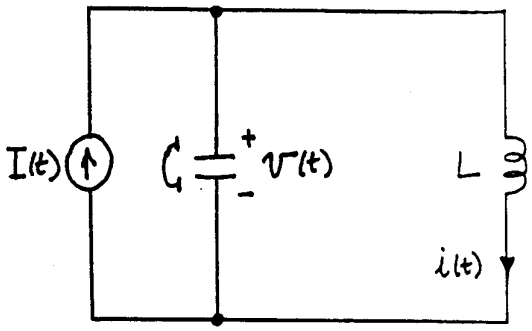
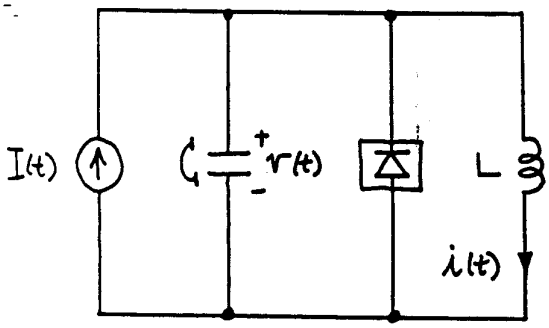
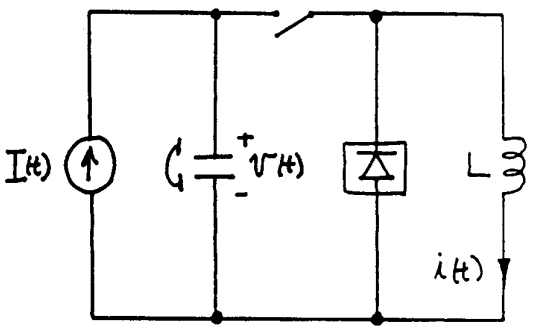


Network #2



Network #3



Problem 3

This problem is concerned with the multi-stage circuit shown below. All diodes and op-amps in the circuit are ideal except that the op-amps are powered by finite voltage supplies of value $\pm V$; note that the voltage supplies are not explicitly shown. Assume, however, that no op-amp saturates except for the one which drives the light bulb.

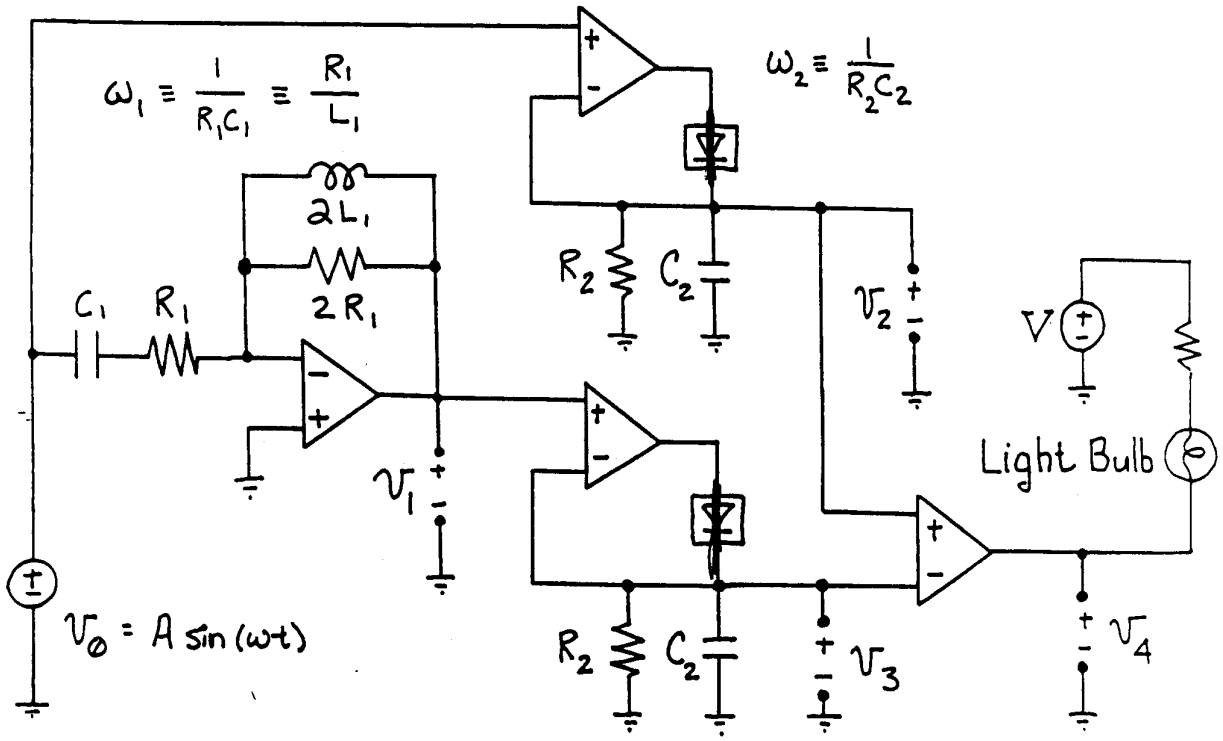
(A) Determine the magnitude of $v_1(t)$ given $v_0(t)$ for arbitrary ω, and use the definition of ω_1 given below to simplify the result. Assume sinusoidal steady-state operation.

(B) Note the definition of ω_2 given below. Neatly sketch $v_2(t)$ on top of $v_0(t)$ for $\omega \approx 10\omega_2$; note that $v_0(t)$ is already sketched on the answer sheet attached to the back of this exam. Assume steady-state operation.

(C) Assuming that $\omega \gg 10\omega_2$, determine $v_2(t)$ given $v_0(t)$; use reasonable engineering approximations. Note that a similar relation exists between $v_3(t)$ and $v_1(t)$.

(D) Assuming that the output of the op-amp which drives the light bulb is saturated at $v_4(t) = \pm V$, determine $v_4(t)$ in terms of $v_2(t)$ and $v_3(t)$.

(E) The light bulb will light whenever $v_4(t) = -V$. Determine conditions on A and ω such that the light bulb will light. Assume that $\omega_1 \gg 10\omega_2$.



Problem 4

This problem analyses the large-signal behavior of the circuit shown below. The circuit contains one diode and one transistor, which should be modeled with the large-signal models given below. The circuit is driven by a voltage source, and in turn drives a resistor load.

(A) Assume that the diode is on, and the that transistor operates in its forward active region. Determine v_{OUT} as a function of v_{IN}.

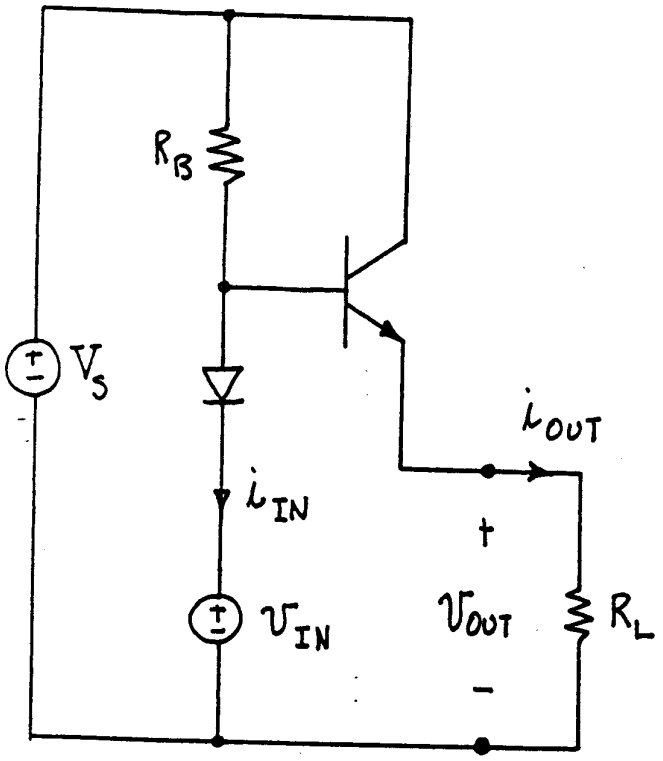
(B) Assume that the diode is on, and that the transistor operates in its forward active region. Determine i_{OUT} as a function of v_{IN}.

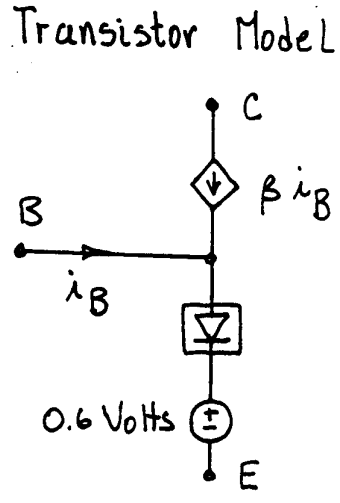
(C) Assume that the diode is on, and that the transistor operates in its forward active region. Determine i_{IN} as a function of v_{IN}.

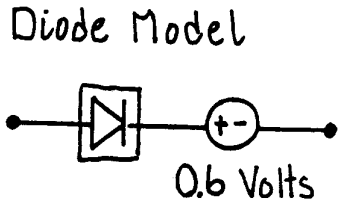
(D) Determine the range of v_{IN} over which the diode is off.

(E) Determine the range of v_{IN} over which the transistor is cut off.

(F) Sketch and clearly label v_{OUT} as a function of v_{IN} over a range of v_{IN} that includes results from Parts A, D and E.







Problem 5

This problem is concerned with the one-transistor amplifier shown below which is driven by a sinusoidal input voltage. Both a large-signal model and a small-signal model for the transistor are also given below. Note that, for algebraic simplicity, the base-collector and base-emitter diodes in the transistor are modeled as ideal in the large signal model.

Answer all parts of this problem in terms of R_1, L, C_1, V_S, β, v_T, A and ω, except as noted in Parts B and F.

(A) Using the large-signal transistor model, determine R_2 such that v_{OUT} is biased at $V_S/2$.

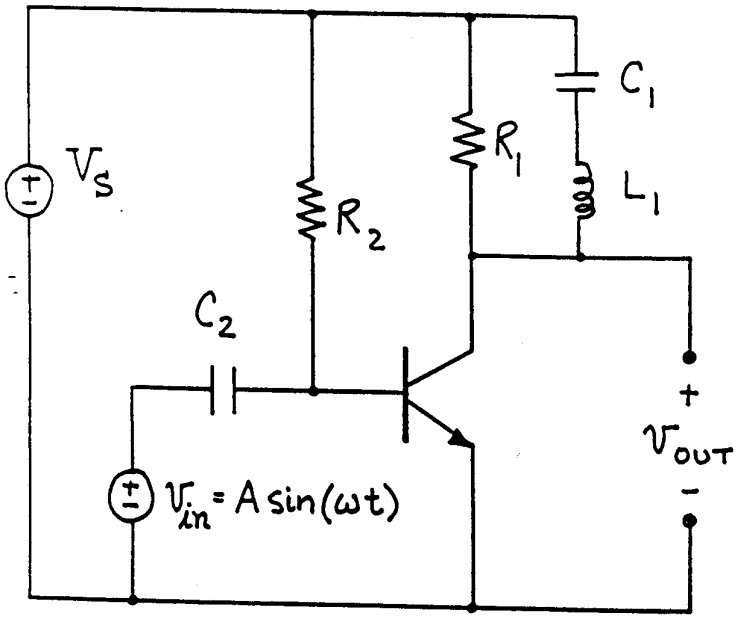
(B) Draw a small-signal model for the amplifier that can be used to find v_{out}, the small-signal component of v_{OUT}, in response to the small-signal input v_{in}. The model should explicitly include r_π.

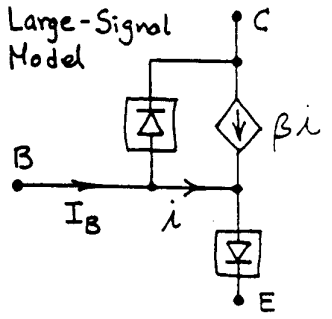
(C) Determine r_π in the small-signal model.

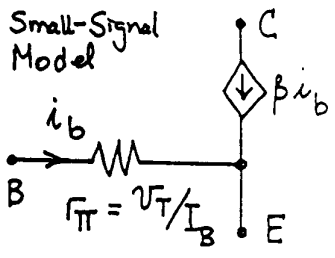
(D) For a given ω, determine the range of values for C_2 such that C_2 may be treated as a short circuit; use reasonable engineering approximations.

(E) Assume that C_2 may be treated as a short circuit, and that the amplifier operates in sinusoidal steady state so that $v_{out}(t) = B\sin(\omega t + \phi)$. Determine B and ϕ.

(F) Determine the maximum value for A such that the transistor will not saturate for any ω. This value should not depend on ω.







Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science

6.002 – Electronic Circuits

Final Exam
Fall 1998

- This exam has five problems. They all carry equal weight.
- A set of five answer sheets is provided with this exam. Please put your name on your answer sheets and on your exam book. Also, please circle the name of your recitation instructor and the time of your recitation on the cover page to the answer sheets.
- Do all of your work in your exam book, and then record your answers on your answer sheets. Hand in both your exam book and your answer sheets at the end of the exam period. You may keep the exam questions.
- You are welcome to use one double-sided page of notes while taking this exam. Good luck!

- Final grades in 6.002 will not be given out by phone or by e-mail. Rather, they should be available through WEBSIS by December 17. You may review and/or take back your final exam at the beginning of IAP in January 1999.

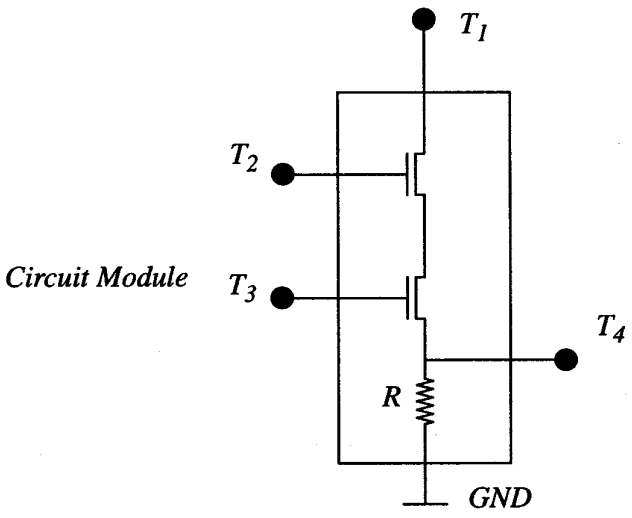
Problem 1

(A) Let A and B be logical variables that can take on the values of 0 or 1. Further, let C be a logic variable that is 1 if the numerical value of A is greater than or equal to the numerical value of B, and 0 otherwise. Write a truth table and a Boolean expression for C in terms of A and B.

(B) Consider the circuit module shown below comprising a pair of series connected n-channel MOSFETs and a resistor. The module has four terminals T1, T2, T3 and T4. Using one or more circuit modules, implement the Boolean function $X = \bar{A} \cdot B + \bar{B} \cdot A$. The implementation must clearly show how the circuit modules are interconnected, how A and B, and the power supply are connected to the implementation, and at which terminal the output X appears.

In developing the implementation make the following four assumptions. First, assume that the ground potential is 0 V and that a 5-V power supply is available. Second, assume that a logical 1 is represented by the voltage of 5 V, and that a logical 0 is represented by the voltage of 0 V. Third, assume that A and B are both available in their true and complementary forms. Fourth, assume that the MOSFETs behave as ideal switches that turn on when a logical 1 is applied to the gate and turn off when a logical 0 is applied.

(C) Now, model the MOSFET using the switch-resistor model, and let the on-state resistance of each MOSFET be $R_{ON} \equiv R_n L/W$. Assuming that all MOSFETs have the same size, derive a constraint for the value of L/W so that the circuit found in Part (B) provides a valid high output voltage given that the high output voltage threshold is specified by $V_{OH} = \tilde{V}_{OH}$. In other words, the constraint must guarantee that the output voltage of the circuit will exceed $\tilde{V}_{OH}$ when the output corresponds to a logical 1. Specify the constraint in terms of R, R_n, $\tilde{V}_{OH}$, and the 5-V power supply voltage.



Problem 2

The circuit shown below delivers a nearly constant current to its load despite the fact that the power supply is noisy. The noise is modeled by the small signal v_s superimposed on the constant supply voltage V_S. Thus, V_S and v_s are the large-signal and small-signal components of the total power supply voltage v_S, respectively. I_L and i_l are the large-signal and small-signal components of the load current i_L, respectively. The noise v_s in the power supply voltage satisfies $v_s \ll V_S$, and is responsible for the presence of i_l in i_L.

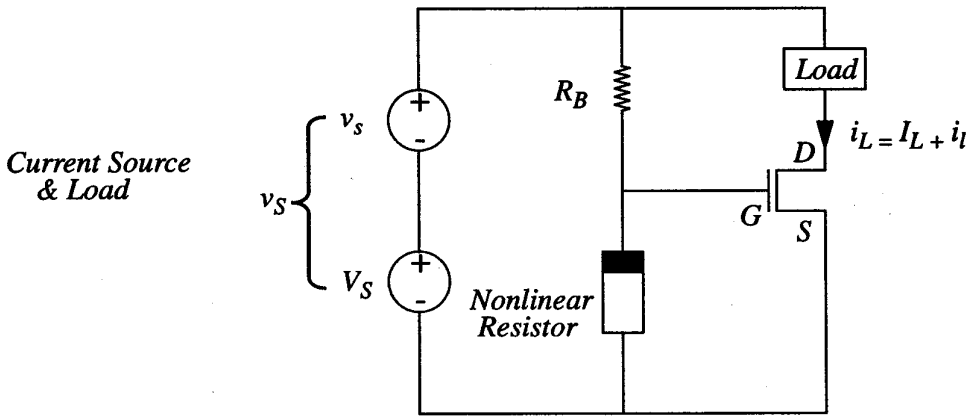
The current source contains a MOSFET which operates in its saturation region such that $i_{DS} = \frac{K}{2}(v_{GS} - v_T)^2$. The current source also contains a nonlinear resistor whose terminal characteristics are described graphically below. Assume that $V_S > V_N > v_T$.

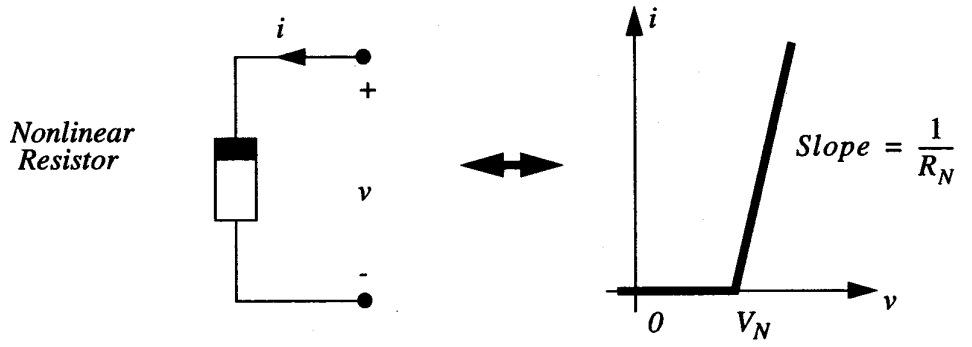
(A) Assume $v_s = 0$. Determine V_{GS}, the large-signal component of v_{GS}, in terms of R_B, R_N, V_N and V_S.

(B) Following the result of Part (A), determine I_L in terms of R_B, R_N, V_N, V_S, K and v_T.

(C) Now assume that $v_s \neq 0$. Draw a small-signal circuit model for the combined circuit comprising the power supply, current source and load, with which i_l can be found from v_s. Clearly label the value of each component in the circuit model.

(D) Using the small-signal model from Part (C), determine the ratio i_l/v_s.





Problem 3

This problem examines the operation of the amplifier circuit shown below which is constructed with a non-ideal op-amp. The op-amp is not ideal because it exhibits internal dynamics and finite gain. A model for the op-amp is also shown below.

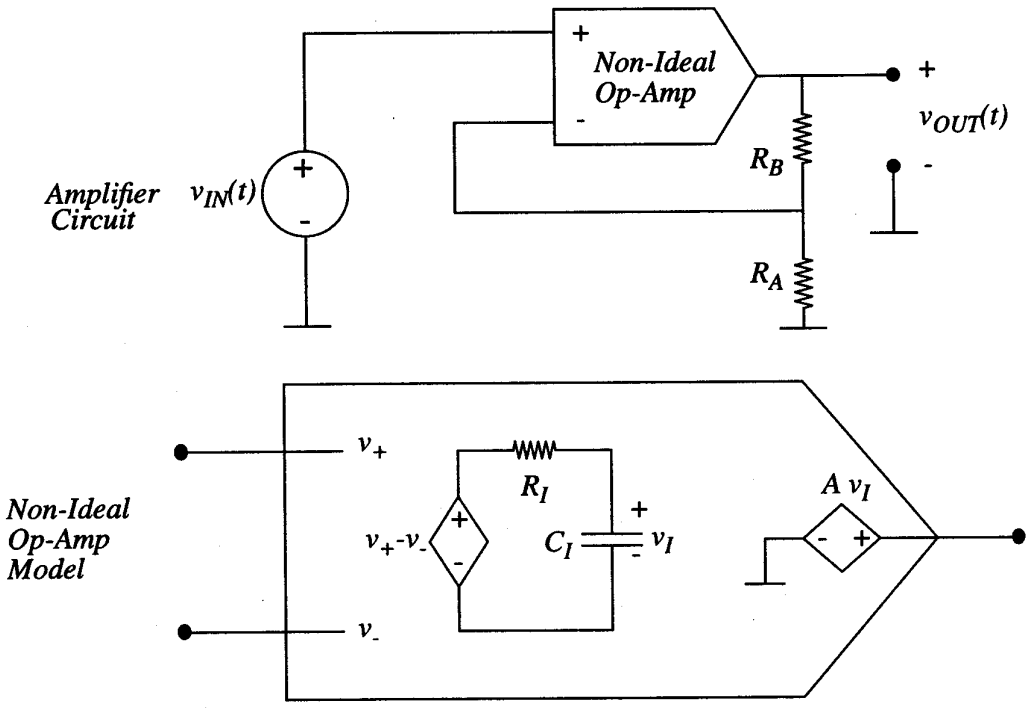
(A) For the amplifier circuit, derive the differential equation that relates $v_{\text{OUT}}(t)$ to $v_{\text{IN}}(t)$.

(B) Let $R_{\text{I}}C_{\text{I}} \to 0$ and $A \to \infty$ so that the op-amp becomes ideal. In this case, determine the ideal amplifier circuit gain G defined according to $G \equiv v_{\text{OUT}}(t)/v_{\text{IN}}(t)$.

(C) Now consider the non-ideal op-amp, but with $A \gg G$. Given that $v_{\text{IN}}(t)$ steps to V_{I} at $t = 0$, determine $v_{\text{OUT}}(t)$ for $t \geq 0$, in terms of A, G, R_{I}, C_{I}, and V_{I}. Assume that $v_{\text{OUT}}(t) = v_{\text{IN}}(t) = 0$ before the step.

(D) Using the step response found in Part (C), determine the rise time T of the amplifier defined such that $v_{\text{OUT}}(T) = (1 - e^{-1})v_{\text{OUT}}(\infty)$.

(E) Does the rise time T increase, decrease or remain unchanged if the ideal gain G is increased?



Problem 4

In this problem, a low-voltage sinusoidal source is coupled to a resistive load through an inductor-capacitor network as shown below. The role of the network is to boost the voltage at the load.

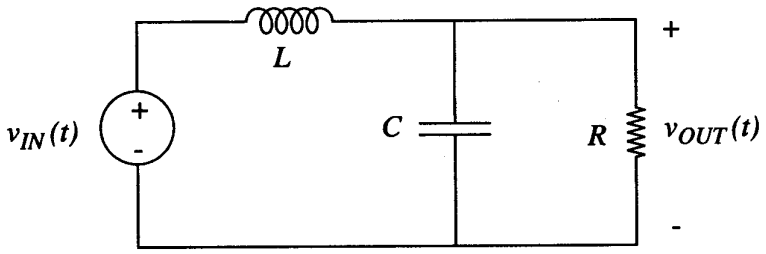
(A) Derive the differential equation that relates $v_{\mathrm{OUT}}(t)$ to $v_{\mathrm{IN}}(t)$.

(B) Assume that the circuit operates in sinusoidal steady state with $v_{\mathrm{IN}}(t) = V_{\mathrm{I}} \cos(\omega t)$. Let $v_{\mathrm{OUT}}(t)$ take the form $v_{\mathrm{OUT}} = V_{\mathrm{O}} \cos(\omega t + \phi)$. Determine $N \equiv V_{\mathrm{O}}/V_{\mathrm{I}}$ and ϕ.

(C) For a given L and ω, determine the value of C which maximizes N, and for this value of C, determine N.

(D) Suppose that $v_{\mathrm{IN}}(t)$ is abruptly set to zero in an attempt to remove quickly the voltage at the load. In this case, the amplitude of the load voltage will decay in proportion to $e^{-t/\tau}$. Assuming that C is chosen to maximize N following the result from Part (C), determine τ in terms of N and ω.

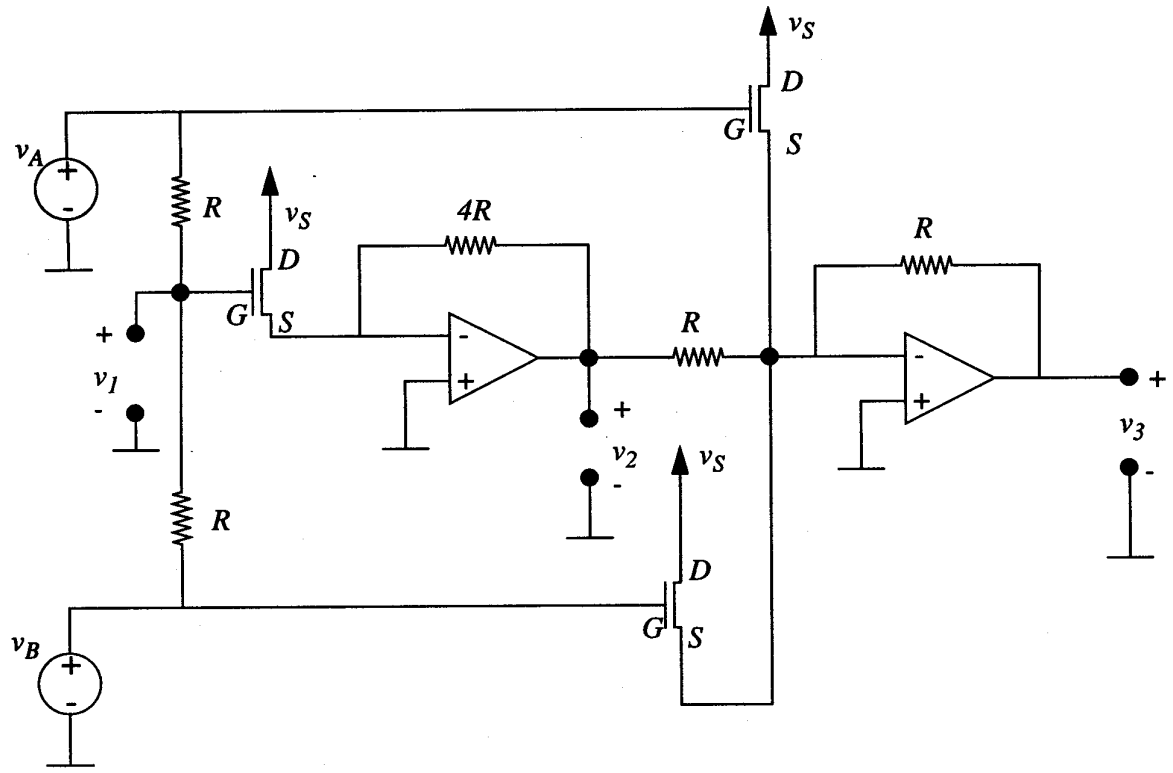
(E) In view of the results of Parts (C) and (D), what is the disadvantage of using an inductor-capacitor network to boost the voltage which excites the load?



Problem 5

This problem studies the multi-stage circuit shown below. Assume that all op-amps in the circuit are ideal. Further, assume the each MOSFET operates in saturation, and that, for simplicity, $v_T = 0$ for each MOSFET. Thus, for each MOSFET, $I_{DS} = \frac{K}{2} v_{GS}^2$.

(A) Determine v_1 in terms of v_A and v_B.

(B) Determine v_2 in terms of v_1.

(C) Determine v_3 in terms of v_A and v_B.