Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science

6.002 – Electronic Circuits
Spring 2000

Final Exam

- Please put your name in the space provided below, and circle the name of your recitation instructor and the time of your recitation.
- Do all of your work on the pages contained within this exam. In particular, do your work for each question within the boundaries of the question, or on the back side of the page preceding the question. When finished, put your answer to each question in the corresponding answer box at the bottom of the page on which the question in written.
- You may use one double-sided page of notes while taking this exam.
- Final grades in 6.002 will not be given out by phone or by e-mail. Rather, they should be available through WEBSIS by May 22. You may review and take back your final exam on or after May 22.
- Good luck!

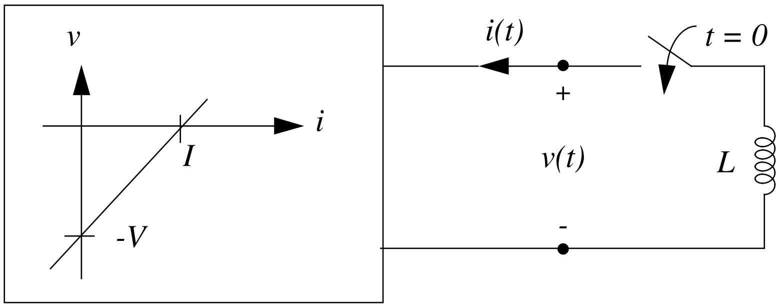
Name: ____

Instructor:	Freidberg		Chandrakasan		Cooke		Weiss	
Time:	9	10	10	11	11	12	1	2

Problem 1 – 20%

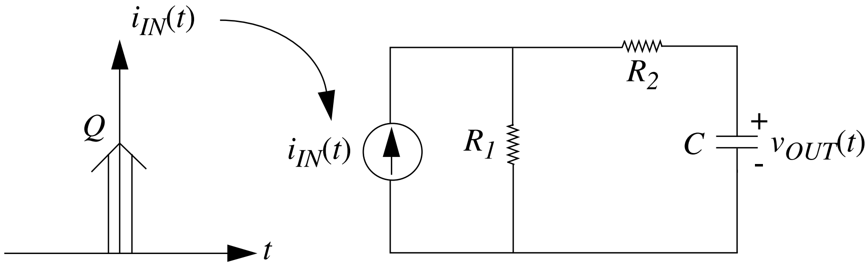
This problem involves determining the transient responses of the three circuits shown below. For each circuit, determine the response analytically, and then graph the response on the axis provided. Clearly label each graph.

(1A) The terminal characteristics of part of this circuit are described graphically. At $t = 0$, the switch closes. Determine $i(t)$ for $t \geq 0$.



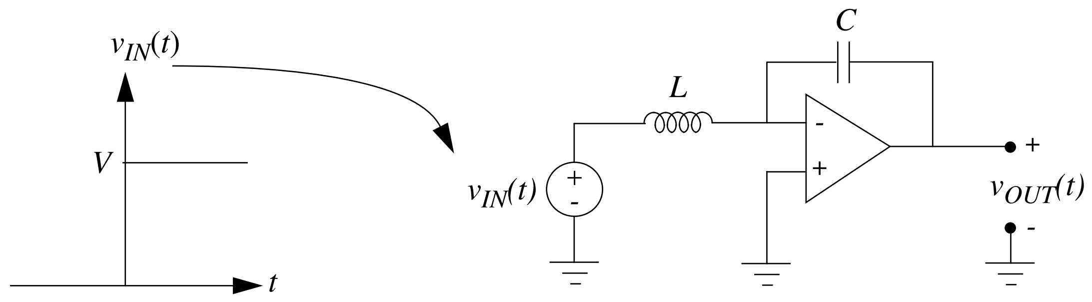
$i(t) =$

(1B) At $t = 0$, the current source provides an impulse of area Q. Just prior to $t = 0$, the capacitor voltage is $v_{\mathrm{OUT}}(0^-) = V$. Determine $v_{\mathrm{OUT}}(t)$ for $t \geq 0^+$.



$v_{\mathrm{OUT}}(t) =$

(1C) This circuit is initially at rest. At $t = 0$, the voltage source takes a step. Assume that the op-amp is ideal. Determine $v_{\mathrm{OUT}}(t)$ for $t \geq 0$.

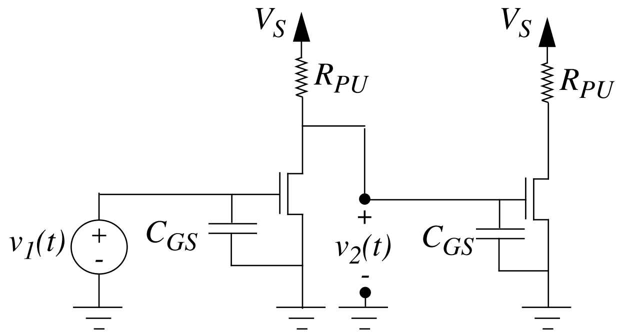


$v_{\mathrm{OUT}}(t) =$

Problem 2 – 20 %

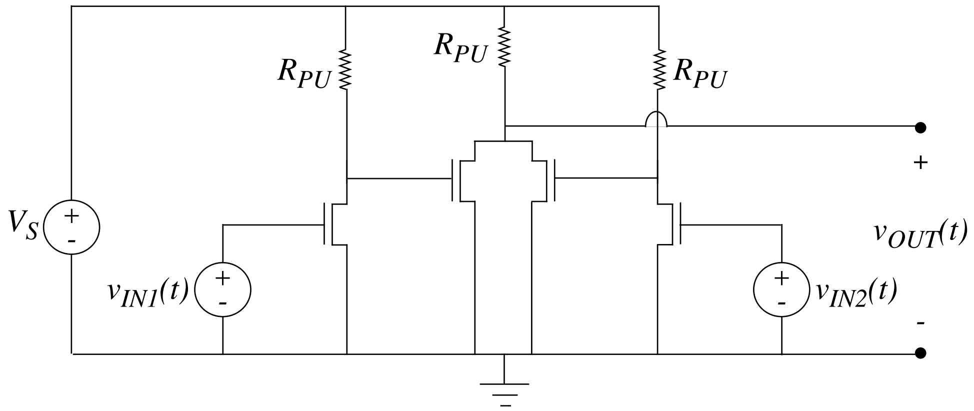
This problem focuses on NMOS digital logic circuits built with MOSFETs, and pull-up resistors having resistance R_{PU}. Model each MOSFET with a switch-resistor model having a threshold voltage V_{T} and on-state resistance R_{ON}. Also include the gate-to-source capacitance C_{GS} in the model. Finally, let $V_{\mathrm{T}} \equiv V_{\mathrm{S}}/2$ and assume that $R_{\mathrm{ON}} \ll R_{\mathrm{PU}}$.

(2A) Consider the cascaded inverters shown below. Determine the fall time T_{F} and the rise time T_{R} of the first inverter in terms of the MOSFET model and circuit parameters. The fall time is defined here as the delay from the time that $v_1(t)$ rises past V_{T} to the time $v_2(t)$ falls past V_{T}; the rise time is the delay from the time that $v_1(t)$ falls past V_{T} to the time $v_2(t)$ rises past V_{T}. Assume that the circuit is at rest before $v_1(t)$ passes V_{T} in both cases, and make reasonable approximations based on the inequality $R_{\mathrm{ON}} \ll R_{\mathrm{PU}}$.



$T_{\mathrm{F}} =$	$T_{\mathrm{R}} =$

(2B) Assuming that the logic level 0 is represented by a voltage below V_T, and that a logic level 1 is represented by a voltage above V_T, determine the truth table for the circuit shown below that describes its operation at rest. Also, design an alternative NMOS circuit implementation that uses fewer MOSFETs and fewer resistors.



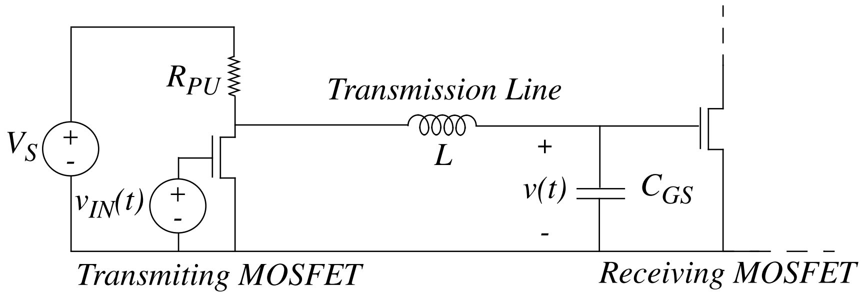
Truth Table		
IN1	IN2	OUT
0	0	
0	1	
1	0	
1	1	

Implementation:

(2C) Consider the circuit from Part (B) at rest with $v_{\mathrm{IN1}} < V_{\mathrm{T}}$ and $v_{\mathrm{IN2}} > V_{\mathrm{T}}$ prior to $t = 0$. At $t = 0$, v_{IN1} rises above V_{T} while v_{IN2} simultaneously falls below V_{T}. For these inputs, sketch and clearly label the time dependence of $v_{\mathrm{OUT}}(t)$ on the axis provided below from slightly before $t = 0$ until slightly after $v_{\mathrm{OUT}}(t)$ reaches its steady state.

Problem 3 – 20%

In this Problem a MOSFET and pull-up resistor having resistance R_{PU} are used to transmit digital data down a transmission line having inductance L as shown below. At the end of the transmission line is a receiving MOSFET having gate-to-source capacitance C_{GS}. Model the transmitting MOSFET with a switch-resistor model having on-state resistance R_{ON}.



(3A) Assume that v_{IN} turns the transmitting MOSFET off at $t = 0$ after it was on for a very long time. In this case, derive *but do not solve* the differential equation that describes the evolution of $v(t)$, the gate-to-source voltage of the receiving MOSFET. Also provide the corresponding initial conditions in terms of $v(t)$ and its derivatives at $t = 0$.

Eqn:

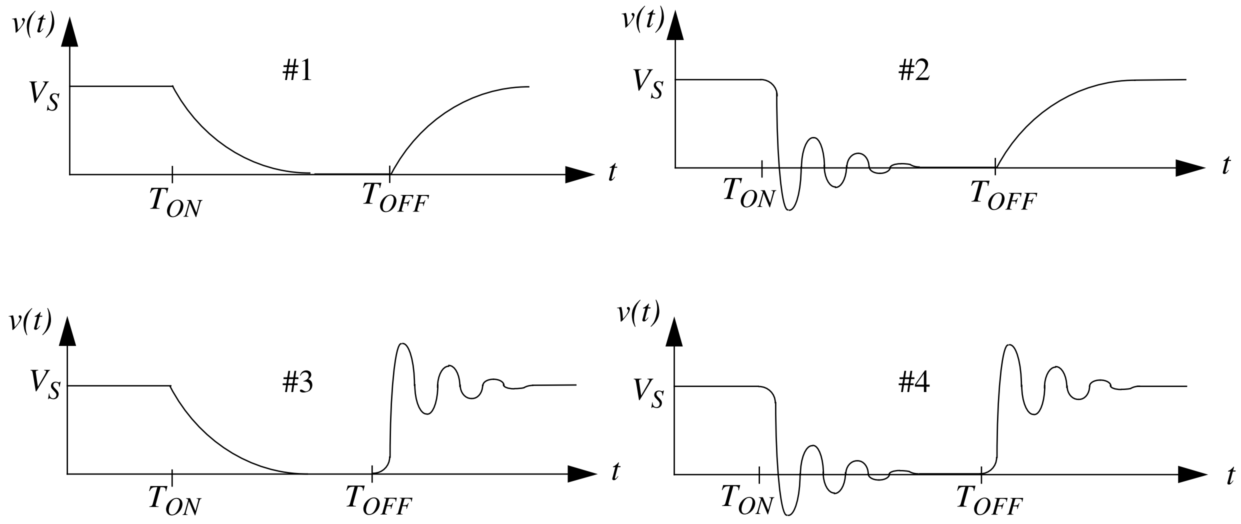
IC:

(3B) Assume that v_{IN} turns the transmitting MOSFET on at $t = 0$ after it was off for a very long time. In this case, derive *but do not solve* the differential equation that describes the evolution of $v(t)$, the gate-to-source voltage of the receiving MOSFET. Also provide the corresponding initial conditions in terms of $v(t)$ and its derivatives at $t = 0$.

Eqn:

IC:

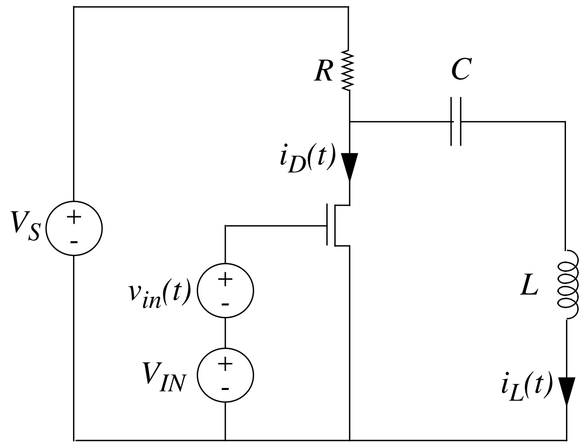
(3C) Assume that $R_{\mathrm{ON}} \ll \sqrt{L/C_{\mathrm{GS}}} \ll R_{\mathrm{PU}}$. In this case, which of the following sketches best describes the evolution of $v(t)$ given that the transmitting MOSFET turns on at T_{ON} and off at T_{OFF}? Why?



Sketch: Why?

Problem 4 – 20%

A MOSFET amplifier is coupled to an inductive load through a capacitor as shown below. The MOSFET is biased into saturated operation by the large signal $V_{\rm IN}$ so that $i_{\rm D}(t) = \frac{K}{2}(v_{\rm GS}(t) - V_{\rm T})^2$. In addition, the MOSFET is excited by the small signal $v_{\rm in}(t)$.



(4A) Let $v_{\rm in}(t) = 0$, and determine $I_{\rm D}$ and $I_{\rm L}$, the large-signal bias components of $i_{\rm D}(t)$ and $i_{\rm L}(t)$, respectively, in terms of $V_{\rm IN}$ and the MOSFET and circuit parameters.

$I_{\rm D} =$	$I_{\rm L} =$

(4B) Draw a small-signal circuit model that relates $i_l(t)$, the small-signal component of $i_L(t)$, to $v_{in}(t)$. Clearly label all parameters in the small-signal circuit model.

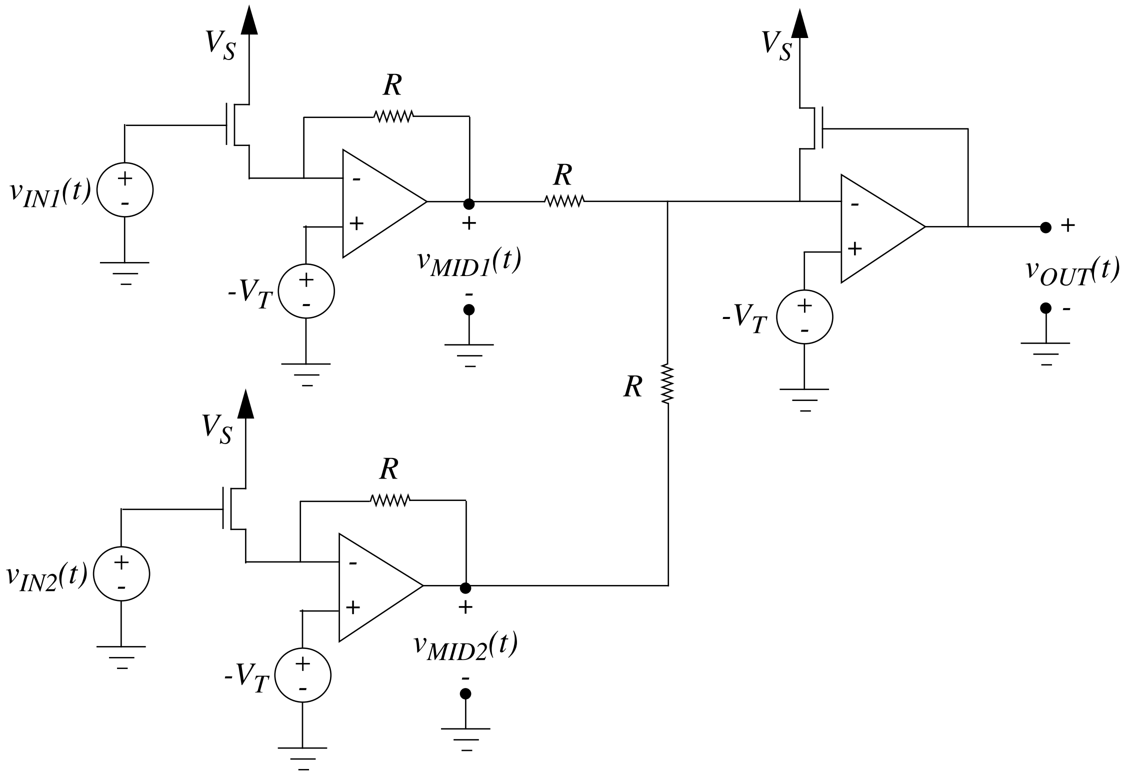
Circuit:

(4C) Assume that $v_{\text{in}}(t) = \Re\left\{V_{\text{in}} e^{j\omega t}\right\}$ such that $i_{\text{l}}(t) = \Re\left\{I_{\text{l}} e^{j\omega t}\right\}$ where V_{in}, and I_{l} are complex constants. Determine I_{l} in terms of V_{in} and the small-signal circuit model parameters.

$I_{\text{l}} =$

Problem 5 – 20%

The circuit shown below has two non-negative input voltages, $v_{\mathrm{IN1}}(t)$ and $v_{\mathrm{IN2}}(t)$, and one output voltage $v_{\mathrm{OUT}}(t)$; two intermediate voltages, $v_{\mathrm{MID1}}(t)$ and $v_{\mathrm{MID2}}(t)$, are also defined. In analyzing this circuit, assume that each op-amp is ideal and that each MOSFET operates in its saturation region so that $i_{\mathrm{D}}(t) = \frac{K}{2}(v_{\mathrm{GS}}(t) - V_{\mathrm{T}})^2$.



(5A) Determine $v_{\mathrm{MID1}}(t)$ as a function of $v_{\mathrm{IN1}}(t)$.

$v_{\mathrm{MID1}}(t) =$

(5B) Determine $v_{\mathrm{OUT}}(t)$ as a function of $v_{\mathrm{MID1}}(t)$ and $v_{\mathrm{MID2}}(t)$.

$v_{\mathrm{OUT}}(t) =$

(5C) Determine $v_{\mathrm{OUT}}(t)$ as a function of $v_{\mathrm{IN1}}(t)$ and $v_{\mathrm{IN2}}(t)$.

$v_{\mathrm{OUT}}(t) =$