Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science

6.002 – Electronic Circuits
Spring 1999

Final Exam

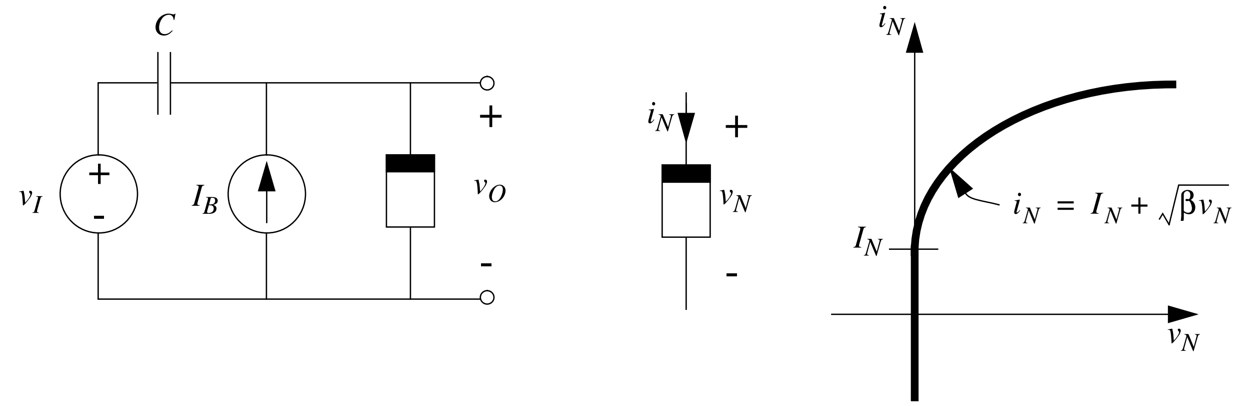
- Please put your name in the space provided below, and circle the name of your recitation instructor and the time of your recitation.
- To the extent possible, do all of your work on the pages contained within this exam. In particular, try to do your work for each question within the boundaries of the question, or on the back side of the page preceding the question.
- You may use one double-sided page of notes while taking this exam.
- Final grades in 6.002 will not be given out by phone or by e-mail. Rather, they should be available through WEBSIS by May 25. You may take back and/or review your final exam on or after May 24.
- Good luck!

Name: ______________________________

Instructor:	Fonstad	Antoniadis	Akinwande	Hagelstein	Parker
Time:	9 10	10 11	11 12	11 12	1 2

Problem 1 – 20 Points

This problem studies the network shown below which contains two sources, a capacitor and a nonlinear resistor. Throughout this problem, the value of the current source, I_B, remains constant. Also, the nonlinear resistor exhibits the terminal relation $i_\mathrm{N} = I_\mathrm{N} + \sqrt{\beta v_\mathrm{N}}$ for $i_\mathrm{N} \geq I_\mathrm{N}$, where β and I_N are positive constants, and $v_\mathrm{N} = 0$ for $i_\mathrm{N} < I_\mathrm{N}$.



(A) Let $v_\mathrm{I} = V_\mathrm{I}$, where V_I is a constant. Determine the range within which I_B must fall for v_O to be greater than zero. *Assume from this point forward that I_B falls within this range.*

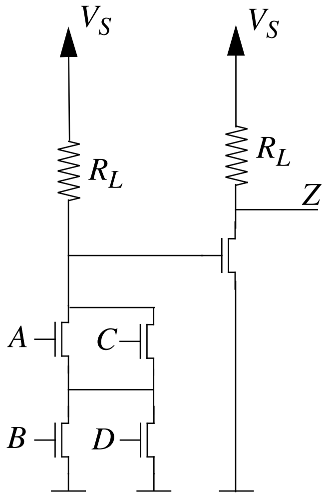
(B) Again let $v_\mathrm{I} = V_\mathrm{I}$, where V_I is a constant. Determine V_O which is the resulting value of v_O.

(C) Now let $v_{\mathrm{I}} = V_{\mathrm{I}} + v_{\mathrm{i}}$, and $v_{\mathrm{O}} = V_{\mathrm{O}} + v_{\mathrm{o}}$, where V_{I} and V_{O} are the constants from Part (B), and v_{i} and v_{o} are small signals. Derive a linear small-signal circuit model that can be used to determine v_{o} from v_{i}. Draw the model and label the components in the model with their values.

(D) Let $v_{\mathrm{i}} = a_{\mathrm{i}} \cos(\omega t)$, where a_{i} is a small amplitude. Following Part (C), determine a_{o} and ϕ_{o} such that $v_{\mathrm{o}} = a_{\mathrm{o}} \cos(\omega t + \phi_{\mathrm{o}})$ in sinusoidal steady state.

Problem 2 – 20 Points

This problem studies the power consumed by an NMOS digital logic circuit and its CMOS counterpart. The circuit shown below is an NMOS digital logic circuit and is therefore constructed from n-channel MOSFETs and pull-up resistors. It has the four inputs A, B, C, and D, and the one output Z.

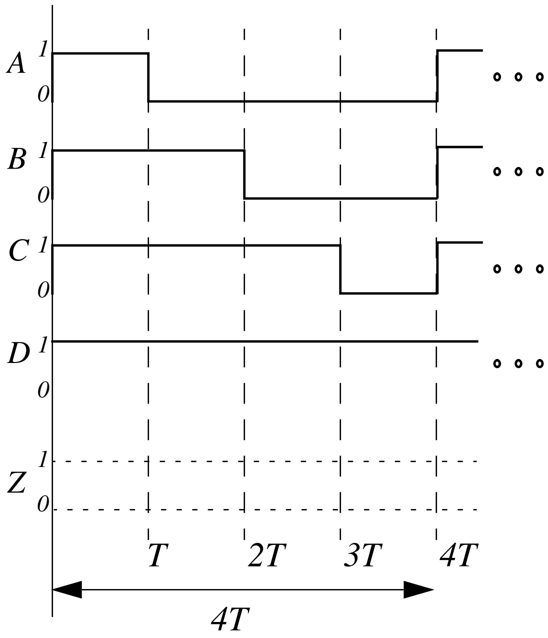


(A) Assume that a logic 1 is represented by a high-valued voltage and a logic 0 is represented by a low-valued voltage. Write a truth table and a boolean expression that describes the operation of the NMOS digital logic circuit.

A	B	C	D	Z
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Z =

(B) Model all MOSFETs with a switch-resistor model having an on-state resistance of R_{ON}, and determine the output Z for the input sequence shown below. Also, determine the time-average *static* power consumed by the digital logic circuit for this input sequence. Note that the figure shows one cycle of the input sequence, which repeats with a period of $4T$.



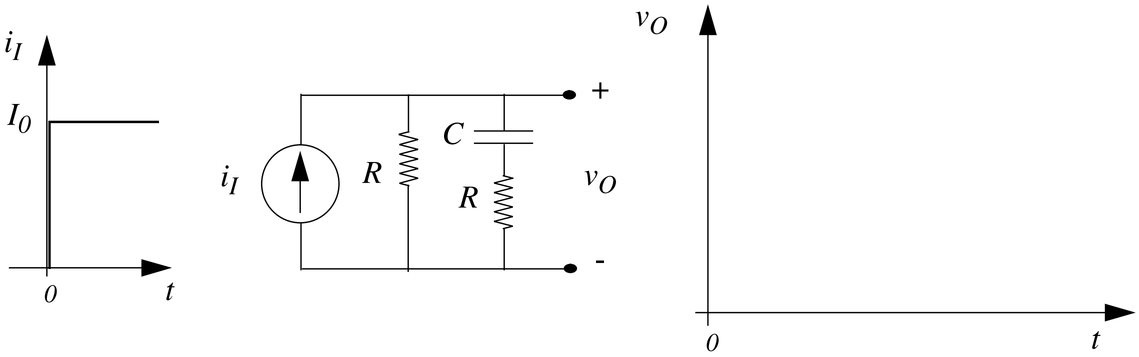
(C) Convert the NMOS digital logic circuit to its corresponding CMOS implementation by replacing its pull-up resistors with p-channel MOSFETs connected appropriately.

(D) Now add a gate-to-source capacitance of value C_{GS} to the n-channel and p-channel MOSFET models. With the revised MOSFET models, compute the time-average *dynamic* power consumed by the CMOS circuit for the inputs given in Part (B). Assume the T is long enough to permit complete capacitor charging and discharging.

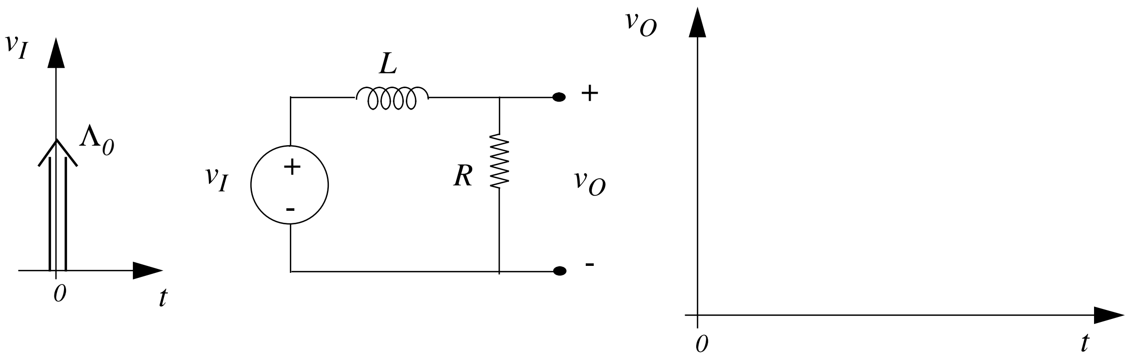
Problem 3 – 20 Points

For each of the five networks shown below, neatly sketch and clearly label its output for $t \geq 0$. Also, provide an expression for the output for $t \geq 0$. Assume that all network states are zero for $t < 0$.

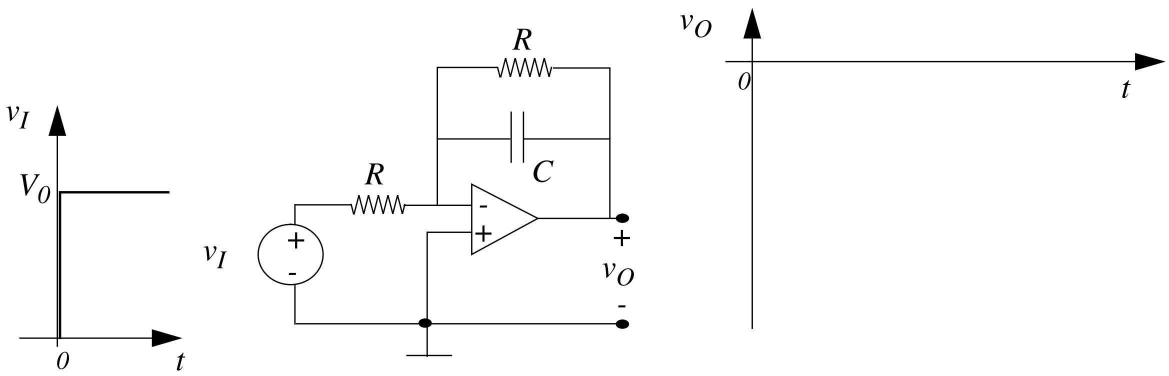
(A) In this network, the output is v_O.



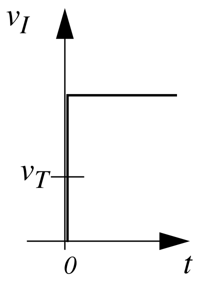
(B) In this network, the output is v_O.

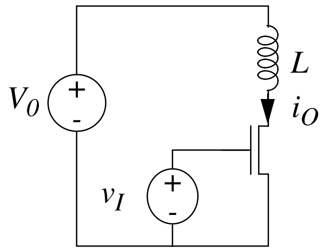


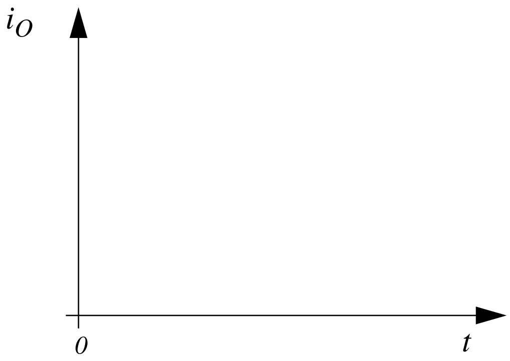
(C) In this network, the output is v_O. Assume that the op-amp is ideal.



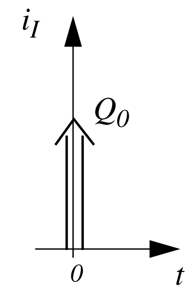
(D) In this network, the output is i_{O}. Assume that the MOSFET behaves like a switch with a threshold voltage of v_{T} and a zero on-state resistance.

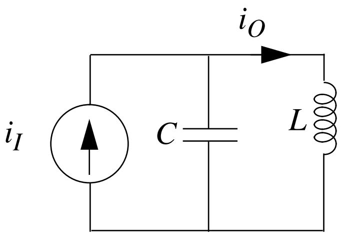


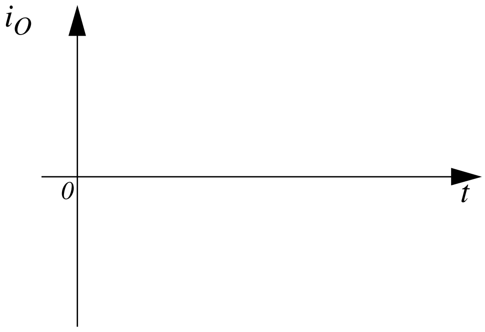




(E) In this network, the output is i_{O}.

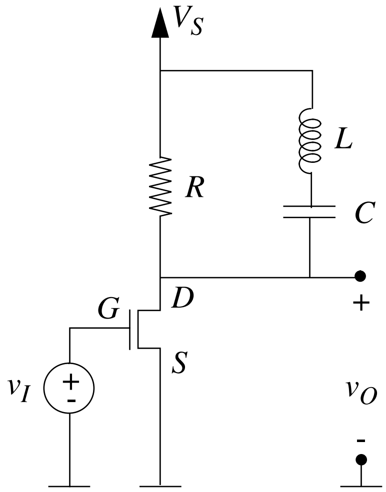






Problem 4 – 20 Points

This problem studies the filter shown below. The MOSFET in this filter operates in its saturation region for $v_{\mathrm{DS}} \geq v_{\mathrm{GS}} - v_{\mathrm{T}}$ and $v_{\mathrm{GS}} \geq v_{\mathrm{T}}$ where v_{T} is its threshold voltage. Within this region, unlike the MOSFETs you have seen previously, i_{DS} is *linearly* related to v_{GS} according to $i_{\mathrm{DS}} = K(v_{\mathrm{GS}} - v_{\mathrm{T}})$.



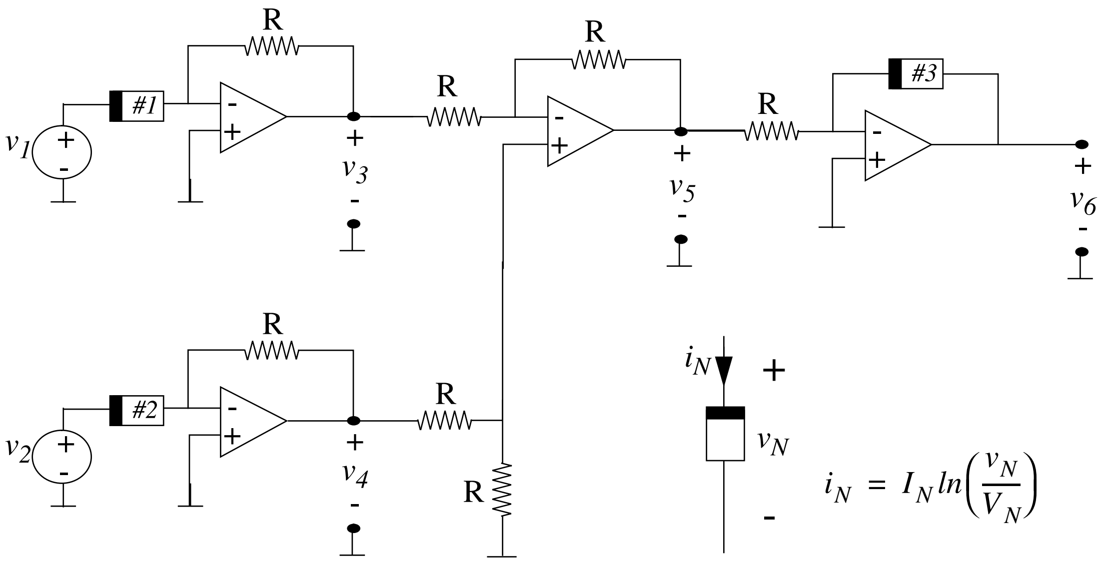
(A) Assume that the MOSFET operates in its saturation region. Let $v_{\mathrm{I}} = V_{\mathrm{I}}$, where V_{I} is a constant. Determine V_{O}, the resulting value of v_{O}.

(B) Following Part (A), determine the range of V_{I}, and the corresponding range of V_{O}, within which the MOSFET operates in its saturation region.

(C) Now let $v_{\mathrm{I}} = V_{\mathrm{I}} + v_{\mathrm{i}} \cos \omega t$, where V_{I} and v_{i} are constants, and assume that the MOSFET operates in its saturation region. In this case, v_{O} takes the form $v_{\mathrm{O}} = V_{\mathrm{O}} + v_{\mathrm{o}} \cos(\omega t + \phi_{\mathrm{o}})$ in steady state, where V_{O}, v_{o} and ϕ_{o} are constants. Determine the amplitude v_{o}.

Problem 5 – 20 Points

This problem studies the circuit shown below, which contains linear resistors, nonlinear resistors and op-amps. The nonlinear resistors all exhibit the terminal relation $i_N = I_N \ln(v_N / V_N)$, for $v_N \geq V_N$, and $i_N = 0$ otherwise, where I_N and V_N are constants. Assume that the op-amps are ideal.



(A) Assume that $v_{N1} \geq V_N$ and that $v_{N2} \geq V_N$. Determine v_3 in terms of v_1, and determine v_4 in terms of v_2.

(B) Determine v_5 in terms of v_3 and v_4.

(C) Assume that $v_{\mathrm{N3}} \geq V_{\mathrm{N}}$. Determine v_6 in terms of v_5.

(D) Assume that v_{N1}, v_{N2} and v_{N3} all equal or exceed V_{N}. Determine v_6 in terms of v_1 and v_2.

(E) What constraints must be imposed on v_1 and v_2 so that v_{N1}, v_{N2} and v_{N3} all equal or exceed V_{N}?