**MASSACHVSETTS INSTITVTE OF TECHNOLOGY**
**Department of Electrical Engineering and Computer Science**

# 6.002 – Electronic Circuits
# Fall 2001

## Reading List and Outline

| Date | Topic | Reading: |
|---|---|---|
| R 9/5 | Elements: Resistors, Sources; Voltage, Current | 1 |
| L 9/6 | Maxwell's Equations: KVL & KCL, Analysis | 1, 2 |
| R 9/7 | KVL & KCL, Series & Parallel, Resistor Dividers | 2.1–2.5, 2.7 |
| L 9/11 | Node Analysis | 3.1–3.3.2, 3.3.4 |
| R 9/12 | Node Analysis Examples | 3.1–3.3.2, 3.3.4 |
| L 9/13 | Linearity & Superposition, Thevenin & Norton | 3.5, 3.6 |
| R 9/14 | Thevenin & Norton Examples | 3.6, 3.7 |
| L 9/18 | Dependent Sources, Ports & Amplifiers | 2.6, 7.1 |
| R 9/19 | Analysis with Dependent Sources | 3.3.3, 3.5.1, 7.2 |
| L 9/20 | Transistors & Models; Amplifiers & Switches | 6.6, 7.3, 7.4 |
| R 9/21 | MOS Transistor Characteristics and Models | 7.4, 7.8, 7.9 |
| L 9/25 | MOS amplifiers & Biasing | 7.5–7.7 |
| R 9/26 | Practice with Load Lines | 7.6 |
| L 9/27 | Small signal analysis | 8 |
| R 9/28 | Small signal analysis example | 8 |
| | End of quiz 1 material. | |
| L 10/2 | Digital Abstraction & Logic | 5 |
| R 10/3 | Digital Logic Examples | 5 |
| L 10/4 | MOS Switches & Digital Logic; Static Power | 6 |
| R 10/5 | MOS Switches & Digital Logic | 6 |
| R 10/10 | No class due to evening quiz | |
| L 10/11 | State, Memory; RC Networks & Step Responses | 9, 10.1 |
| R 10/12 | RL Networks & Step Responses | 10.2 |
| L 10/16 | Transient Response Relations – Impulses | 9.4.3, 10.5.3 |
| R 10/17 | Digital circuit delay | 10.3 |
| L 10/18 | Digital memory | 11 |
| R 10/19 | Digital memory | 11 |
| L 10/23 | LC Networks & Responses | 13 |
| R 10/24 | RLC Networks & Responses | 13 |
| L 10/25 | Impedance & Admittance; $e^{st}$ | 14.1–14.3 |

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| R 10/26 | Impedance & Admittance examples | 14.3 |
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| L 10/30 | SSS & frequency response; poles & zeros | 14.4 |
| R 11/31 | SSS & frequency response examples | 14.5 |
| L 11/1 | Filters, RLC Network SSS & Q | 14.6, 15.3 |
| R 11/2 | Resonance; time-frequency response | 15.1, 15.2 |
| | End of quiz 2 material. | |
| L 11/6 | Op-Amps & Feedback Amplifiers | 16.1–16.3 |
| R 11/7 | Op-Amp inverting amp | 16.3 |
| L 11/8 | Add & Sub & Int & Diff | 16.5, 16.6 |
| R 11/9 | Op-Amp Circuits and D-to-A | 16.6 |
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| L 11/13 | Resonant Impedance Match – synthesis | special topic |
| R 11/14 | No class due to evening quiz | |
| L 11/15 | Differential Amplifiers – How an Op amp works | 8Ex107 |
| R 11/16 | Op-Amp Filters | 16.6 |
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| L 11/20 | Positive Feedback & Oscillation; Schmitt Trigger | 16.7, 16.8 |
| R 11/21 | Positive Feedback & Oscillation | 16.7, 16.8 |
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| L 11/27 | Energy & Power in digital logic, CMOS | 12 |
| R 11/28 | CMOS examples | 12 |
| L 11/29 | Nonlinear: Diode switch or Attenuator | 17 |
| R 11/30 | Assumed states, Diode Wave Shaper | 17.5 |
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| L 12/4 | Clocks | special topic |
| R 12/5 | | |
| L 12/6 | Chaos | special topic |
| R 12/7 | | |
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| L 12/11 | Limitations of Lumped Parameter Abstraction | 1 |
| R 12/12 | Review | everything |