MASSACHVSETTS INSTITVTE OF TECHNOLOGY
Department of Electrical Engineering and Computer Science

6.002 – Electronic Circuits
Fall 2001

Problem Set 11

Issued: November 15, 2001 Due: November 28, 2001

Readings:

- Agarwal & Lang Section 16.6 for Friday, November 16.
- Agarwal & Lang Sections 16.7 and 16.8 for Tuesday, November 20.
- Agarwal & Lang Chapter 12 for Tuesday, November 27.

Introduction:

This problem set focuses on the analysis and design of a system for playing back a digitally-stored audio signal. Additionally, this assignment serves as the pre-lab exercises for Lab 4, which will involve the construction, testing, and demonstration of the audio playback system. *Consequently, you must save a copy of your results for use during Lab 4.*

A block diagram of the audio playback system is shown in Figure 1. At the center of the system is a digital memory in which 32,768 samples of the audio signal are stored. Each sample in the memory has a unique numerical address between 0 and 32,767, inclusive. Consecutive samples are stored at consecutive addresses.

To obtain 32,768 consecutive samples of the audio signal, 4.096 seconds of continuous analog audio signal are first sampled at an 8-kHz rate. The analog audio samples are then digitized by an 8-bit analog-to-digital converter. That is, the samples are quantized to take on one of 256 possible discrete digital values between 0 and 255, inclusive. Here, the digital value of 0 corresponds to the most positive signal voltage, and the digital value of 255 corresponds to the most negative signal voltage. The resulting digital data is then written into the memory.

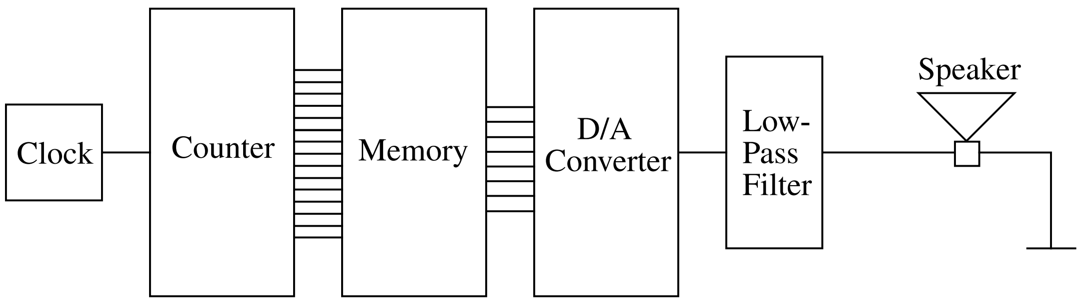

Figure 1: block diagram of the audio playback system.

To retrieve the stored audio signal samples in sequence at the proper rate, the memory is addressed by a counter which counts from 0 to 32,767 at an 8-kHz rate established by an external clock. After counting to 32,767 the counter returns to 0, and the retrieval process repeats itself. As the memory address increments, the corresponding data appears at the memory output. This data is converted back to an analog voltage in a piecewise constant manner by a digital-to-analog converter.

During the course of recording and playing back the analog audio signal, the signal is sampled in time, quantized in amplitude, and reconstructed in a piecewise constant manner. As you will learn in 6.003, this process introduces undesirable high-frequency components into the signal. To minimize the perceived impact of these components, the signal is filtered by a low-pass filter after it is reconstructed by the digital-to-analog converter. Finally, the signal is fed into a speaker.

In the course of this homework assignment you will analyze and design three of the functional blocks shown in Figure 1. These blocks are the clock, the digital-to-analog converter, and the low-pass filter. In Lab 4, you will construct these blocks and verify that they perform as desired. Then, you will combine them with the counter, the read-only memory, and the speaker to construct and demonstrate the entire audio playback system.

Problems:

1. The circuit shown in Figure 2 is the system clock, which is a square-wave oscillator followed by a CMOS inverter; the inverter functions only as a buffer. The oscillator is constructed from another CMOS inverter, a resistor, and a capacitor. Both inverters are powered between the positive supply voltage V_S and ground, and both exhibit the hysteretic input-output characteristic defined in the figure. The inverters are otherwise ideal.

   (A) Assume that v_{CAP} has just charged up to V_H so that v_{OSC} has just switched to 0 V. How much time elapses before v_{CAP} decays to V_L, which in turn causes v_{OSC} to switch to V_S?

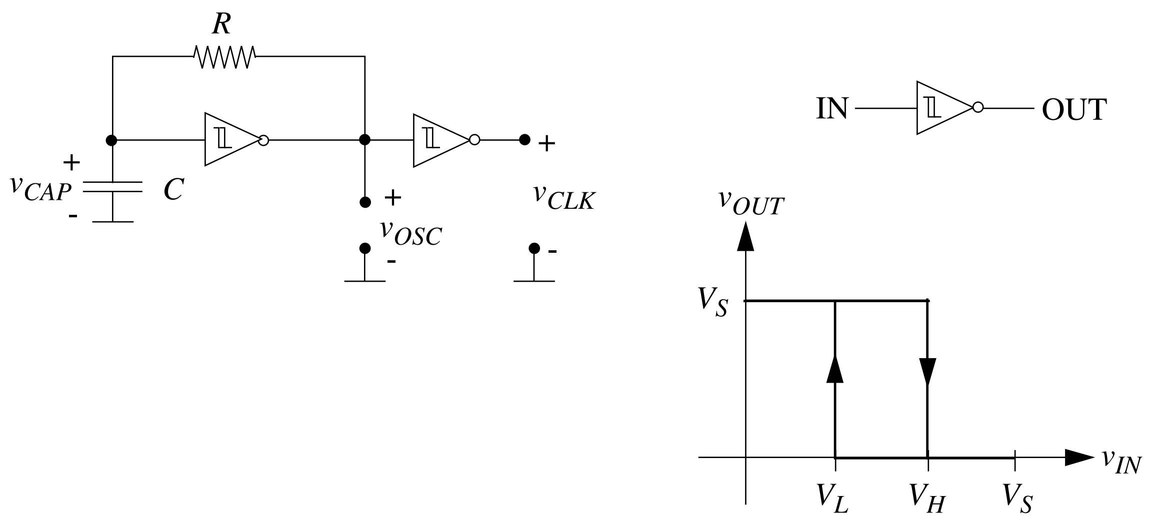

Figure 2: the system clock.

(B) Assume that v_{CAP} has just decayed to V_L so that that v_{OSC} has just switched to V_S. How much time elapses before v_{CAP} charges up to V_H, which in turn causes v_{OSC} to switch to 0 V?

(C) Determine the frequency of the oscillator in terms of R, C, V_L, V_H, and V_S.

(D) Assume that $V_L = 1.8$ V, $V_H = 3.0$ V, and $V_S = 5.0$ V. Choose values for R and C so that the oscillator oscillates at or very near 8 kHz. Since oscillator frequency alone under-specifies R and C, there is no single correct choice. Therefore, choose values for R and C which are easily implemented with the components in the 6.002 lab kit.

(E) For the choice of R and C from Part (D), sketch and clearly label a single graph that displays v_{CAP}, v_{OSC}, and v_{CLK} as a function of time over one period of oscillation.

2. The circuit shown in Figure 3 is the digital-to-analog converter. The voltage sources v_{DB0} through v_{DB7} represent the voltages supplied by the eight data bits of the digital memory, DB0 through DB7. These voltages will be approximately 5 V when the corresponding data bit is a logical high, and approximately 0 V when the corresponding data bit is a logical low. The voltage v_{OFF}, which is set by a potentiometer, is an offset voltage that is used to center the output of the converter around 0 V. Assume that the op-amp in the converter is ideal.

   (A) Determine v_{DAC} as a function of v_{DB0} through v_{DB7}, and v_{OFF}.

   (B) With $v_{OFF} = 0$ V, the output of the digital-to-analog converter should span the range of 0 V to -2.5 V. Thus, the output of the converter should be given by

$$v_{DAC} = -2.5 \text{ V} \sum_{i=0}^{7} \frac{2^i}{255} \text{DB}i$$

   where each data bit DBi takes on the numerical value of 1 when high and 0 when low. In this manner, each successive data bit from DB0 to DB7 is given a voltage weighting twice

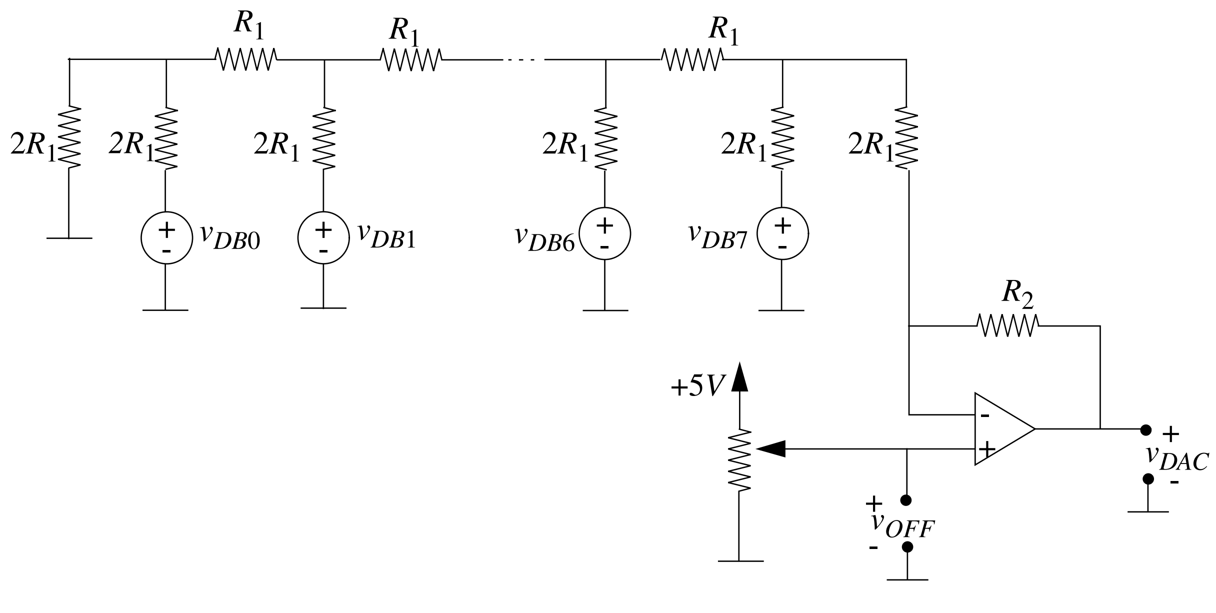

Figure 3: the digital-to-analog converter.

that of the preceding data bit, making it possible for the converter to output voltages from 0 V to -2.5 V in steps of $-2.5/255$ V. Given this, determine R_2 in terms of R_1.

The input voltage rating of the speaker is approximately ± 1.25 V. Since the low-pass filter has unity voltage gain over the frequency range of interest, the output range of the digital-to-analog converter must be designed to match the speaker rating. This is why the range is chosen to be 0 V to -2.5 V, with $v_{OFF} = 0$. Note further that the output range of the converter is negative. This is because the converter is based upon the inverting amplifier configuration.

(C) The role of v_{OFF} is to offset the output of the digital-to-analog converter so that it is centered around 0 V. That is, with DB0 through DB7 all low, v_{DAC} should be 1.25 V, and with DB0 through DB7 all high, v_{DAC} should be -1.25 V. Given this, what must be the value of v_{OFF}?

(D) Assume that $R_1 = 10$ kΩ. Use the result of Part (B) to determine R_2.

3. The circuit shown in Figure 4 is the low-pass filter. It is a second-order filter, and is driven by the output of the digital-to-analog converter. Its purpose is to remove the high-frequency components of the audio signal that result from the sampling, quantization and reconstruction of that signal. Assume that the op-amp in the filter is ideal.

   (A) Assume that the low-pass filter operates in sinusoidal steady state with $v_{DAC} = \Re\{V_{dac}e^{j\omega t}\}$ and $v_{LPF} = \Re\{V_{lpf}e^{j\omega t}\}$ where V_{dac} and V_{lpf} are complex amplitudes. Find the input-output transfer function $H_{LPF}(\omega)$ of the filter where $H_{LPF}(\omega) \equiv V_{lpf}/V_{dac}$.

   (B) Using the results of Part (A), find the magnitude and phase of $H_{LPF}(\omega)$.

   (C) There is no best design for the low-pass filter to meet the needs of the audio playback system. However, with the appropriate choice of C_1, C_2, and R, the transfer function of one good design will take the form

$$|H_{LPF}(\omega)| = \frac{1}{1 + (\omega/\omega_{LPF})^2}$$

   where ω_{LPF} is a specified frequency. For this design, show that the low-frequency and

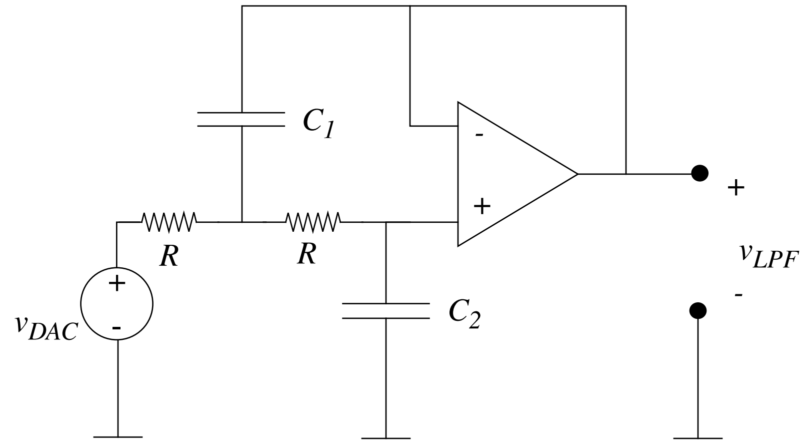

Figure 4: the low-pass filter.

high-frequency asymptotes of $|H_{LPF}(\omega)|$ intersect at $\omega = \omega_{LPF}$, and therefore that ω_{LPF} is the frequency that delineates the pass band of the low-pass amplifier.

(D) What constraints must be imposed on C_1, C_2, and R to obtain the low-pass filter transfer function described in Part (C)?

(E) Given that the low-pass filter is to be designed as described in Part (C), use the results of Part (D) to choose values for C_1, C_2, and R so that $\omega_{LPF} \approx 2\pi \times 4000$ rad/s. Since the results of Part (D) under-specify C_1, C_2, and R, there is no single correct choice. Therefore, choose C_1, C_2, and R so that they are easily implemented with the components in the 6.002 lab kit.

(F) Given the choice of C_1, C_2, and R from Part (E), determine ω_{LPF}, and plot both the log-magnitude and phase of $H_{LPF}(\omega)$ against log-frequency for $2\pi \times 10^1$ rad/s $\leq \omega \leq 2\pi \times 10^5$ rad/s.