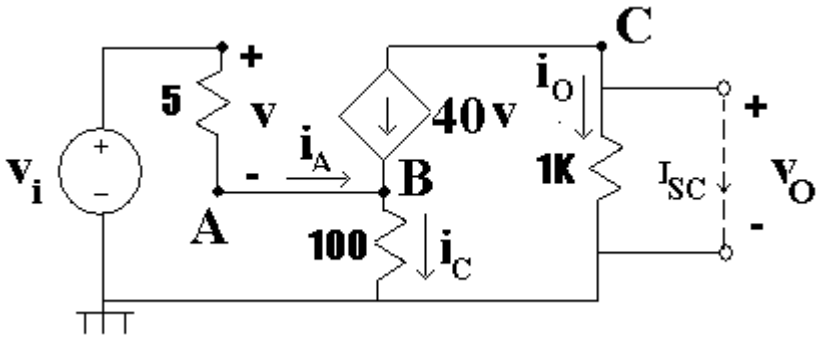
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Department of Electrical Engineering and Computer Science

6.002 – Electronic Circuits
Fall 2001

Problem Set 3 Solutions

Problem 1



a) In order to find v_O, we need to know i_O -- the current through the $1K$ resistor.

$$v_O = 1000 \cdot i_O$$

From KCL at node C, $i_O = -40v$; thus, $v_O = -40{,}000 \cdot v$.

To find v, label the ground node and compute the voltage at nodes A and B in terms of v and the known circuit variables: $v_A = v_B = v_i - v$.

Now, setup KCL at node B.

$$i_A + 40v = i_C; \quad i_A = \frac{v}{5}; \quad i_C = \frac{v_i - v}{100}.$$

So,

$$\frac{v}{5} + 40v = \frac{v_i - v}{100},$$

$$v_i = 20v + 4000v + v,$$

$$v = \frac{v_i}{4021}.$$

$$v_O = -40{,}000v; \; -10v_i.$$

The voltage gain is $g = \left|\frac{v_O}{v_i}\right|$; 10.

b) $V_{TH} = V_{OC} = v_O = -10v_i$. (from part a)

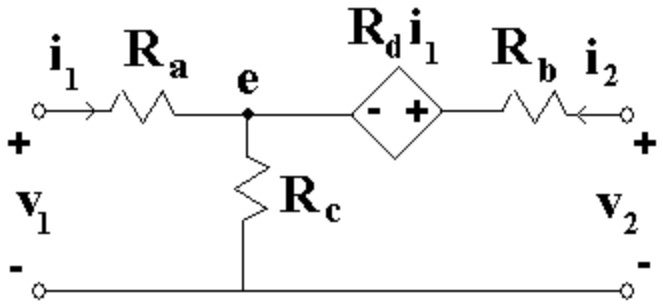
$R_{TH} = \dfrac{V_{TH}}{I_{SC}}$, where I_{SC} denotes the short circuit current through the output terminals. If the terminals are shorted, no current flows through the $1K$ resistor and $I_{SC} = -40v$. Since the rest of the circuit, which determines v, is not altered, it is still true that $v = \dfrac{v_i}{4021}$. Thus, I_{SC} ; $-\dfrac{v_i}{100}$. $R_{TH} = \dfrac{-10v_i}{-v_i/100} = 1000 = 1K$.

Problem 2

a) $i_1 = \dfrac{v_1 - R_{12}i_2}{R_{11}}$, $i_2 = \dfrac{v_2 - R_{21}i_1}{R_{22}}$.

Thus, $v_1 = R_{11}i_1 + R_{12}i_2$ and $v_2 = R_{21}i_1 + R_{22}i_2$.

b)



Choose a ground node and label voltages throughout the circuit.

KCL at node e: $i_1 + i_2 = \dfrac{e}{R_c}$, $i_1 = \dfrac{v_1 - e}{R_a}$, $i_2 = \dfrac{v_2 - e - R_d i_1}{R_b}$.

Solving for unknown voltages, $e = R_c(i_1 + i_2)$,

$$v_1 = R_a i_1 + e = (R_a + R_c)i_1 + R_c i_2$$

$$v_2 = R_b i_2 + R_d i_1 + R_c(i_1 + i_2) = (R_c + R_d)i_1 + (R_b + R_c)i_2.$$

c) Comparing the results from parts a) and b) ,

$$R_a + R_c = R_{11}, \quad R_c = R_{12}, \quad R_c + R_d = R_{21}, \quad R_c + R_b = R_{22}.$$

$R_a = R_{11} - R_c = R_{11} - R_{12}$; $R_b = R_{22} - R_c = R_{22} - R_{12}$; $R_c = R_{12}$; $R_d = R_{21} - R_{12}$.

d) The circuits are *port equivalent* by construction. However, they are NOT *terminal equivalent* because the two negative (lower) terminals are shorted together in the circuit on figure 3, but they are not connected to each other in the circuit on figure 2. That is, if you measure the voltage difference between these two terminals, it will always be zero in one case, but not necessarily so in the

other. The two circuits are equivalent only in the sense that their port variables v_1, v_2, i_1, i_2 are connected by the same set of equations:

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} R_{11} & R_{12} \\ R_{21} & R_{22} \end{bmatrix} \times \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}$$

Problem 3

In general, considering that the circuit is linear and applying superposition, we get

$$v_1 = R_{11} i_1 + R_{12} i_2$$
$$v_2 = R_{21} i_1 + R_{22} i_2$$

Now, in order to find R_{12}, we force i_1 to zero and compute v_1 as a function of i_2 only. Similarly, for R_{21}, we set i_2 to zero and compute v_2 due to i_1. The claim is that the two resistances are the same.

Case 1: $i_1 \equiv 0$.

$$v_1 = \frac{R_x}{R_x + R_y} v_2 \quad \text{(voltage divider)}$$
$$v_2 = R_z i_z \quad \text{(constitutive)}$$
$$i_z = \frac{(R_x + R_y)}{(R_x + R_y) + R_z} i_2 \quad \text{(current divider)}$$
$$v_1 = \frac{R_x}{R_x + R_y} R_z \frac{R_x + R_y}{R_x + R_y + R_z} i_2 = \frac{R_x R_z}{R_x + R_y + R_z} i_2$$
$$\text{Thus, } R_{12} \ @ \frac{R_x R_z}{R_x + R_y + R_z}.$$

Case 2: $i_2 \equiv 0$.

$$v_2 = \frac{R_z}{R_y + R_z} v_1 \quad \text{(voltage divider)}$$
$$v_1 = R_x i_x \quad \text{(constitutive)}$$
$$i_x = \frac{(R_y + R_z)}{(R_y + R_z) + R_x} i_1 \quad \text{(current divider)}$$
$$v_2 = \frac{R_z}{R_y + R_z} R_x \frac{R_y + R_z}{R_x + R_y + R_z} i_1 = \frac{R_x R_z}{R_x + R_y + R_z} i_1$$
$$\text{Thus, } R_{21} \ @ \frac{R_x R_z}{R_x + R_y + R_z}.$$

We have demonstrated that $R_{12} \equiv R_{21}$ for this network.

Problem 4

a) The relationship between v_{IN} and v_{MID} is the same as the relationship between v_{MID} and v_{OUT} because, apart from the common voltage, v_{MID}, the two transistor circuits are completely decoupled: there is no current flowing from one to the other. If the input resistance of the second MOSFET weren't infinite, the situation would be different. There would be a nonzero current flowing into it's gate terminal and ultimately changing the KCL at its G-D-S supernode. Then, the current flowing through the load resistance would no longer be equal to the drain-to-source current, $i_{DS} \neq \frac{V_S - v_{OUT}}{R}$, and it would, in general, depend on the current flowing out of the first MOSFET.

b) According to the description in Problem 2 on page 486 in the text, the first MOSFET can be operating in three states, depending on the value of v_{IN}.

If $v_{IN} < V_T$, then the MOSFET looks like an open circuit, and hence $v_{MID} = V_S$.

If the input voltage is sufficiently large, $v_{IN} > V_T + \varphi$, for some φ to be determined later, the MOSFET looks like a short circuit, and $v_{MID} = 0$.

In between, the MOSFET looks like a dependent current source with the current set at $i_{DS} = \frac{K}{2}(v_{IN} - V_T)^2$ and $v_{MID} = V_S - \frac{K \cdot R}{2}(v_{IN} - V_T)^2$.

The value of φ can be determined by constraining the MOSFET to be both in the 'unsaturated' and in the 'saturated' regions.

When MOSFET is 'on', the current that flows from its drain to its source is $i_{DS} = \frac{V_S}{R}$.

When it's saturated, the current is $i_{DS} = \frac{K}{2}(v_{IN} - V_T)^2$.

Equating the two, we find the critical value of $v_{IN} = V_T + \sqrt{\frac{2V_S}{K \cdot R}} = V_T + \varphi$.

By the argument in part a), the relationship between v_{MID} and v_{OUT} is exactly the same as that between v_{IN} and v_{MID}.

Thus, for $v_{MID} < V_T$, $v_{OUT} = V_S$. For $v_{MID} > V_T + \sqrt{\frac{2V_S}{K \cdot R}}$, $v_{OUT} = 0$.

For $V_T \leq v_{MID} \leq V_T + \sqrt{\frac{2V_S}{K \cdot R}}$, $v_{OUT} = V_S - \frac{K \cdot R}{2}(v_{MID} - V_T)^2$.

c) When $v_{IN} < V_T$, the first MOSFET (M1) is in cutoff. That means that there is no current flowing from its drain port and its output voltage is very high: $v_{MID} = V_S$.
The output of M1 is the input to M2 (the second MOSFET). Since the input voltage to M2 is high, we can reasonably assume that it is in the 'unsaturated' region and replace it with a short circuit. Then we compute its drain-to-source current, i_{DS_2}, and check whether our assumption is correct.

When M1 is an open circuit and M2 is a short circuit, $i_{DS_2} = \frac{V_S}{R}$ and the limiting value of the current is $I_T = \frac{K}{2}(V_s - V_T)^2$, which appears to be much bigger than i_{DS_2}. (When you plug in the parameters from Problem 2 on page 488, it does come out that way.)

When we increase the gate voltage of M1 beyond the threshold value, $v_{IN} \geq V_T$, M1 goes into the saturation mode, its drain current gradually starts to increase and its output voltage, v_{MID}, starts to decline from V_S. Since v_{MID} is also the gate voltage of M2, the behavior of M2 is affected as well. At first, v_{MID} is still sufficiently high that M2 remains a short circuit. However, as v_{MID} goes down to $V_T + \varphi$, M2 switches into saturation, and now both transistors are in saturation.

To determine what happens as we further increase v_{IN}, consider the point when it has just reached the value of $V_T + \varphi$ and so M1 has just become a short circuit. In that case, $v_{MID} = 0$, and M2 is already in cutoff. That means that M2 goes into cutoff while M1 is still in the saturation region. In order to find the exact values of the input voltage for which M2 goes into saturation and into cutoff, we solve for v_{IN} that produces $v_{MID} = V_T + \varphi$ and $v_{MID} = V_T$ when M1 is in saturation.

$$v_{MID} = V_T + \varphi = V_S - \frac{R \cdot K}{2}(v_{IN} - V_T)^2$$

$$v_{IN} = V_T + \sqrt{\frac{2(V_S - V_T - \varphi)}{K \cdot R}} = V_T + \theta$$

$$v_{MID} = V_T = V_S - \frac{R \cdot K}{2}(v_{IN} - V_T)^2$$

$$v_{IN} = V_T + \sqrt{\frac{2(V_S - V_T)}{K \cdot R}} = V_T + \phi$$

As a check, you can see that $\theta < \phi < \varphi$, so as v_{IN} is increased, first M1 goes into saturation, then M2 goes into saturation, then M2 goes into cutoff, and only then does M1 go into the 'unsaturated' regime, where it acts as a short circuit between drain and source terminals.

All in all, we have five separate regimes of operation between the two transistors.

Stage 1: $v_{IN} < V_T \quad \rightarrow \quad v_{MID} = V_S$ (M1 off), $v_{OUT} = 0$ (M2 on)

Stage 2: $V_T \le v_{IN} < V_T + \theta \quad \rightarrow \quad V_T + \varphi \le v_{MID} < V_S$ (M1 sat), $v_{OUT} = 0$ (M2 on)

Stage 3:

$$V_T + \theta \le v_{IN} < V_T + \phi \quad \rightarrow \quad V_T \le v_{MID} < V_T + \varphi \text{ (M1 sat)},$$

$$v_{MID} = V_S - \frac{K \cdot R}{2}(v_{IN} - V_T)^2, \quad v_{OUT} = V_S - \frac{K \cdot R}{2}(v_{MID} - V_T)^2$$

$$V_S \ge v_{OUT} > 0 \text{ (M2 sat)}$$

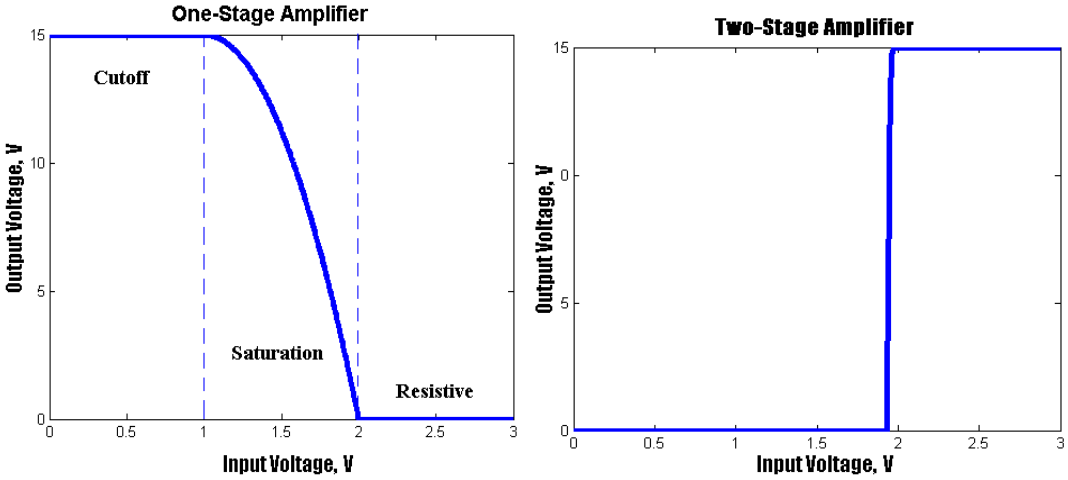
Stage 4: $V_T + \phi \le v_{IN} < V_T + \varphi \quad \rightarrow \quad v_{MID} < V_T$ (M1 sat), $v_{OUT} = V_S$ (M2 off)

Stage 5: $V_T + \varphi \le v_{IN} \quad \rightarrow \quad v_{MID} = 0$ (M1 on), $v_{OUT} = V_S$ (M2 off)

d) see Stage 3: $0 \le v_{OUT} \le V_S$

e) $V_T = 1\text{V}$, $\varphi = \sqrt{\frac{2 \cdot 15\text{V}}{15\text{e}3 \cdot 2\text{e}\text{-}3}} = 1\text{V}$, $\phi = \sqrt{\frac{2 \cdot 14}{15\text{e}3 \cdot 2\text{e}\text{-}3}}$; 0.97V,

$\phi = \sqrt{\frac{2 \cdot (15 - 1 - 1)}{15\text{e}3 \cdot 2\text{e}\text{-}3}}$; 0.93V, $\gamma = \sqrt{\frac{2 \cdot 1}{15\text{e}3 \cdot 2\text{e}\text{-}3}}$; 0.26V .



One-stage amplifier is inverting, while two-stage isn't. Another difference is that the graph of a two-stage amplifier resembles more nearly a unit step at v_{IN} ; 2V because small differences in the output of stage 1 are sufficiently amplified to make a significant difference at the output of stage 2.

Problem 5

a) By symmetry,

$$i_{D_1} = i_{D_2} = I/2$$

$$I/2 = \frac{K}{2}(v_{GS} - V_T)^2 = \frac{K}{2}(v_S + V_T)^2; \quad v_S = -\sqrt{\frac{I}{K}} - V_T .$$

The last two equations follow from the requirement that both transistors must be operated in the saturation region.

b) There are two requirements to this problem: the MOSFET must resemble a current source, so it must be operated in the saturation region; the limiting current of the transistor is fixed at the value of I.

$$v_{GS} = V_B - (-V_S) = V_B + V_S, v_{GS} \geq V_T \rightarrow V_B \geq V_S + V_T \ ;$$

$$I = \frac{K_n}{2}(v_{GS} - V_T)^2 \frac{W}{L} \rightarrow \lambda \ @ \frac{W}{L} = \frac{2I}{K_n}(V_B + V_S - V_T)^{-2}$$

c) Denote the currents flowing through the left and right sides as i_A and i_B, respectively.

$$v_{OA} = V_S - R_L i_A, \quad v_{OB} = V_S - R_L i_B$$

$$i_A = \frac{K}{2}(v_{IA} - v_S - V_T)^2, \quad i_B = \frac{K}{2}(v_{IB} - v_S - V_T)^2$$

$$i_A + i_B = I, \quad v_O = v_{OA} - v_{OB}, \quad v_{IA} = -v_{IB}$$

Solving for v_S,

$$I = \frac{K}{2}\left[(v_{IA} - (v_S + V_T))^2 + (-v_{IA} - (v_S + V_T))^2\right]$$

$$\frac{2I}{K} = 2{v_{IA}}^2 + 2(v_S + V_T)^2$$

$$v_S = -V_T - \sqrt{\frac{I}{K} - {v_{IA}}^2}$$

The square root is taken with a negative sign because v_S must be negative to insure that v_{GS} is positive for both transistors, so that they can operate in saturation region.

Solving for v_{OA}, v_{OB}, and v_O we obtain:

$$v_{OA} = V_S - \frac{R_L K}{2}(v_{IA} - v_S - V_T)^2, \quad v_{OB} = V_S - \frac{R_L K}{2}(-v_{IA} - v_S - V_T)^2$$

$$(\mathrm{K})^2 = \left(\pm v_{IA} + \sqrt{\frac{I}{K} - {v_{IA}}^2}\right)^2 = \frac{I}{K} \pm 2v_{IA}\sqrt{\frac{I}{K} - {v_{IA}}^2}$$

$$v_{OA} = V_S - \frac{R_L I}{2} - R_L K v_{IA}\sqrt{\frac{I}{K} - {v_{IA}}^2}$$

$$v_{OB} = V_S - \frac{R_L I}{2} + R_L K v_{IA}\sqrt{\frac{I}{K} - {v_{IA}}^2}$$

$$v_O = v_{OA} - v_{OB} = -2R_L K v_{IA}\sqrt{\frac{I}{K} - {v_{IA}}^2}$$