MASSACHVSETTS INSTITVTE OF TECHNOLOGY
Department of Electrical Engineering and Computer Science

6.002 – Electronic Circuits
Fall 2001

Lab 2: Logic Gates & First-Order Circuits

Introduction

The first part of the lab explores the static behavior of logic gates constructed with n-channel MOSFETs and resistors. The second part examines the dynamic behavior of the gates. You should complete the pre-lab exercises in your lab notebook before coming to lab. Then, carry out the in-lab exercises between October 22 and October 26. After completing the in-lab exercises, have a TA check your work and sign your lab notebook. Finally, complete the post-lab exercises in your lab notebook. Do *not* turn in your lab book. You will need it to complete the pre-lab exercises for Lab 3. The post-lab exercises for Lab 2 and Lab 3 will be graded together.

Pre-Lab Exercises

In Lab 1, we explored the saturated region of MOSFET operation. Here, we will explore the cutoff and linear regions in the context of logic gates. When dealing exclusively with these regions, it is convenient to think of the MOSFET as a switched resistor, as discussed in sections 6.5 and 7.8 of the notes.

(2-1) Figure 1 shows a NOT gate, or inverter, a NOR gate and a NAND gate constructed from n-channel MOSFETs and 1 kΩ resistors. The figure also shows a switch-resistor model for the n-channel MOSFET. Using the switch-resistor model, compute v_{OUT} for all three gates. In doing so, consider all combinations of input voltages; an input voltage may be either above or below the MOSFET threshold voltage V_T. In each case, evaluate v_{OUT} assuming $R_{ON} = 4\ \Omega$. Summarize your results for each gate in a table.

(2-2) Figure 2 shows a combinational logic circuit. Determine the input-output truth table for this circuit.

(2-3) Draw the circuit diagram for the combinational logic circuit shown in Figure 2 using the gates shown in Figure 1.

(2-4) Consider the network shown in Figure 3. First, assume that $v_{OUT} = 0$ at $t = 0$. Then, write an expression for $v_{OUT}(t)$ for $t \geq 0$ given that v_{IN} steps from 0 V to V_I at $t = 0$.

(2-5) For the transient determined in Pre-Lab Exercise 2-4, determine the time at which v_{OUT} reaches a given V_T where $0 < V_T < \frac{R_2}{R_1+R_2}V_I$.

In-Lab Exercises

(2-1) You have been provided with five 2N7000 MOSFETs in your lab kit. These will be used to construct the three gates illustrated in Figure 1. However, before building the gates, you will

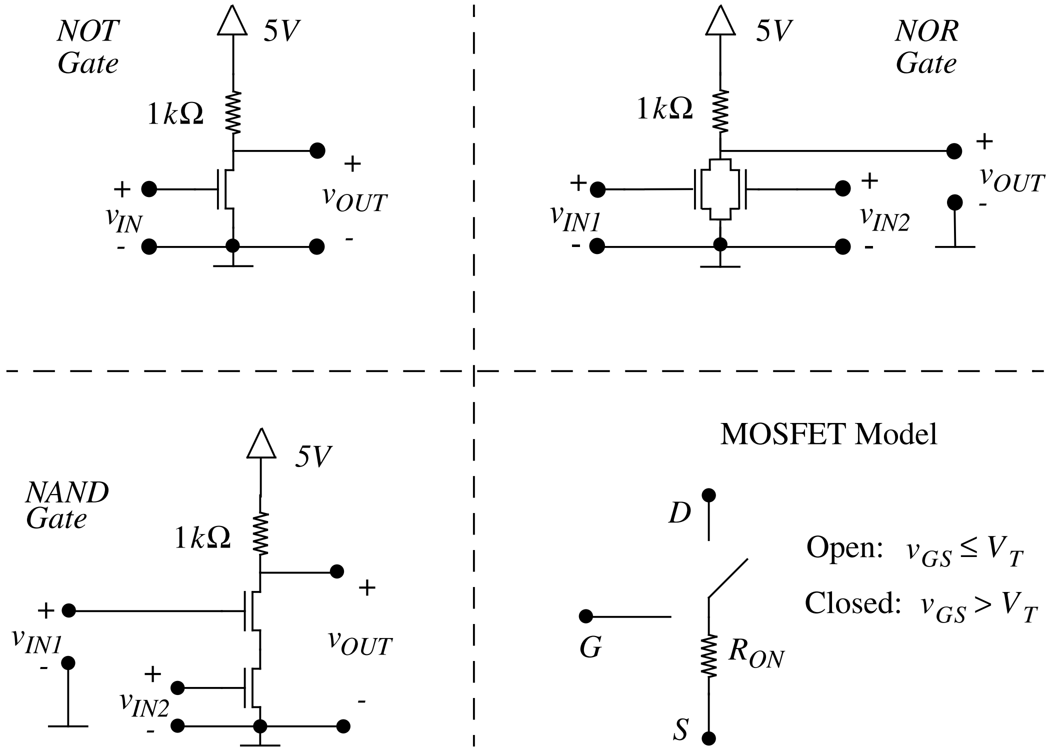

Figure 1: a NOT gate, a NOR gate, a NAND gate, and the switch-resistor MOSFET model.

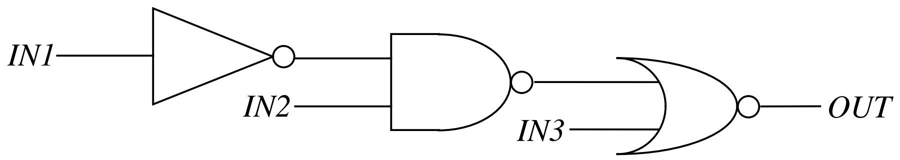

Figure 2: combinational logic circuit for Pre-Lab Exercises 2-2 and 2-3.

need to measure the R_{ON} values for each of the MOSFETs. The method of measurement is illustrated in Figure 4. With v_{GS} at 5 V, measure R_{DS} with the multimeter. This resistance is R_{ON} for $v_{GS} = 5$ V; note that the multimeter supplies a very small voltage when used as an ohmmeter. After you have measured all of the devices, make sure you keep track of which device is which in the logic gate circuits, as it will be essential for interpretation of data in the post-lab exercises.

(2-2) Construct the NOT gate from Figure 1 and connect its input to a switch and 10 kΩ resistor as shown in Figure 5. For both switch positions, that is for both logic input levels to the gate, measure v_{OUT} with the multimeter. *Save the NOT gate for In-Lab Exercise 2-5.*

Important note: The switch packs and the 10 kΩ resistor array have been chosen to simplify the wiring of the switches to their associated resistors. Specifically, a switch pack can be placed in the protoboard so that one side is on a common ground strip and each pin on

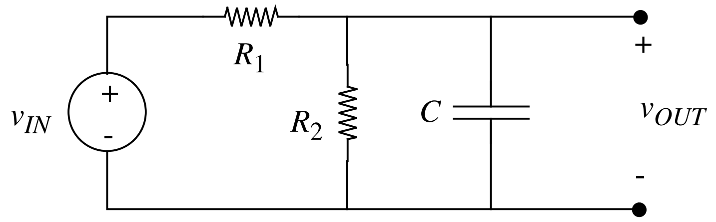

Figure 3: network for Pre-Lab Exercises 2-4 and 2-5.

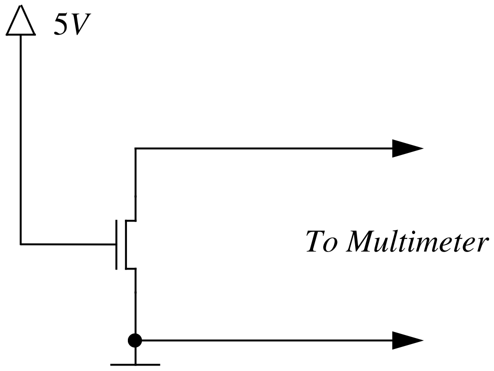

Figure 4: circuit to measure R_{ON}.

the other side is on a separate trace. You should use two switch packs because the three gates you build in In-Lab Exercises 2-2 through 2-4 involve a total of five input signals. The resistor pack can be inserted into the protoboard along side the switch packs so that separate resistors connect to each switch. Finally, the common pin of the resistor pack can be connected to the 5 V power supply through a single wire.

(2-3) Construct the NOR gate from Figure 1. As for the NOT gate shown in Figure 5, connect the inputs to the NOR gate to switches and 10 kΩ resistors. For all combinations of switch positions, that is for all combinations of logic input levels to the gate, measure v_{OUT} with the multimeter. *Save the NOR gate for In-Lab Exercise 2-5.*

(2-4) Repeat In-Lab Exercise 2-3 for the NAND gate. *Save the NAND gate for In-Lab Exercise 2-5.*

(2-5) Modify your existing NOT, NOR, and NAND gates to implement the combinational logic circuit of Figure 2, as outlined in Pre-Lab Exercise 2-3. Ensure that each of the three inputs to the logic circuit are connected to a switch and resistor in the manner of In-Lab Exercises 2-2 through 2-4. You may opt to use the three remaining switches in the switch packs for this purpose. For all eight combinations of switch positions, that is for all combinations of logic input levels to the gates, measure v_{OUT} with the multimeter. The measurements should demonstrate that the logic circuit functions properly.

At this point, remove two MOSFETs and a 1 kΩ resistor from your logic circuit so they can be used in the following exercises. The next three exercises will analyze the delay of the MOSFET amplifier when it is used as a digital logic inverter.

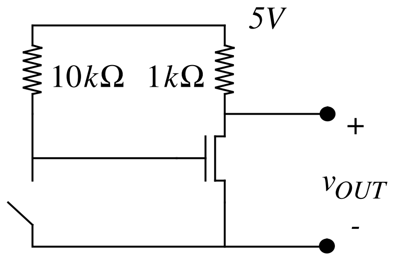

Figure 5: experimental NOT gate.

(2-6) The first step is to measure the threshold voltage of a MOSFET. Use the method of Lab 1 In-Lab Exercise 1-4. We will designate this particular MOSFET as “M” in In-Lab Exercises 2-7 and 2-8.

(2-7) Since the delay of an inverter is related to the capacitance of the node that is driven by its output, this exercise measures the capacitance seen by the output of an inverter that is driving the gate of a MOSFET. First, construct the circuit shown in Figure 6. You will measure the capacitance C_P seen at node P in the circuit. C_P is the capacitance at node P, and includes C_{GS}, the gate capacitance of MOSFET M, in parallel with the oscilloscope input capacitance and a parasitic wiring capacitance. Set the signal generator to produce a 20-kHz square wave with an amplitude of 5 V peak-to-peak and an offset of 2.5 V. Channel #2 of the oscilloscope should display both a first-order rising step response and a first-order falling step response. Measure the time constant of the rising step response (i.e., the time from 0 to 3.16 V). Since the on resistance of the MOSFET is very small, the falling response has a very small time constant that is difficult to measure. Therefore, we will focus on the rising step response.

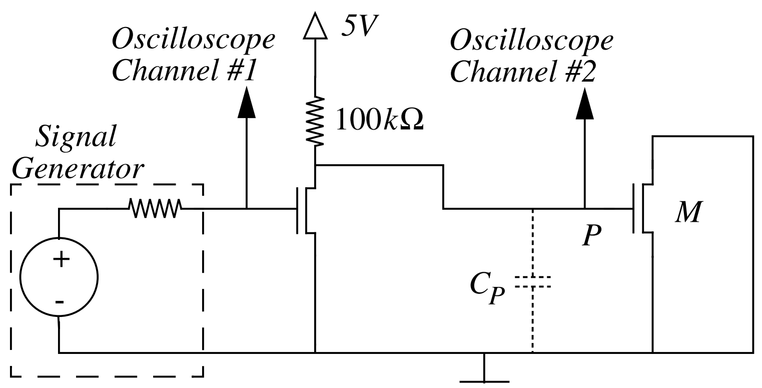

Figure 6: measuring the gate-to-source capacitance of a MOSFET amplifier.

(2-8) This exercise measures the delay of the MOSFET amplifier when it is used as a digital logic inverter. Construct the circuit shown in Figure 7; As in the previous exercise, set the signal generator to produce a 20-kHz square wave with an amplitude of 5 V peak-to-peak and an offset of 2.5 V. Finally, use the oscilloscope to measure the delay from the time at which the signal generator switches low (Channel #1) to the time at which the inverter pair output (Channel #2) begins to switch low. (Note that a high to low transition of the signal generator corresponds to a rising transition at the node P).

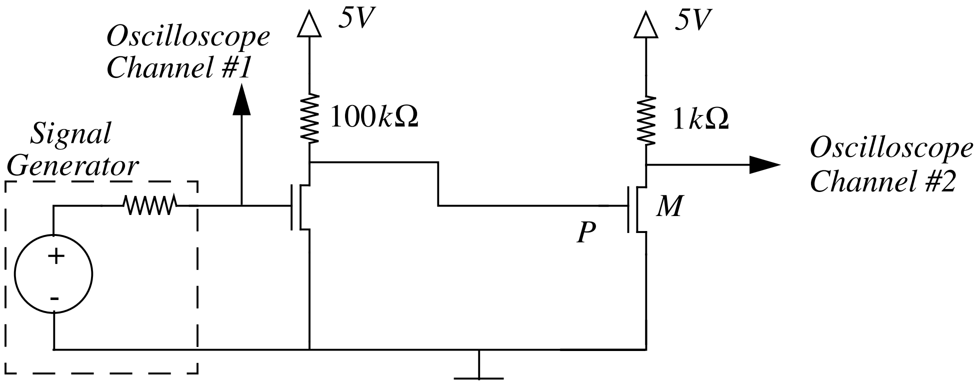

Figure 7: measuring the delay of a MOSFET amplifier when it is used as a digital logic gate.

Post-Lab Exercises

(2-1) Using the values of R_{ON} measured during In-Lab Exercise 2-1, re-calculate the output voltages for each gate in the manner of Pre-Lab Exercise 2-1. Explain any discrepancies between the re-calculated output voltages and those measured during In-Lab Exercises 2-2 through 2-4.

(2-2) Figure 3 models the behavior of node P in Figure 6 when the MOSFET of the first inverter stage is off: R_1 is the 100 kΩ resistor; R_2 models the oscilloscope input resistance and C models C_P. Recall C_P is the capacitance of node P, and includes C_{GS}, the gate capacitance of MOSFET M, in parallel with the oscilloscope input capacitance and a parasitic wiring capacitance. Assume that the oscilloscope input resistance and capacitance are 100 MΩ and 10 pF, respectively. Combine the analysis of Pre-Lab Exercise 2-4 and the time constant measured in In-Lab Exercise 2-7 to determine the sum of C_{GS} and the parasitic wiring capacitance.

(2-3) The analysis of Pre-Lab Exercise 2-5 models the delay measured during In-Lab Exercise 2-8. Using the parameters computed in Post-Lab Exercise 2-2, and V_T measured in In-Lab Exercise 2-6, predict the delay and compare the prediction to the measurement. Note that the oscilloscope with its input resistance and capacitance were not connected to the MOSFET gate at node P when the delay was measured; see Figure 7.