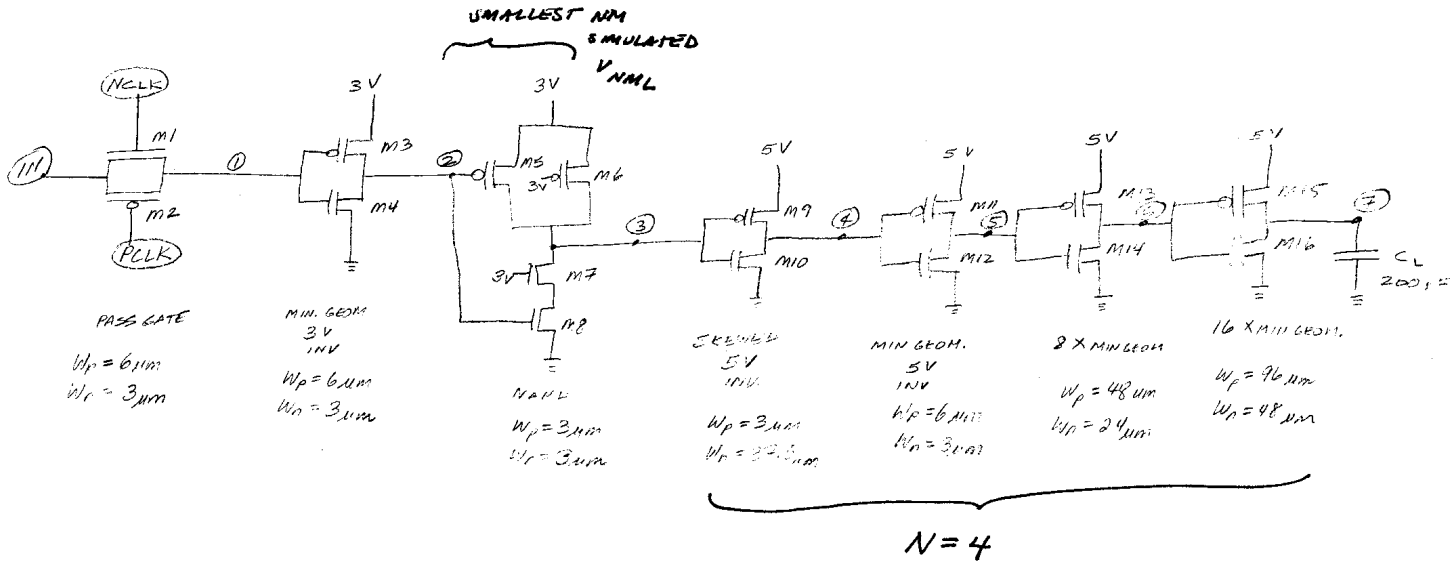
SPECIFICATION	YOUR DESIGN
N (number of inverters at output stage)	46 (INCLUDING NAND GATE) TOTAL

PARAMETER	SPECIFICATION	YOUR CALCULATED VALUE	YOUR SIMULATED VALUE
OUTPUT t_r	< 200 ns	0.5 ns*	90 ns
OUTPUT t_f	< 200 ns	0.5 ns*	100 ns
t_{pd0}	< 400 ns	37 ns	30 ns
t_{pd1}	< 400 ns	37 ns	30-40 ns
Average power dissipation	< 1 mW	0.8 mW	0.6 mW
Minimum Noise Margin	> 1.0 Volt	1.4 V (3V inverter)	1.1 V (NAND)

FINAL DES · (Summary of Results)

Notes: (1) Node labels correspond to SPICE scripts.
(2) $L_n = L_p = 1.5\mu m$ for all devices
(3) Device labels correspond to SPICE scripts



Design Project- Row Driver : Abstract

A row selection driver using dynamic registers to reduce the number of transistors needed to select a row line was implemented. The design constraints were a delay of less than 400 ns after clock edge, rise and fall times less than 200 ns, and total average power dissipation for all 1024 drivers less than 1mW within the period of a frame update rate of 75 Hz . An unspecified area constraint was also stated. The driver, consisting of a pass gate, NAND gate, and CMOS inverters, was designed using 3 V and 5 V NMOS and PMOS devices. The design approach was based on attaining the best timing performances and scaling back devices to achieve power and/or size constraints. Hand calculations were made with this time approach in mind and SPICE simulation was performed for the latter power and size considerations. In instances where inverters are removed, the correct logic function was kept in check my maintaining that the number of inversions be even. The final design which removed two output buffer inverters and rescaled one output buffer inverter from the original hand calculations met and in many cases exceeded the performance requirements with rise/fall times around 100 ns, delays of 30-40 ns, and power dissipation only slightly above half a mW.

Notes on the design approach:
The basic approach to design the row driver was to begin with an architectural view of the circuit design. Following from the RS input to the capacitive load of 200 pF, we know that the driver need a pass gate follow by an inverter and then a NAND gate. This has been already provided for us. After the NAND gate, there maybe N inverters. The main challenges are as follows: (1) to be able to charge and discharge the load capacitance (plus parasitics) within 200 ns; (2) to supply an output of 0 to 5 V when our input signal RS is limited to 0 to 3 V; (3) to minimize the delay between the input RS and output signal to less than 400 ns; and (4) to dissipate less than 1 mW power within the 75 Hz frame update rate for all 1024 drivers combined.

We attacked first the timing constraints. For a mimimum geometry 5 V inverter that is symmetrical feeding another minimum geometry 5 V symmetrical inverter, we found that the time delay for 50% charge/discharge is about 0.5 ns. In addition for such a setup, the load capacitance at the 1st 5V inverter due to its drain to bulk depletion capacitance and the capacitance of the gate of the following inverter, is quite small at around 58 fF. Thus making the 200 pF load capacitance be more than 3000 times larger. As the time to charge/discharge is proportional to the capacitance being charged/discharged, we expect that approximately 3000*0.5ns=1500 ns would result if we use the minimum geometry inverter to connect directly with the 200 pF load. Therefore, to meet time requirements, we must employ buffers. By taking N roots of the capacitive ratio and realizing that N*roots*tmin gives the scaled delay (see page 6 of hand calc.), we select 4 buffers for 5 V inverters that are scaled 8 times at each stage. This approach gives about 16 ns delay from the minimum geometry 5 V to the output. As this value is small compared to the 400 ns and also realizing that the other devices could be at their minimum geometry for symmetry (except for the 1st 5V inverter), we approximate that the minimum delay per inverter or gate is 1 ns and that for the buffers we recalculate with this assumption and get a total delay of about 37 ns (see "Rough Estimates" spreadsheet). As this is small and most devices are symmetrical (by design selection of Wp=2*Wn for inverters and Wp=Wn for NAND gate), we assume that the delays for low-to-high is the same as high-to-low. The big assumptions of symmetry is actually a design choice. Symmetry facilitates the determination of Vm and noise margins and as such, we choose symmetry for all our circuits except the 1st 5V inverter which necessarily must be skewed so that a 3V high input could safely generate a logic low signal output. To simplify the driver design flow, we place a skewed 5 V inverter in between the NAND gate and the 5 V minimum geometry inverter. For the the NAND gate and the logic preceding it, we choose to supply with 3V. Therefore the pass gate then inverter then NAND would all take supply from 3V. With the VDD and the dimensions and number of inverters determined, we could go through and calculate the load capacitances due to each input/output nodes. We then take this capacitance at each stage and multiply by VDD squared and the update rate so that we could roughly get the average power dissipation (see "Rough Calc."). This then gives us roughly 0.8 mW of dissipation. The last rough calculation is for rise/fall time which is just the minimum geometry 5 V's times. By using scaling with the buffers, the times are ridiculously low at 0.5 ns.

The hand calculations provided us with a circuit to model in SPICE. The results of the 1st several simulations show a need for optimization. The time delays and rise/fall time were tremendously lower than spec. Re-examination of the device size selected, we realize that the 2 last buffers had sizes that were too big! and thus they were removed and then the remaining buffers were rescaled approriately (letting the delays increased so that the area could be minimized.

What follows are the plots of the noise margins for the final circuit devices. The lowest noise margin came out to be for the NAND gate. NAND gate NM calculations are not provided by the text and a rough attempt at hand calculations was made. Then, the SPICE code for transient analysis along with performances follow. The DC sweeps use on DC input voltage that is moved from one gate node to the next for noise margin of each device. The hand calculations that follows are mainly to calculate NMs and CL per stage. The time calculations were already mentioned with rough cal. spreadsheet. Minor attempts were made to calculate ID but for th most part it did not seem worthwhile knowing the hand calculated values for the current.

Rough Estimates for Power,Delay and Rise/Fall Time given the CL values and minimum delays from the attached hand calculations

Total Power Dissipation

f		75 Hz	
CL	VDD	P=CL*VDD*VDD*f	
6.40E-14	3	4.32E-11	
5.75E-14	3	3.88E-11	
1.89E-13	3	1.28E-10	
8.90E-14	5	1.67E-10	
2.75E-13	5	5.16E-10	
2.13E-12	5	3.99E-09	
1.69E-11	5	3.17E-08	
1.36E-10	5	2.54E-07	
2.66E-10	5	4.99E-07	
	sum	7.89E-07 W	
	X1024 rows	8.08E-04 W	(Assume I_D static of 5V skewed inv. inverter $\neq 0$) by design $V_{IH} < V_{OH}$ (see plots)

Propagational Delay

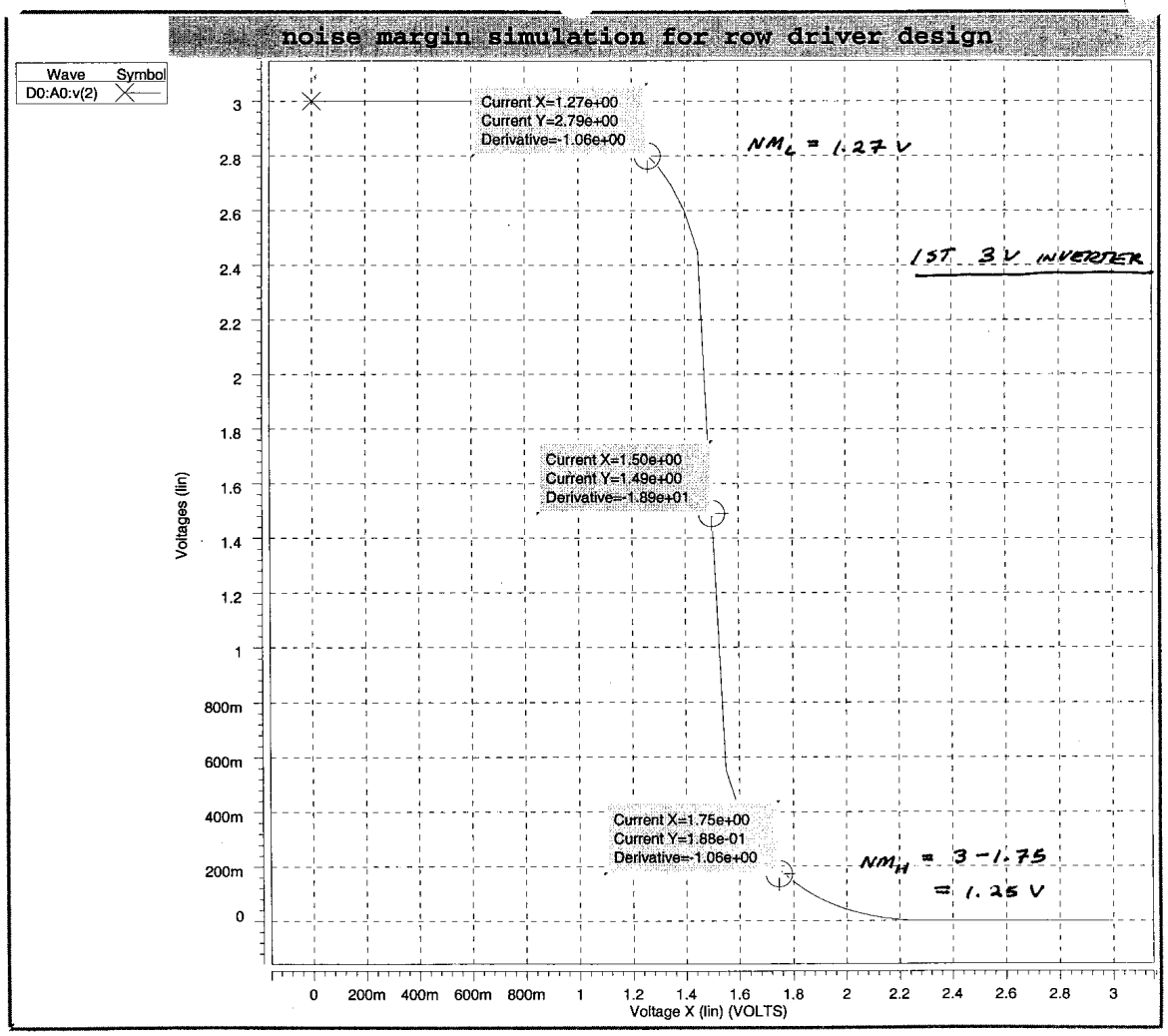
With minimum geometry tpHL=tpLH=0.5 ns << 400 ns, roughly
calculate delays by summation of devices by assuming tdelaymin=1ns

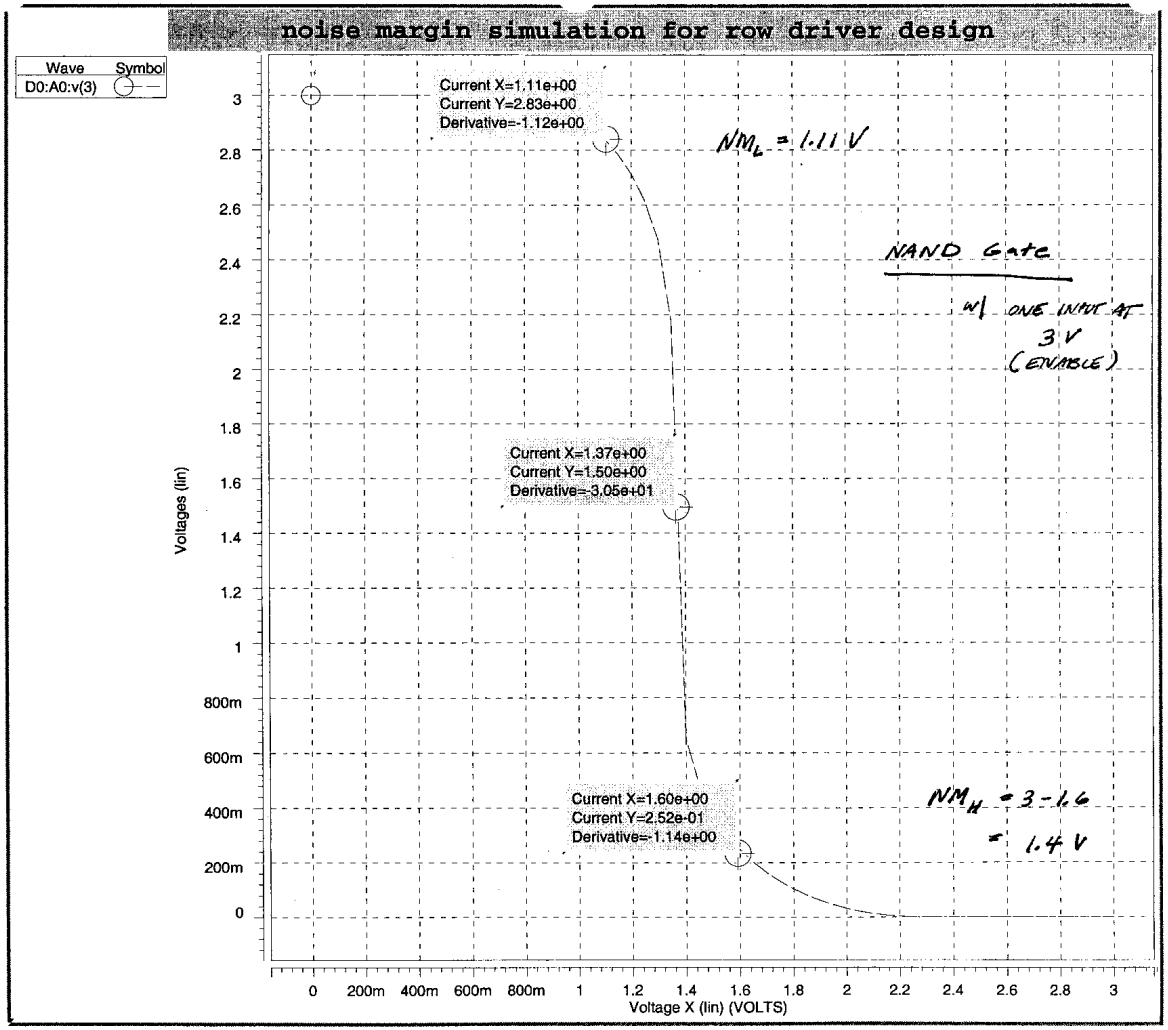
DEVICE	delay
pass gate	1
3 V Inv	1
NAND	1
5 V Inv (skewed Vm)	1
min geom. 5 V inv	1
4 buffers	32
total delay	37 ns
for both tpD1 & tpD0	

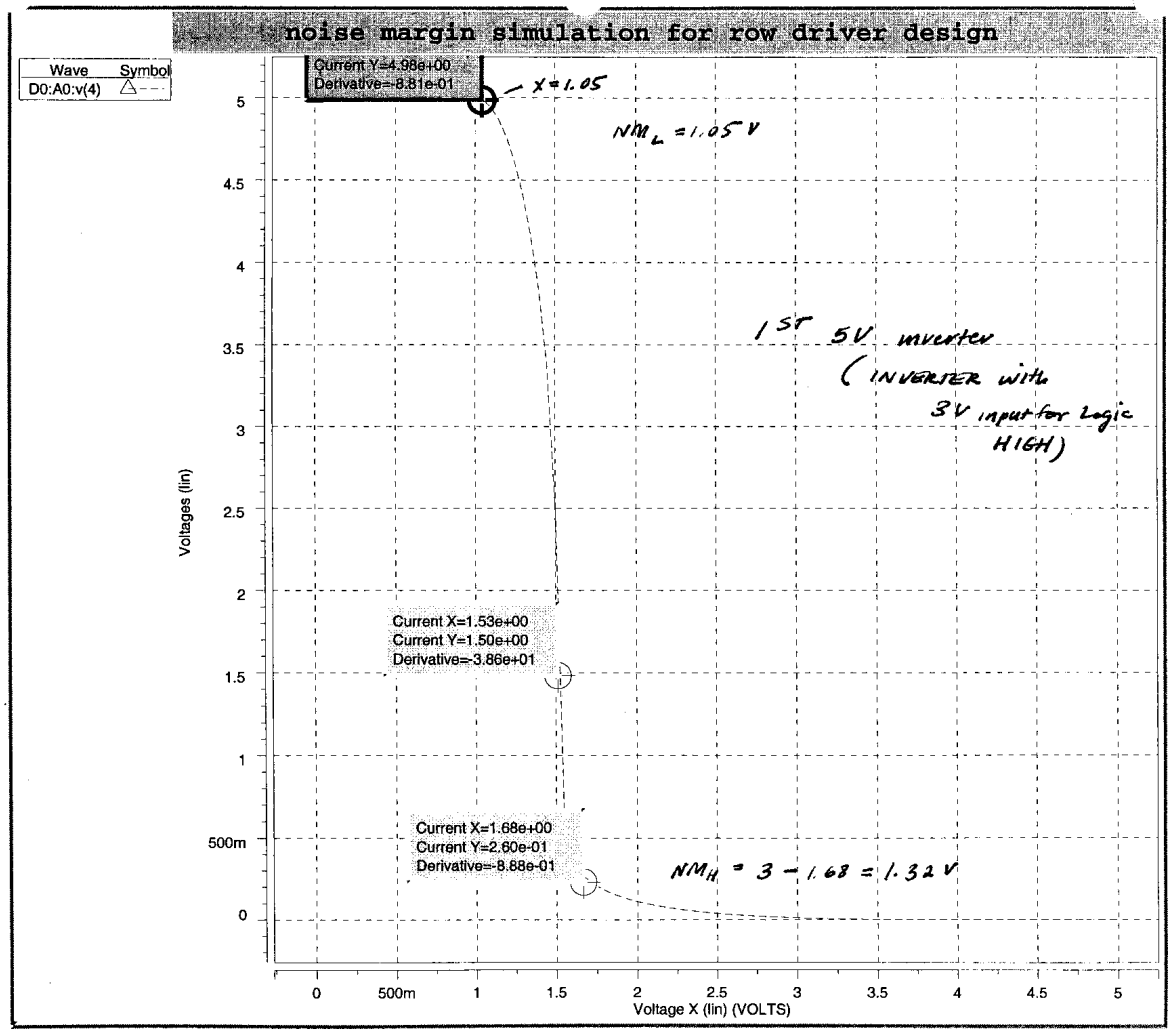
Rise/Fall Time

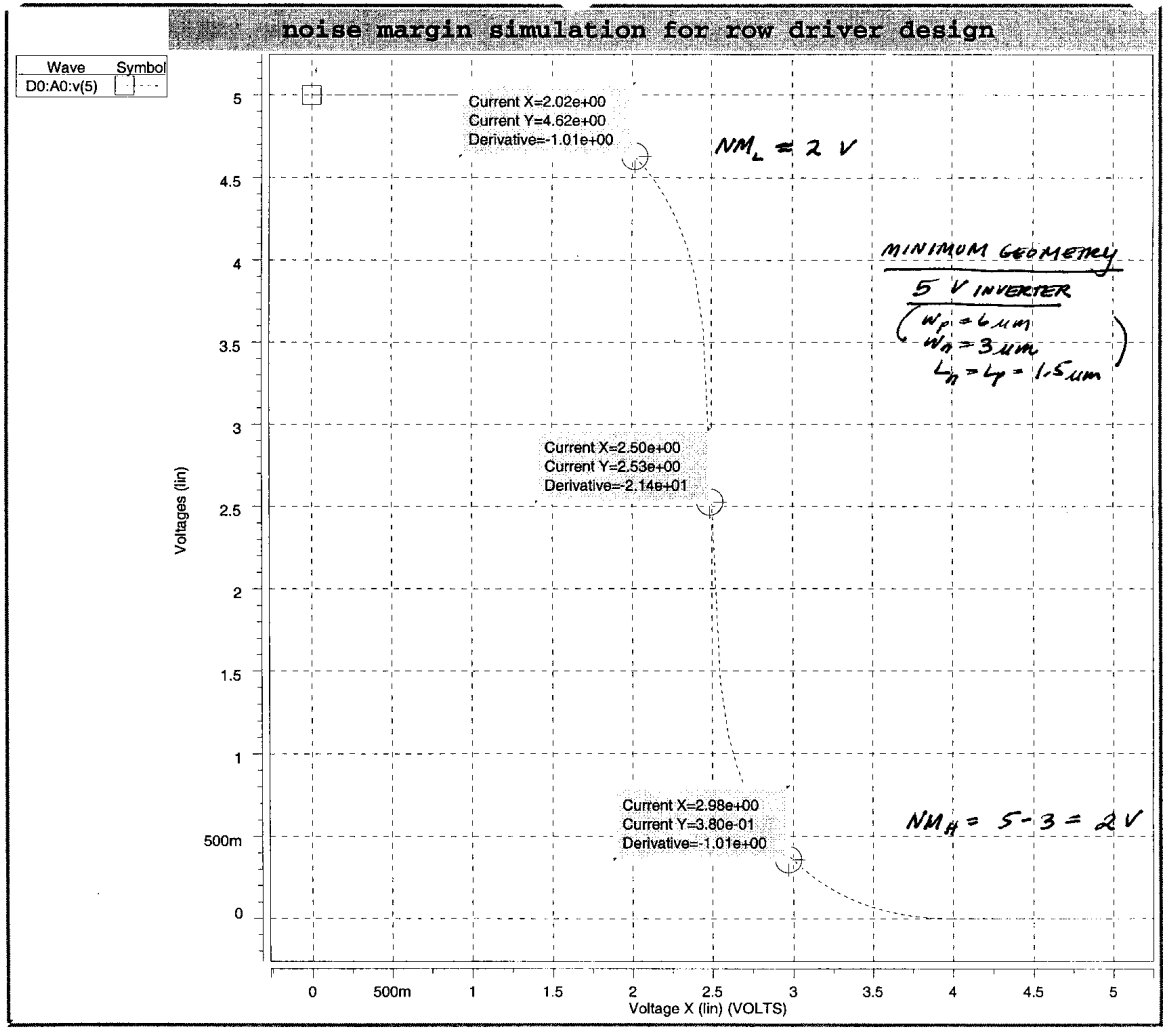
With CL=200 pF (actually calculated to 266 pF when including CP)
t=CL*0.8VDD/ID
with VDD=5V , 0.8 for the 90%-10% and assuming linear charge/discharge

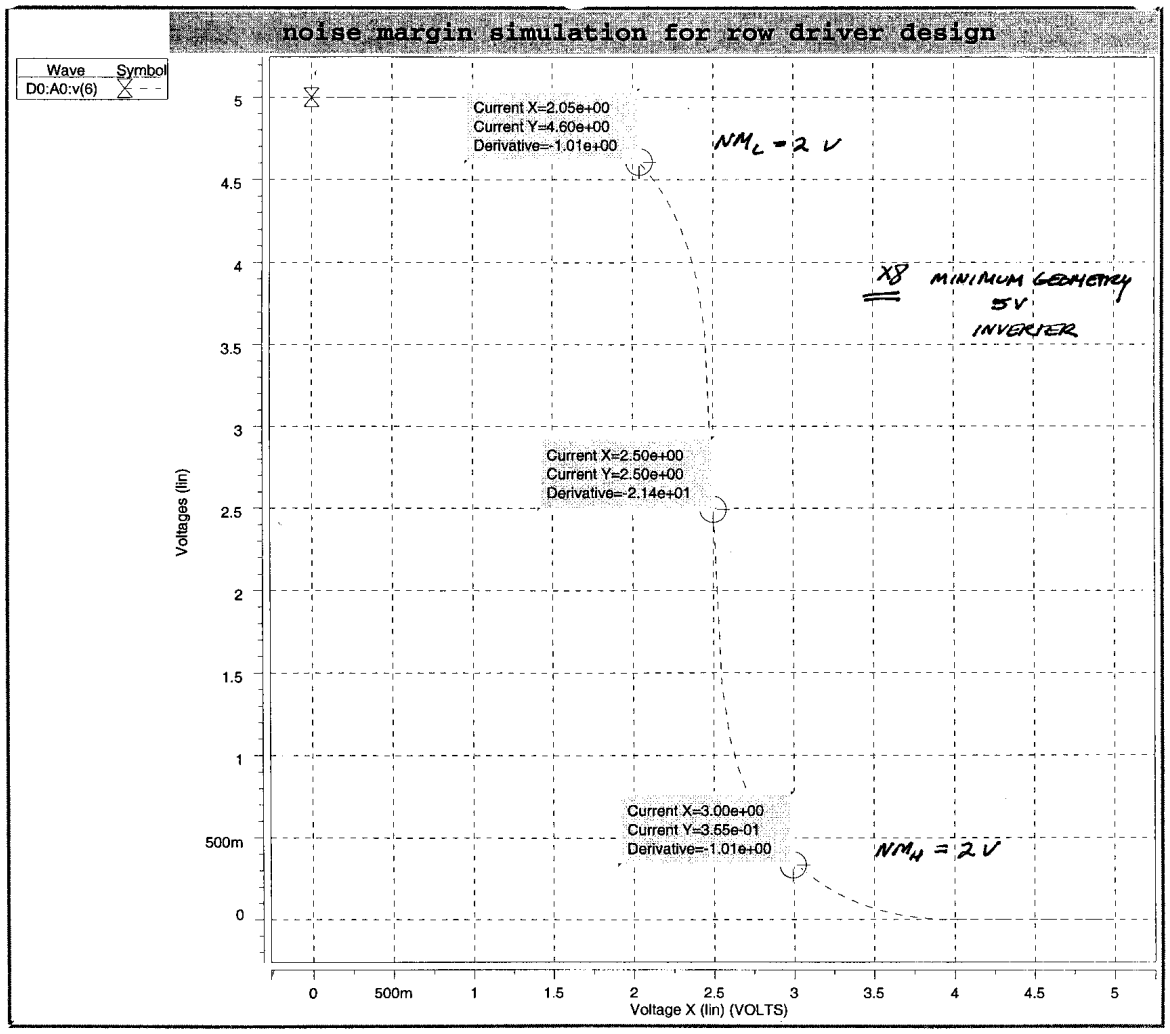
ID	1.6384
t=CL*0.8VDD/ID	4.8828E-10 s

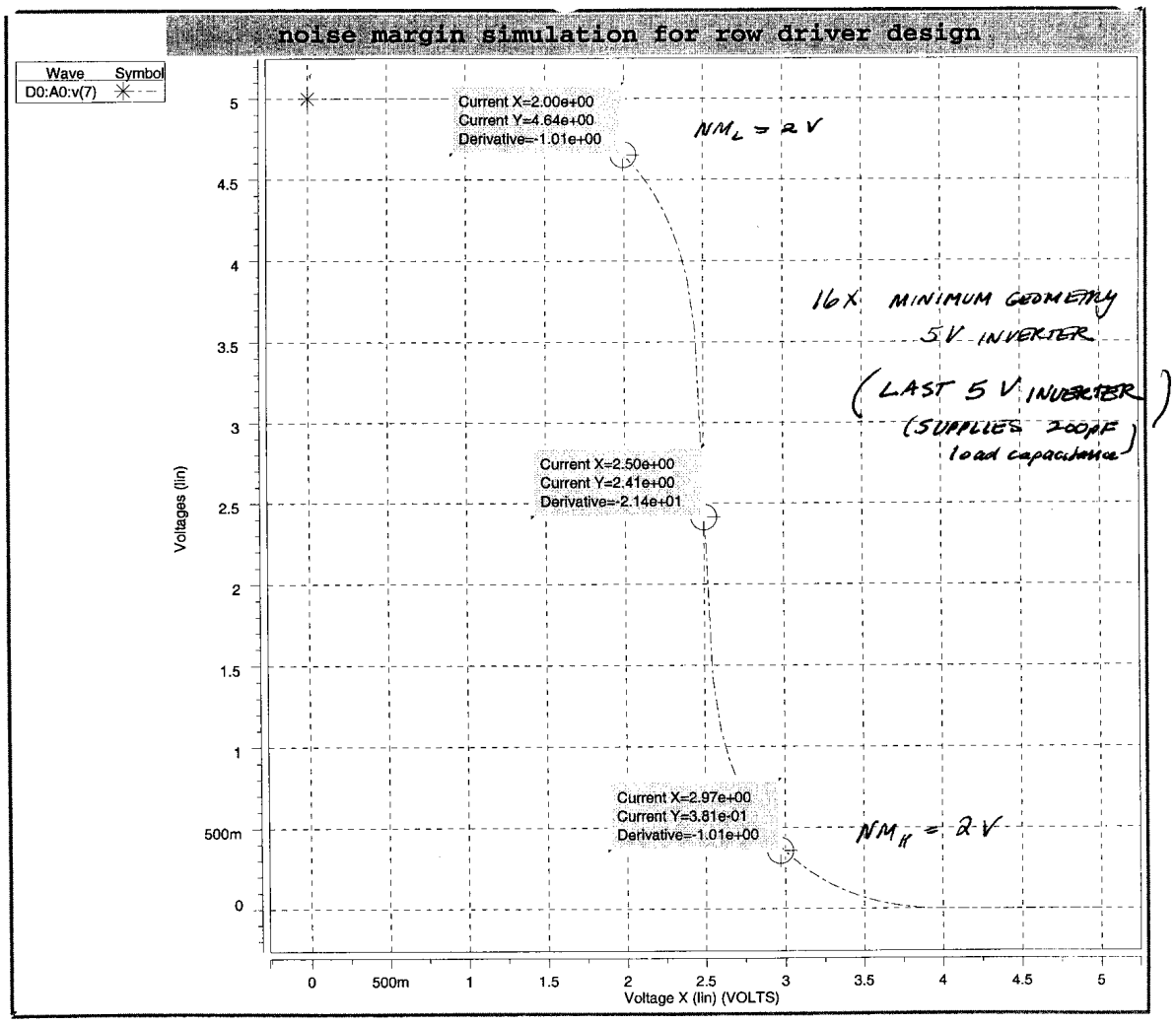

noise margin simulation for row driver design
Wave Symbol
D0:A0:v(2)
Current X=1.27e+00
Current Y=2.79e+00
Derivative=-1.06e+00
NM_L = 1.27 V
1ST 3V INVERTER
Current X=1.50e+00
Current Y=1.49e+00
Derivative=-1.89e+01
Current X=1.75e+00
Current Y=1.88e-01
Derivative=-1.06e+00
NM_H = 3 - 1.75
= 1.25 V
Voltages (lin)
Voltage X (lin) (VOLTS)
0
200m
400m
600m
800m
1
1.2
1.4
1.6
1.8
2
2.2
2.4
2.6
2.8
3


noise margin simulation for row driver design
Wave Symbol
D0:A0:v(3)
Current X=1.11e+00
Current Y=2.83e+00
Derivative=-1.12e+00
NM_L = 1.11 V
NAND Gate
w/ one input at 3 V (enable)
Current X=1.37e+00
Current Y=1.50e+00
Derivative=-3.05e+01
Current X=1.60e+00
Current Y=2.52e-01
Derivative=-1.14e+00
NM_H = 3 - 1.6 = 1.4 V
Voltages (lin)
Voltage X (lin) (VOLTS)
0
200m
400m
600m
800m
1
1.2
1.4
1.6
1.8
2
2.2
2.4
2.6
2.8
3


noise margin simulation for row driver design
Wave Symbol
D0:A0:v(4)
Current Y=4.98e+00
Derivative=-8.81e-01
X=1.05
NM_L = 1.05 V
1ST 5V inverter
(INVERTER with
3V input for Logic
HIGH)
Current X=1.53e+00
Current Y=1.50e+00
Derivative=-3.86e+01
Current X=1.68e+00
Current Y=2.60e-01
Derivative=-8.88e-01
NM_H = 3 - 1.68 = 1.32 V
Voltages (lin)
Voltage X (lin) (VOLTS)
0
500m
1
1.5
2
2.5
3
3.5
4
4.5
5


noise margin simulation for row driver design
Wave
Symbol
D0:A0:v(5)
Current X=2.02e+00
Current Y=4.62e+00
Derivative=-1.01e+00
NM_L = 2 V
MINIMUM GEOMETRY
5 V INVERTER
(W_p = 6 μm
W_n = 3 μm
L_n = L_p = 1.5 μm)
Current X=2.50e+00
Current Y=2.53e+00
Derivative=-2.14e+01
Current X=2.98e+00
Current Y=3.80e-01
Derivative=-1.01e+00
NM_H = 5 - 3 = 2 V
Voltages (lin)
Voltage X (lin) (VOLTS)
0
500m
1
1.5
2
2.5
3
3.5
4
4.5
5


noise margin simulation for row driver design
Wave Symbol
D0:A0:v(6)
Current X=2.05e+00
Current Y=4.60e+00
Derivative=-1.01e+00
NM_L = 2 V
X8 MINIMUM GEOMETRY 5V INVERTER
Current X=2.50e+00
Current Y=2.50e+00
Derivative=-2.14e+01
Current X=3.00e+00
Current Y=3.55e-01
Derivative=-1.01e+00
NM_H = 2 V
Voltages (lin)
5
4.5
4
3.5
3
2.5
2
1.5
1
500m
0
0
500m
1
1.5
2
2.5
3
3.5
4
4.5
5
Voltage X (lin) (VOLTS)


noise margin simulation for row driver design
Wave Symbol
D0:A0:v(7)
Current X=2.00e+00
Current Y=4.64e+00
Derivative=-1.01e+00
Current X=2.50e+00
Current Y=2.41e+00
Derivative=-2.14e+01
Current X=2.97e+00
Current Y=3.81e-01
Derivative=-1.01e+00
Voltages (lin)
Voltage X (lin) (VOLTS)
0
500m
1
1.5
2
2.5
3
3.5
4
4.5
5
NM_L = 2 V
NM_H = 2 V
16X MINIMUM GEOMETRY
5V INVERTER
(LAST 5 V INVERTER
(SUPPLIES 200fF
load capacitance)

filename : nm_project1.sp

MTL's

/home[redacted]

```
Noise Margin Simulation for Row Driver Design
.OPTIONS POST
.OP
*M1 IN NCLK 1 0 NCH3 L=1.5U W=3U AD=18P AS=18P PD=15U PS=15U
*M2 IN PCLK 1 VCC3 PCH3  L=1.5U W=6U AD=36P AS=36P PD=18U PS=18U
*M3 2 1 VCC3 VCC3 PCH3 L=1.5U W=6U AD=36P AS=36P PD=18U PS=18U
*M4 2 1 0 0 NCH3 L=1.5U W=3U AD=18P AS=18P PD=15U PS=15U
*M5 3 2 VCC3 VCC3 PCH3  L=1.5U W=3U AD=18P AS=18P PD=15U PS=15U
*M6 3 VCC3 VCC3 VCC3  PCH3  L=1.5U W=3U AD=18P AS=18P PD=15U PS=15U
*M7 3 VCC3 10 0 NCH3  L=1.5U W=3U AD=18P AS=18P PD=15U PS=15U
*M8 10 2 0 0 NCH3  L=1.5U W=3U AD=18P AS=18P PD=15U PS=15U
*M9 4 3 VCC5 VCC5 PCH5  L=1.5U W=3U AD=18P AS=18P PD=15U PS=15U
*M10 4 3 0 0 NCH5 L=1.5U W=37.5U AD=225P AS=225P PD=49.5U PS=49.5U
*M11 5 4 VCC5 VCC5 PCH5 L=1.5U W=6U AD=36P AS=36P PD=18U PS=18U
*M12 5 4 0 0 NCH5 L=1.5U W=3U AD=18P AS=18P PD=15U PS=15U
*M13 6 5 VCC5 VCC5 PCH5 L=1.5U W=48U AD=288P AS=288P PD=60U PS=60U
*M14 6 5 0 0 NCH5 L=1.5U W=24U AD=144P AS=144P PD=36U PS=36U
M15 7 6 VCC5 VCC5 PCH5 L=1.5U W=96U AD=576P AS=576P PD=108U PS=108U
M16 7 6 0 0 NCH5 L=1.5U W=48U AD=288P AS=288P PD=60U PS=60U
VCC3 VCC3 0 DC 3
VCC5 VCC5 0 DC 5
VIN 5 0 DC 0
.DC VIN 0 5 0.05
.MODEL PCH5 PMOS LEVEL=1 VTO=-1 KP=25E-6 LAMBDA=7E-2 CJ=3E-4 CJSW=3.5E-10
+PB=0.9 TOX=1.5E-8
.MODEL NCH5 NMOS LEVEL=1 VTO=1 KP=50E-6 LAMBDA=7E-2 CJ=1E-4 CJSW=5E-10
+PB=0.9 TOX=1.5E-8
*.MODEL PCH3 PMOS LEVEL=1
*.MODEL NCH3 NMOS LEVEL=1
.MODEL PCH3 PMOS LEVEL=1 VTO=-0.7 KP=25E-6 LAMBDA=7E-2 CJ=3E-4 CJSW=3.5E-10
+PB=0.9 TOX=1.5E-8
.MODEL NCH3 NMOS LEVEL=1 VTO=0.7 KP=50E-6 LAMBDA=7E-2 CJ=1E-4 CJSW=5E-10
+PB=0.9 TOX=1.5E-8
.END
```

moves node to node per interested inverter.

filename : tr_project1.sp

~~Noise Margin~~ Transient Simulation for Row Driver Design mtz /home/[redacted]/spice/6.012

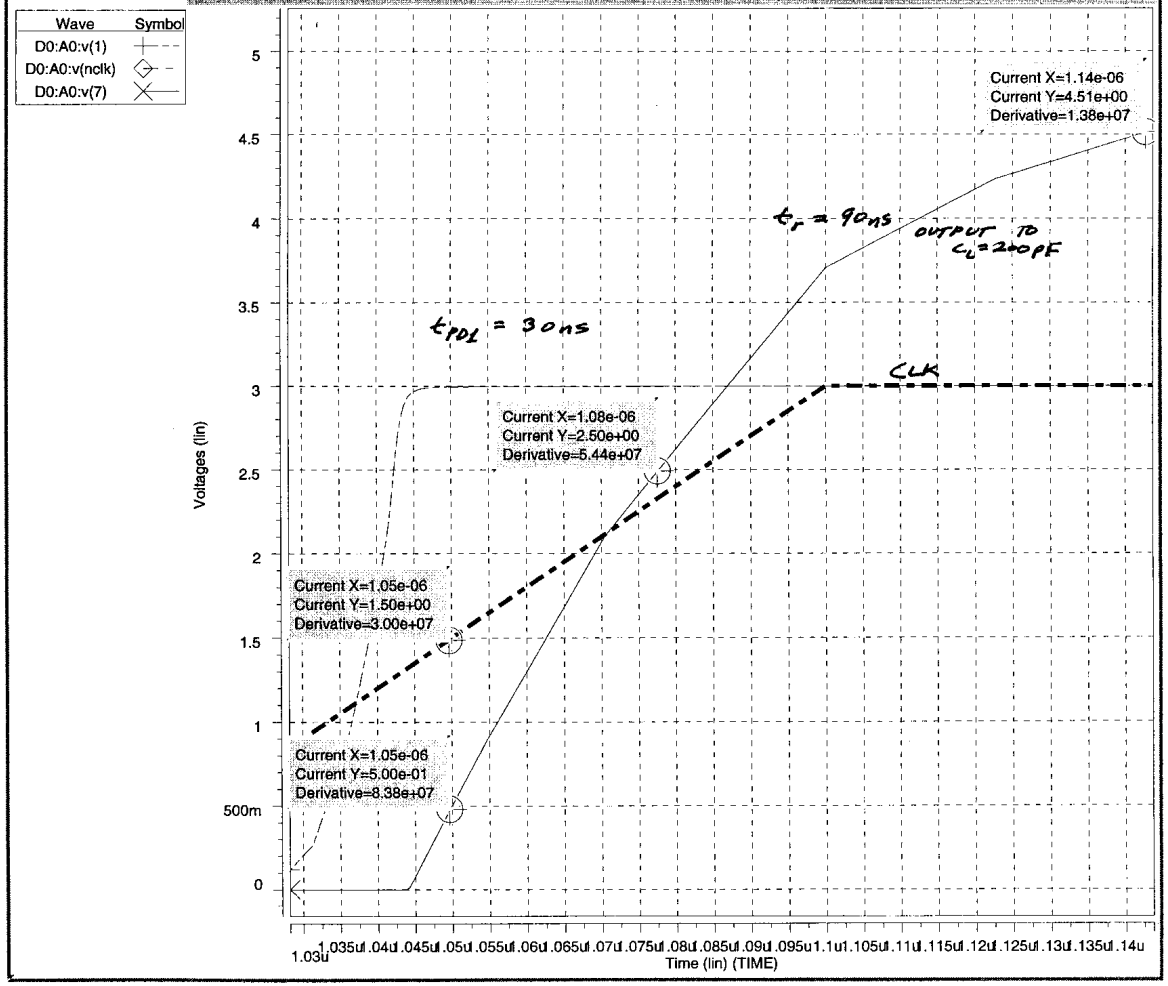
```
.OPTIONS LIST NODE POST
.TRAN 10n 13.33M
*.PRINT TRAN V(IN) V(9)
   'ASURE TRAN PDISS AVG POWER FROM=0N TO 13.33M
1.  IN NCLK 1 0 NCH3 L=1.5U W=3U AD=18P AS=18P PD=15U PS=15U
M2  IN PCLK 1 VCC3 PCH3  L=1.5U W=6U AD=36P AS=36P PD=18U PS=18U
M3  2 1 VCC3 VCC3 PCH3 L=1.5U W=6U AD=36P AS=36P PD=18U PS=18U
M4  2 1 0 0 NCH3 L=1.5U W=3U AD=18P AS=18P PD=15U PS=15U
M5  3 2 VCC3 VCC3 PCH3  L=1.5U W=3U AD=18P AS=18P PD=15U PS=15U
M6  3 VCC3 VCC3 VCC3  PCH3  L=1.5U W=3U AD=18P AS=18P PD=15U PS=15U
M7  3 VCC3 10 0 NCH3  L=1.5U W=3U AD=18P AS=18P PD=15U PS=15U
M8  10 2 0 0 NCH3  L=1.5U W=3U AD=18P AS=18P PD=15U PS=15U
*MA 11 3 VCC3 VCC3 PCH3 L=1.5U W=6U AD=36P AS=36P PD=18U PS=18U
*MB 11 3 0 0 NCH3 L=1.5U W=3U AD=18P AS=18P PD=15U PS=15U
M9  4 3 VCC5 VCC5 PCH5  L=1.5U W=3U AD=18P AS=18P PD=15U PS=15U
M10 4 3 0 0 NCH5 L=1.5U W=37.5U AD=225P AS=225P PD=49.5U PS=49.5U
M11 5 4 VCC5 VCC5 PCH5 L=1.5U W=6U AD=36P AS=36P PD=18U PS=18U
M12 5 4 0 0 NCH5 L=1.5U W=3U AD=18P AS=18P PD=15U PS=15U
M13 6 5 VCC5 VCC5 PCH5 L=1.5U W=48U AD=288P AS=288P PD=60U PS=60U
M14 6 5 0 0 NCH5 L=1.5U W=24U AD=144P AS=144P PD=36U PS=36U
M15 7 6 VCC5 VCC5 PCH5 L=1.5U W=96U AD=576P AS=576P PD=108U PS=108U
M16 7 6 0 0 NCH5 L=1.5U W=48U AD=288P AS=288P PD=60U PS=60U
*M15 7 6 VCC5 VCC5 PCH5 L=1.5U W=384U AD=2304P AS=2304P PD=396U PS=396U
*M16 7 6 0 0 NCH5 L=1.5U W=192U AD=1152P AS=1152P PD=204U PS=204U
*M17 8 7 VCC5 VCC5 PCH5 L=1.5U W=3072U AD=18432P AS=18432P PD=3084U PS=3084U
*M18 8 7 0 0 NCH5 L=1.5U W=1536U AD=9216P AS=9216P PD=1548U PS=1548U
*M19 9 8 VCC5 VCC5 PCH5 L=1.5U W=24576U AD=147456P AS=147456P PD=24588U PS=24588
*M20 9 8 0 0 NCH5 L=1.5U W=12288U AD=73728P AS=73728P PD=12300U PS=12300U
C    7 0 200P
   J3 VCC3 0 DC 3
VCC5 VCC5 0 DC 5
V_RS IN 0 0 PULSE 0 3 0 100N 100N 6.5U 13.33M
V_CLK NCLK 0 0 PULSE 0 3 1U 100N 100N  3.055U 13.02U
V_INVCLK PCLK 0 0 PULSE 3 0 1U 100N 100N 3.055U 13.02U
.MODEL PCH5 PMOS LEVEL=1 VTO=-1 KP=25E-6 LAMBDA=7E-2 CJ=3E-4 CJSW=3.5E-10
+PB=0.9 TOX=1.5E-8
.MODEL NCH5 NMOS LEVEL=1 VTO=1 KP=50E-6 LAMBDA=7E-2 CJ=1E-4 CJSW=5E-10
+PB=0.9 TOX=1.5E-8
*.MODEL PCH3 PMOS LEVEL=1
*.MODEL NCH3 NMOS LEVEL=1
.MODEL PCH3 PMOS LEVEL=1 VTO=-0.7 KP=25E-6 LAMBDA=7E-2 CJ=3E-4 CJSW=3.5E-10
+PB=0.9 TOX=1.5E-8
.MODEL NCH3 NMOS LEVEL=1 VTO=0.7 KP=50E-6 LAMBDA=7E-2 CJ=1E-4 CJSW=5E-10
+PB=0.9 TOX=1.5E-8
.IC V(1)=0
.END
```

```
.***
noise margin simulation for row driver design
 ******  transient analysis                tnom=  25.000 temp=  25.000
******
  pdiss           =  5.6596E-07  from=  0.0000E+00     to=  1.3330E-02

        ***** job concluded
```

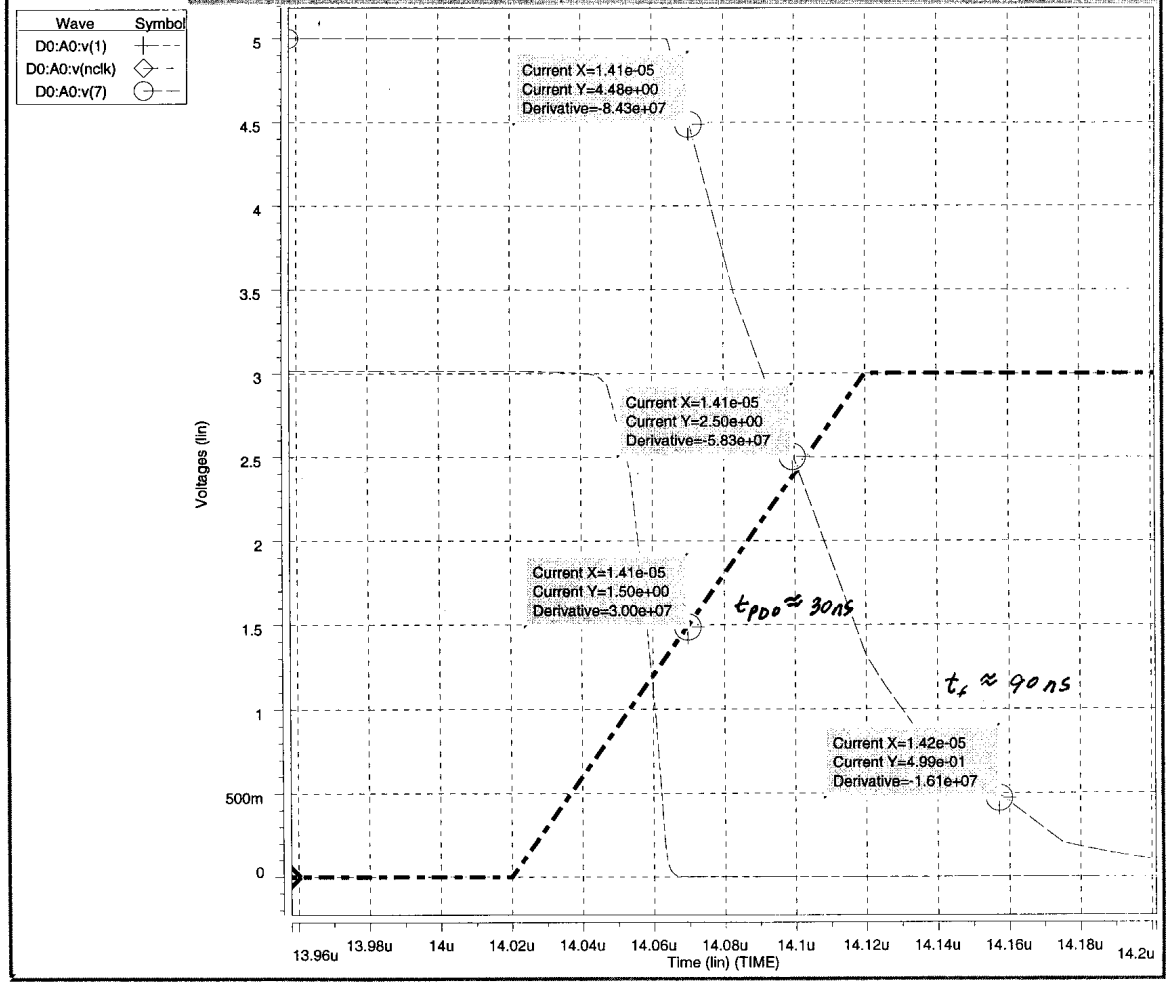
transient

noise-margin simulation for row driver design

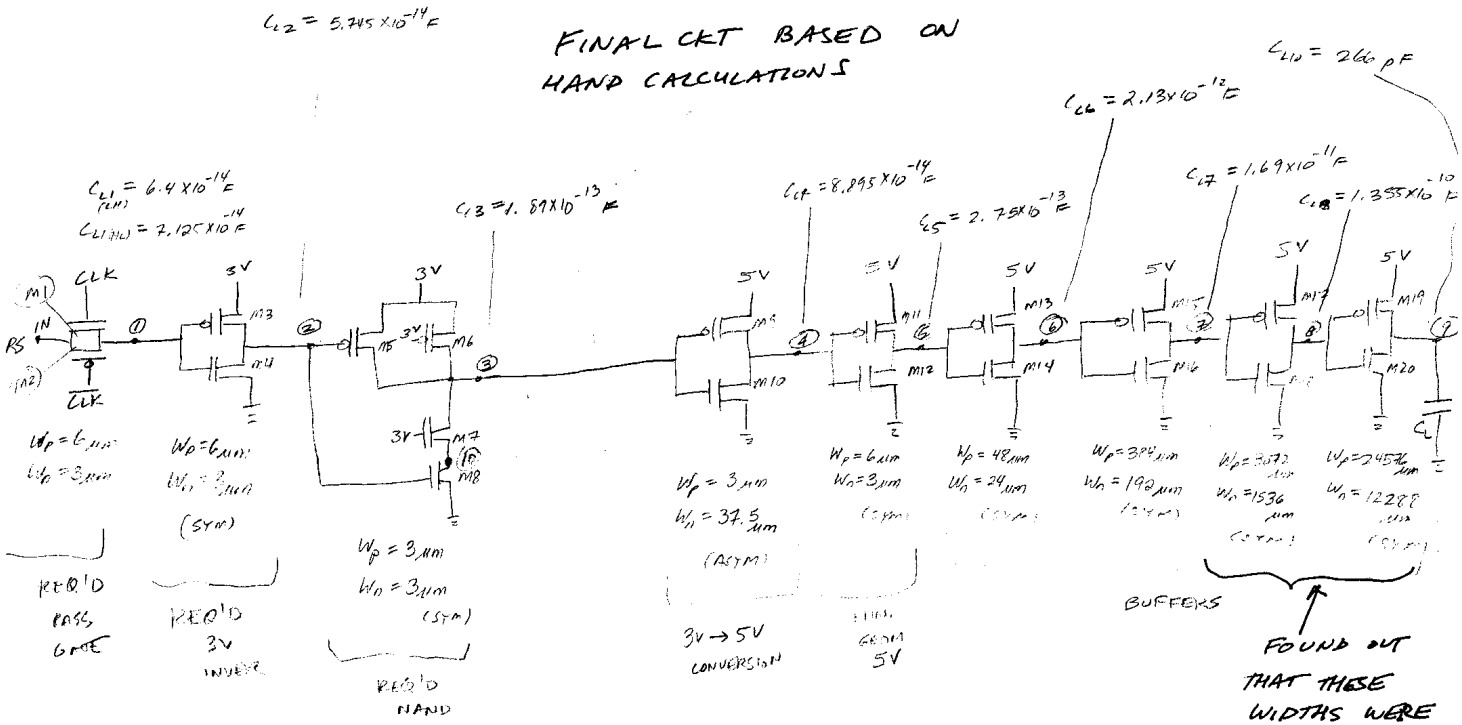


transient

~~noise-margin~~ simulation for row driver design



SUMMARY OF RESULTS FOR CALCULATIONS (PAGES 1 - 15)



Index of hand calculations:

(1) pages 1 – 9 calculation for min. geometry 5 V inverter + buffers

(2) pages 10 - 10A 5 V skewed inverter

(3) pages 11 - 15 calculation for 3V inverter, NAND gate, PASS gate

Select $W_p = 6\,\mu m$ so that $k_p = k_n$ and simplify hand calculations.
(TO MAKE PROPAGATION DELAY SYMMETRICAL)

GIVEN $L_n = 1.5\,\mu m = L_p$

$W_n = 3\,\mu m$

Select $W_p = 2W_n = 6\,\mu m$

$k_n = \left(\frac{W}{L}\right)_n \mu_n C_{ox}$, $k_p = \left(\frac{W}{L}\right)_p \mu_p C_{ox_p}$

$\left(\frac{W}{L}\right)_p = 2\left(\frac{W}{L}\right)_n$

with $\mu_n C_{ox_n} = KP_n = 50\times10^{-6}\,A/V^2$ (TABLE 1)

$\mu_p C_{ox_p} = KP_p = 25\times10^{-6}\,A/V^2$ (TABLE 1)

$KP_n = 2KP_p$

(1) $k_n = \left(\frac{W}{L}\right)_n \mu_n C_{ox_n}$, $k_p = \left(\frac{W}{L}\right)_p \mu_p C_{ox_p} = 2\left(\frac{W}{L}\right)_n \left(\frac{1}{2}\right)\mu_n C_{ox_n}$

$$\boxed{k_p = k_n}$$

setting $I_{Dn} = I_{DD}$

(2) $$V_M = \frac{V_{Tn} + \sqrt{\frac{k_p}{k_n}}\left(V_{DD} + V_{Tp}\right)}{1 + \sqrt{\frac{k_p}{k_n}}}$$

$V_{Tn} = 1\,V$; $V_{BS} = 0\,V$

$V_{Tp} = -1\,V$; $V_{SB} = 0\,V$

$V_{DD} = 5\,V$

$$V_M = \frac{V_{Tn} + \left(V_{DD} + V_{Tp}\right)}{1+1}$$

$$V_M = \frac{V_{DD}}{2} = \boxed{2.5\,V = V_M}$$

(3) $$g_{mn} = k_n\left(V_M - V_{Tn}\right) = \left(\frac{W}{L}\right)_n \mu_n C_{ox_n}\left(V_M - V_{Tn}\right)$$

$$= \left(\frac{3}{1.5}\right) 50\times10^{-6}\,\frac{A}{V^2}\left(2.5 - 1\right)V$$

$$g_{mn} = 150\times10^{-6}\,A/V = \boxed{150\times10^{-6}\,S = g_{mn}}$$

(4) $$I_{Dn} = \left(\frac{W}{2L}\right)_n \mu_n C_{ox_n}\left(V_M - V_{Tn}\right)^2\left(1 + \lambda_n V_M\right)\ ;\ \lambda_n = 7\times10^{-2}\,V^{-1}$$

$$= \left(\frac{3}{2(1.5)}\right) 50\times10^{-6}\,\frac{A}{V^2}\left(2.5 - 1V\right)^2\left(1 + 7\times10^{-2}\,\frac{1}{V}(2.5V)\right)$$

$$\boxed{I_{Dn} = 1.32\times10^{-4}\,A = -I_{DD}}$$

(5) $$r_{on} = \frac{1}{\lambda_n I_{Dn}} = \frac{1}{(7\times10^{-2}\,V^{-1})(1.32\times10^{-4}\,A)} = \boxed{1.08\times10^{5}\,\Omega = r_{on}}$$

(6) $g_{mp} = k_p (V_{DD} - V_m + V_{TP})$

$= \left(\frac{W}{L}\right)_p \mu_p C_{ox_p} (V_{DD} - V_m - V_{tp})$

$= \left(\frac{6}{1.5}\right)(25\times10^{-6}\ A/V^2)(5 - 2.5 - 1)\ V$

$g_{mp} = 150\times10^{-6}\ S = g_{mn}$ (makes sense since $k_n = k_p$ and $V_{DD} - V_m + V_{TP} = V_{DD} - V_m$)

(7) $r_{op} = \frac{1}{\lambda_p I_{DP}} = \frac{1}{(7\times10^{-2}\ V^{-1})(1.32\times10^{-4}\ A)} = 1.08\times10^5\ \Omega = r_{on}$

(again by $k_p = k_n$ + V_m symm.)

(8) $A_v = -(g_{mn} + g_{mp})(r_{on} \| r_{op})$ with $g_{mn} = g_{mp}$ $r_{on} = r_{op}$

$= (-2 g_{mn}) \frac{r_{on}}{2}$

$= -g_{mn} r_{on} = -(150\times10^{-6}\ S)(1.08\times10^5\ \Omega)$

$A_v = -16.2$

(9) $V_{IL} = V_m + \left(\frac{V_{out} - V_m}{A_v}\right) = 2.5 + \left(\frac{2.5}{-16.2}\right)$

$\boxed{V_{IL} = 2.34\ V}$

(10) $V_{IH} = V_m - \frac{V_m}{A_v} = 2.5 - \frac{2.5}{-16.2} = \boxed{2.65\ V = V_{IH}}$

(11) $NM_L = V_{IL} - V_{OL}$; $V_{OL} = 0\ V$ (APPROX.)

$\boxed{NM_L = V_{IL} = 2.35\ V} > 1\ V$ REQ.

(12) $NM_H = V_{OH} - V_{IH}$; $V_{OH} = 5\ V$ (APPROX.)

$\boxed{NM_H = 5 - 2.65 = 2.35\ V} > 1\ V$ REQ

(13) $t_{PHL} = \frac{C_L \Delta V}{I_D} = \frac{C_L \, V_{OH}/2}{\frac{k_n}{2}(V_{OH} - V_{TH})^2}$; $V_{OH} = V_{DD}$, $V_{TH} = 1V$, $k_n = \left(\frac{W}{L}\right)_n \mu_n C_{ox_n}$, need C_L

(14) $C_L = C_G + C_P$

Assume the 5V CMOS inverter drives another CMOS inverter of same type, that is, with $L_n = L_p$ AND $W_p = 2W_n$:

(15) $C_G = C_{ox_p}(WL)_p + C_{ox_n}(WL)_n$; $t_{ox_p} = t_{ox_n} = 1.5\times10^{-8}\,m = t_{ox}$

$= \frac{\varepsilon_{ox}}{t_{ox}} 2W_n L + \frac{\varepsilon_{ox}}{t_{ox}} W_n L$ $\quad W_p = 2W_n$, $L_p = L_n = L$

$= \frac{3\varepsilon_{ox} W_n L}{t_{ox}} = 3\left(\frac{3.45\times10^{-13}\,F/cm}{1.5\times10^{-8}\,m}\right)(3\,\mu m)(1.5\,\mu m)\times\frac{1\,m}{10^6\,\mu m}\times\frac{1\,m}{10^6\,\mu m}\times\frac{10^2\,cm}{1\,m}$

$$C_G = 3.105\times10^{-14}\,F$$

(16) $C_P = C_{db} + C_{sb} + C_{wire}$ ← Assume Cwire negligible

$C_P = W_n L_{diff_n} C_{jn} + W_p L_{diff_p} C_{jp} + (W_n + 2L_{diff_n}) C_{jsw_n} + (W_p + 2L_{diff_p}) C_{jsw_p}$

WITH, $L_{diff_n} = L_{diff_p} = L_{diff} = 6\,\mu m$, $C_{jn} = 1\times10^{-4}\,F/m^2$, $C_{jp} = 3\times10^{-4}\,F/m^2$

$C_{jsw_n} = 5\times10^{-10}\,F/m$ $\quad C_{jsw_p} = 3.5\times10^{-10}\,F/m$

$W_n = 3\,\mu m$, $W_p = 6\,\mu m$

$C_P = (3\times10^{-6}m)(6\times10^{-6}m)\left(1\times10^{-4}\frac{F}{m^2}\right) + (6\times10^{-6}m)(6\times10^{-6}m)\left(3\times10^{-4}\frac{F}{m^2}\right) + \left(3\times10^{-6}m + 2(6\times10^{-6}m)\right)\left(5\times10^{-10}\frac{F}{m}\right)$

$+ \left(6\times10^{-6}m + 2(6\times10^{-6}m)\right)\left(3.5\times10^{-10}\,F/m\right)$

$C_P = 1.8\times10^{-15} + 1.08\times10^{-14} + 7.5\times10^{-15} + 6.3\times10^{-15}\ F$

$$C_P = 2.64\times10^{-14}\,F$$

With (14): $C_L = 3.105\times10^{-14} + 2.64\times10^{-14}$

$$C_L = 5.745\times10^{-14}\,F$$ load capacitance of a 5V CMOS inverter with $W_p = 2W_n = 6\,\mu m$ driving similar 5 V CMOS inverter

NOW, with $C_L = 5.745 \times 10^{-14}$ F AND (13)

$$t_{PHL} = \frac{C_L \, V_{OH}/2}{\frac{k_n}{2}(V_{OH} - V_{Tn})^2}$$

$V_{OH} = V_{DD} = 5V$

$V_{Tn} = 1V$

$k_n = \left(\frac{W}{L}\right)_n \mu_n C_{ox_n}$

$$= \frac{(5.745 \times 10^{-14} F)(2.5V)}{\frac{1}{2}\left(\frac{3}{1.5}\right) 50 \times 10^{-6} \frac{A}{V^2} (2.5V)^2}$$

$$t_{PHL} = 4.596 \times 10^{-10} s \rightarrow \underline{0.46 ns}$$

(17) $$t_{PLH} = \frac{C_L \, V_{OH}/2}{\frac{k_p}{2}(V_{DD} + V_{Tp})^2}$$

$V_{Tp} = -V_{Tn}$

$k_p = k_n$ (by design)

$$= \frac{C_L \, V_{OH}/2}{\frac{k_n}{2}(V_{DD} - V_{Tn})^2} = t_{PHL} = 0.46 ns$$

symmetrical by design.

Give Ratio of load capacitance C_L at output to the load capacitance for a 5V CMOS inverter by χ. To minimize propagation delay scaled size inverters are cascaded. If each following inverter is u times wider than the previous, then for N inverters cascaded.

$$\chi = u^N$$
$$\ln \chi = N \ln u$$
$$N = \frac{\ln \chi}{\ln u}$$

Total delay $t = N \cdot u \, t_1$ where t_1 is the delay of a 5V CMOS inverter with $W_p = 2W_n = 6 \mu m$.

IF for a function $F = N u t_1 = \frac{\ln \chi}{\ln u} u t_1$

$$\frac{dF}{du} = \frac{d}{du}\left(\frac{\ln \chi}{\ln u} u\right) = 0 \quad \text{for minima}$$

$$\ln \chi \left(\frac{\ln u - \frac{1}{u} u}{(\ln u)^2}\right) = 0$$

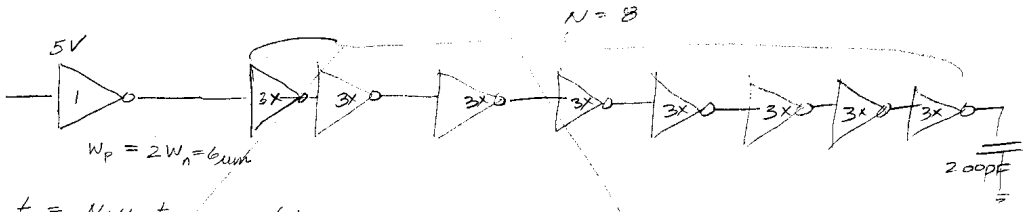
$$\ln u = 1$$
$$e^{\ln u} = e \rightarrow u = e \sim 2.8$$

So for optimum, 8 times larger inverters would be best. Selecting a closest integer of $3 = 4$.

$$3^N = \frac{200pF}{3.675 \times 10^{-14} F}$$

$$N \approx 7.93 \longrightarrow \text{choose } N = 8$$

So FOR buffers:



$t = N \cdot 4 \cdot t_{PHL}$ $(t_{PHL} = t_{PLH})$

$= (2)(3)(0.294\,ns)$

$= 7\,ns$

$C_L = 200pF$

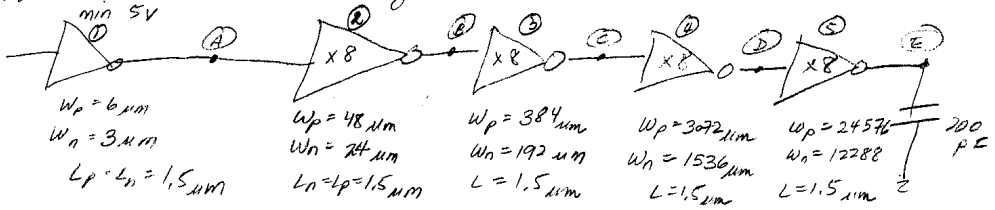
C_L of min. $(W_p = 2W_n = 6\mu m) = 5.75 \times 10^{-14} F$

$\frac{200 \times 10^{-12} F}{5.75 \times 10^{-14} F} = 3478$, $t_{min} = t_{pLH} = t_{pHL} = 0.46 ns$

N	$\sqrt[N]{x}$	$t = N \cdot x \cdot t_{min}$
0	—	—
1	3478	1.60 ns
2	59.0	54.3 ns
3	15.2	20.9 ns
4	7.68	14.13 ns
5	5.108	11.7 ns
6	3.89	10.7 ns

N	$\sqrt[N]{x}$	t	
7	3.20	10.3 ns	
8	2.77	10.2 ns	optimum
9	2.47	10.22	

We do not need to choose an optimum t delay with 8 buffers since 400ns is a relax delay requirement, We need an even number to perform the correct logic function* so choose $N = 4$ ($N=2$ would use too big of an area



$t_{delay} = 0.46ns \times 8 \times 4 = \underline{14.72 ns}$

For ① : previously calculated, by symmetry,

$V_m = 2.5 V$

$g_{mn} = g_{mp} = 150 \times 10^{-6} S$

$r_{on} = r_{op} = 1.08 \times 10^5 \Omega$

$A_V = -16.2$

$V_{IL} = 2.35 V \rightarrow NM_L = 2.35 V$

$V_{OL} = 2.65 V \rightarrow NM_H = 2.35 V$

$$t_{PHL} = \frac{C_{LA} \Delta V}{I_D} = \frac{C_{LA} V_{OH}/2}{\frac{k_n}{2}(V_{OH} - V_{tn})^2} \rightarrow C_{LA}$$

* Not including the minimum width 5 V inverter at $W_p = 2W_n = 6\mu m$ and assuming a 3 V inverter and 5V inverter (of special NM) after the NAND gate. See design schematic.

$C_{LA} = C_{G2} + C_{P1}$

$C_{G2} = C_{ox_p}(WL)_{p2} + C_{ox_n}(WL)_{n2}$

$= 3\,C_{ox_n}(WL)_{n2}$

$= (3)\dfrac{(3.45\times10^{-13}\ F/cm)}{1.5\times10^{-8}\ m}(24\times10^{-6}\ m)(1.5\times10^{-6}\ m)\dfrac{10^2\ cm}{1\ m}$

$C_{G2} = 2.484\times10^{-13}\ F$

$C_{P1} = C_{db1} + C_{sb1}$ ($C_{wire} = 0$)

$C_{P1} = W_{n1}L_{diff_n}C_{jn} + W_{p1}L_{diff_p}C_{jp} + (W_{n1} + 2L_{diff_n})C_{jsw_n} + (W_{p1} + 2L_{diff_p})C_{jsw_p}$

= PREVIOUS CALCULATION

$= 2.64\times10^{-14}\ F$

$C_{LA} = C_{G2} + C_{P1} = \underline{2.75\times10^{-13}\ F}$

$t_{pHL} = \dfrac{(2.75\times10^{-13}\ F)(2.5)}{\frac{1}{2}\left(\frac{3}{1.5}\right)50\times10^{-6}\ (2.5)}$

$t_{pHL} = \underline{2.2\ ns} = t_{PLH}$

FOR ②, ③, ④, ⑤:

$V_m = 2.5\ V$ by symmetry

$g_{mn_2} = g_{mp_2} = \left(\frac{W}{L}\right)_{p2}(V_{DD} - V_m + V_{TP}) = 8\left(\frac{W}{L}\right)_{p1}(V_{DD} - V_m + V_{tp})$

$= \underline{1.2\times10^{-3}\ S}$

$r_{on_2} = r_{op_2} = \dfrac{1}{\lambda_n I_{Dn2}} = \dfrac{1}{\lambda_n\left(\frac{W}{2L}\right)_{n2}\mu_n C_{ox_n}(V_m - V_{Tn})^2(1+\lambda_n V_m)}$

$= \frac{1}{8}r_{on1} = \underline{1.35\times10^4\ \Omega}$

$A_V = -2g_{mn_2}\dfrac{r_{on2}}{2} = -g_{mn_2}r_{on2} = -8g_{mn1}\frac{1}{8}r_{on1} = +A_{V_1} = \underline{-16.2}$

$\therefore V_{IL2} = 2.35\ V \quad NM_{L2} = 2.35\ V$

$V_{IH} = 2.65\ V \quad NM_{H2} = 2.35\ V$

Since g_m increases by the scaling factor & r_o decreases by same scaling factor, A_V is same for all buffers & so are the noise margins. So

$V_{IL3} = V_{IL4} = V_{IL5} = 2.35\ V$, $NM_{L3} = NM_{L4} = NM_{L5} = 2.35\ V$

$V_{IH3} = V_{IH4} = V_{IH5} = 2.65\ V$, $NM_{H3} = NM_{H4} = NM_{H5} = 2.35\ V$

C_{LE} : $C_{LE} = C_{G6} + C_{p5}$

$C_{G6} = C_L = 200pF$

$C_{p5} = (12288\times10^{-6}m)(6\times10^{-6}m)(1\times10^{-6}\frac{F}{m^2}) + (24576\times10^{-6}m)(6\times10^{-6}m)(3\times10^{-6}\frac{F}{m^2}$

$+(12288\times10^{-6}m + 2(6\times10^{-6}m))(5\times10^{-10}\frac{F}{m}) + (24576\times10^{-6}m + 2(6\times10^{-6}m))(3.5\times10^{-10}\frac{F}{m})$

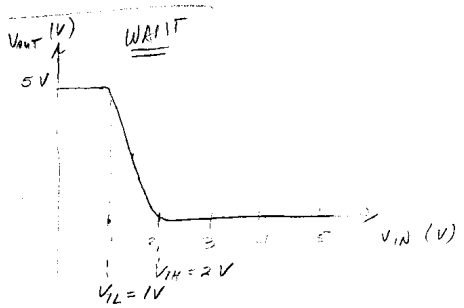
$= 6.6369\times10^{-11}F$

$C_{LE} = 266\,pF$

5 V inverter with input from 3 V inverter

$V_{OH_{3V}} = 3\ V$

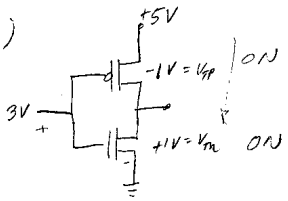
$V_{OL_{3V}} = 0\ V$



Would like to switch my with a 3V input. If impose a 1V noise margin, then that implies $V_{IH} = 2\ V$

We will try by shifting V_m to less than $\frac{V_{DD}}{2}$ where $V_{DD} = 5V$.

Shift w/ Select $V_m = 1.5\ V$ (Same as the 3V inverter sym.)



$$V_m = \frac{V_{tn} + \sqrt{\frac{k_p}{k_n}}(V_{DD} + V_{tp})}{1 + \sqrt{\frac{k_p}{k_n}}}$$

$$V_m\left(1 + \sqrt{\frac{k_p}{k_n}}\right) = V_{tn} + \sqrt{\frac{k_p}{k_n}}(V_{DD} + V_{tp})$$

$$V_m + \sqrt{\frac{k_p}{k_n}}V_m = V_{tn} + \sqrt{\frac{k_p}{k_n}}(V_{DD} + V_{tp})$$

$$V_m - V_{tn} = \sqrt{\frac{k_p}{k_n}}(V_{DD} + V_{tp} - V_m)$$

$$\sqrt{\frac{k_p}{k_n}} = \frac{V_m - V_{tn}}{V_{DD} + V_{tp} - V_m} = \frac{1.5 - 1}{5 - 1 - 1.5} = \frac{0.5}{2.5} = \frac{1}{5} \Rightarrow k_n = 25\,k_p$$

$$\left(\frac{W}{L}\right)_n \mu_n C_{ox_n} = 25\left(\frac{W}{L}\right)_p \mu_p C_{ox_p}$$

$$\frac{\left(\frac{W}{L}\right)_n}{\left(\frac{W}{L}\right)_p} = \frac{25\,\mu_p C_{ox_p}}{\mu_n C_{ox_n}} = \frac{25(125\mu)}{50\times10^{-6}}$$

$$\frac{W_n}{W_p} = 12.5$$

$W_n = 12.5\,W_p$

$$g_{mn} = k_n(V_{in} - V_{tn}) = \left(\frac{W}{L}\right)_n KP(V_m - V_{tn})$$

$$= 125\left(\frac{3}{1.5}\right)50\times10^{-6}\frac{A}{V^2}(1.5 - 1) = 6.25\times10^{-4}\,S$$

$$g_{mp} = k_p(V_{DD} - V_m + V_{tp}) = \left(\frac{3}{1.5}\right)25\times10^{-6}\frac{A}{V^2}(5 - 1.5 - 1) = 1.25\times10^{-4}\,S$$

$$I_{Dn} = \left(\frac{W}{2L}\right)_n KP(V_m - V_{tn})^2(1 + \lambda V_m)$$

$$= \frac{125}{2}\left(\frac{3}{1.5}\right)(50\times10^{-6}\frac{A}{V^2})(0.5V)^2(1 + 7\times10^{-2}(1.5)) = 1.173\times10^{-4}\,A$$

$(w/o\ \lambda_n\ I_{Dn} = 1.56\times10^{-4}\,A)$

$$-I_{Dp} = \left(\frac{W}{2L}\right)_p KP(V_{DD} - V_{tp} + V_{tp})^2(1 + \lambda(V_{DD} - V_m))$$

$$= \left(\frac{1}{2}\right)\left(\frac{3}{1.5}\right)(5 - 1.5 - 1)^2(1 + 7\times10^{-2}(5 - 1.5))\times25\times10^{-6}\frac{A}{V^2} = 1.945\times10^{-4}\,A$$

$(w/o\ \lambda_p\ -I_{Dp} = 1.56\times10^{-4}\,A)$

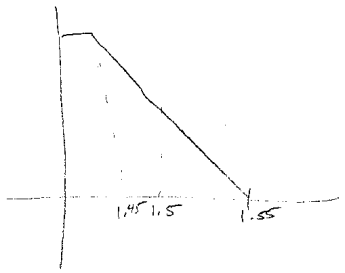
$I_{Dn} \approx -I_{Dp}$ with λ

$$r_{on} = \frac{1}{\lambda_n I_{Dn}} = \frac{1}{7\times10^{-2}\,V^{-1}\,(1.73\times10^{-4}\,A)} = 8.26\times10^{4}\,\Omega \approx r_{op} \quad \left(\text{by } \lambda_n = \lambda_p,\ I_{Dn} = I_{Dp}\right)$$

$$A_v = -(g_{mn} + g_{mp})\,r_{on} \,//\, r_{op}$$

$$= -(6.25\times10^{-4}\,S + 1.25\times10^{-4}\,S)\,\frac{8.26\times10^{4}\,\Omega}{2}$$

$$\approx -31$$



$$V_{IL} = V_m + \frac{V_{DD} - V_m}{A_v} = 1.5 + \frac{5-1.5}{-31}$$

$$V_{IL} = 1.39\ V$$

$$V_{IH} = V_m - \frac{V_m}{A_v} = 1.5 - \frac{1.5}{-31} = 1.55\ V$$

$$NM_L = 1.39\ V$$

$$NM_H = 3 - 1.55 = 1.45\ V$$

C_L : C_G (OF 5V INVERTER) + C_P (OF THIS 5V SKEWED V_m)

$C_G = 3.105\times10^{-14}\,F$ (prev. calculated)

$$C_P = C_{DB} = W_n L_{diff_n} C_{jn} + W_p L_{diff_p} C_{jp} + (W_n + 2L_{diff_n}) C_{jsw_n} + (W_p + 2L_{diff_p}) C_{jsw_p}$$

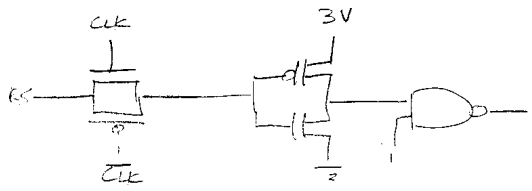
$$= 12.5\,(3\times10^{-6}\,m)(6\times10^{-6}\,m)\left(1\times10^{-4}\,\frac{F}{m^2}\right) + (3\times10^{-6}\,m)(6\times10^{-6}\,m)\left(3\times10^{-4}\,\frac{F}{m^2}\right)$$

$$+ \left(12.5\,(3\times10^{-6}\,m) + 2(6\times10^{-6}\,m)\right)\left(5\times10^{-10}\,\frac{F}{m}\right) + \left(3\times10^{-6} + 2(6\times10^{-6})\right)\left(3.8\times10^{-10}\,\frac{F}{m}\right)$$

$$= 5.79\times10^{-14}\,F$$

$$C_L = 8.895\times10^{-14}\,F$$

PASS GATE + 3V INVERTER + NAND



PASS GATE

$$t_{PLH} = \frac{C_{LH}\left(\frac{V_{OH}}{2}\right)}{\overline{I}_{DLH_n} + \overline{I}_{DLHp}}$$

Choose $W_p = 6\mu m$, $W_n = 3\mu m$ $\longrightarrow \left(\frac{W}{L}\right)_p = \left(\frac{6}{1.5}\right)$ $\left(\frac{W}{L}\right)_n = \left(\frac{3}{1.5}\right)$

w/o γ $\rightarrow V_{Tn} = V_{T0}$

$$\overline{I}_{DLH_n} = \frac{\frac{k_n}{2}\left(V_{DD} - V_{T_n}\right)^2 + \frac{k_n}{2}\left(V_{DD} - V_{OH} - V_{Tn}\right)^2}{2} \quad ; \quad \text{with } V_{OH} = V_{DD}$$

$$= \frac{\frac{1}{2}\left(\frac{W}{L}\right)_n KP_n\left[\left(V_{DD} - V_{T0_n}\right)^2 + \left(\frac{V_{DD}}{2} - V_{Tn}\right)^2\right]}{2}$$

$$= \frac{1}{2}\left(\frac{3}{1.5}\right)\left(50\times10^{-6}\frac{A}{V^2}\right)\left[(3-0.7)^2 + (1.5-0.7)^2\right]$$

$$\overline{I}_{DLH_n} = 1.4825\times10^{-4}\,A$$

$$\overline{I}_{DLHp} = \frac{k_p}{2}\left(V_{DD} + V_{Tp}\right)^2 = \frac{1}{2}\left(\frac{W}{L}\right)_p KP\left(V_{DD} + V_{Tp}\right)^2 = \left(\frac{6}{1.5}\right)\left(25\times10^{-6}\frac{A}{V^2}\right)(3-0.7V)^2$$

$$\overline{I}_{DLHp} = 2.64\times10^{-4}\,A$$

$$C_{LH} = C_G + C_{DB} + \underbrace{\frac{2}{3}(WL)_n C_{ox}}_{C_{GPS}} \qquad (\text{Assume } C_{ov} = 0)$$

$$C_G = (WL)_n C_{ox} + (WL)_p C_{ox} \quad ; \quad \text{let } W_p = 2\cdot W_n = 6\mu m \text{ for 3V inverter}, \; L_n = L_p = 1.5\mu m$$

$= 3(WL)_n C_{ox} = C_G$ of 5V inverter w/ same dimensions

$= 3.105\times10^{-14}\,F$

$$C_{DB} = W_n L_{diff_n} C_{j_n} + W_p L_{diff_p} C_{j_p} + \left(W_n + 2L_{diff_n}\right)C_{jsw_n} + \left(W_p + 2L_{diff_p}\right)C_{jsw_p}$$

$=$ SAME AS C_{DB} of 5V inverter w/ same dimensions

$C_{DB} = 2.64\times10^{-14}\,F$

$C_{GPG} = \frac{2}{3}(WL)_p C_{ox}$ (OF PASS GATE)

$$\frac{2}{3}\left(3\times10^{-6}m\right)\left(1.5\times10^{-6}m\right)\left(3.45\times10^{-13}\frac{F}{cm}\right)\frac{10^2 cm}{1m}$$
$$1.5\times10^{-8}m$$

$C_{GPG} = 6.9\times10^{-15}F$

$C_{LLH} = 3.105\times10^{-14} + 2.64\times10^{-14} + 6.9\times10^{-15}F$

$C_{LLH} = 6.9\times10^{-14}F$

$$t_{PLH} = \frac{(6.9\times10^{-14}F)(1.5V)}{(1.483\times10^{-4} + 2.64\times10^{-4})\frac{A}{V^2}}$$

$t_{PLH} = 2.33\times10^{-10}s = 0.233ns$

$$t_{PHL} = \frac{C_{LHL}V_{DD}/2}{\bar{I}_{DHLn} + \bar{I}_{DHLp}}$$

$$\bar{I}_{DHLp} = \frac{\frac{k_p}{2}(V_{DD}+V_{TOP})^2 + \frac{k_p}{2}(V_{DD}-\frac{V_{DD}}{2}+V_{TP})^2}{2} \qquad V_{TP} = V_{TOP} = -.7V$$

$$= \frac{1}{2}\left(\frac{W}{L}\right)_p K^p\left[(V_{DD}+V_{TOP})^2 + (\frac{V_{DD}}{2}+V_{TOP})^2\right]$$
$$2$$

$$= \frac{1}{4}\left(\frac{6}{1.5}\right)\left(25\times10^{-6}\frac{A}{V^2}\right)\left((3-0.7)^2+(1.5-0.7)^2\right)$$

$\bar{I}_{DHLp} = 1.4825\times10^{-4}A$

$$\bar{I}_{DHLn} = \frac{k_n}{2}(V_{DD}+V_{TOP})^2 = \frac{1}{2}\left(\frac{3}{1.5}\right)50\times10^{-6}\frac{A}{V^2}(2.3V)^2$$
$$= 2.645\times10^{-4}A$$

$C_{LHL} = C_G + C_{DB1} + \frac{2}{3}(WL)_p C_{ox}$

$$\frac{2}{3}(WL)_p C_{ox} = \frac{2}{3}\left(6\times10^{-6}m\right)\left(1.5\times10^{-6}m\right)\frac{3.45\times10^{-13}F/cm\times10^2 cm}{1.5\times10^{-8}m\ 1m} = 1.38\times10^{-14}F$$

$C_{LHL} = 3.105\times10^{-14} + 2.64\times10^{-14} + 1.38\times10^{-14}$

$C_{LHL} = 7.125\times10^{-14}F$

$$t_{PHL} = \frac{(7.125\times10^{-14}\text{F})(1.5\text{ V})}{(1.4925\times10^{-4}\text{ A/V}^2) + (2.645\times10^{-4}\text{ A/V}^2)}$$

$$t_{PHL} = 2.59\times10^{-10}\text{ s} = \underline{0.259\text{ ns}}$$

$NM_L = V_{TN} = 0.7\text{ V}$

$NM_H = -V_{TP} = +0.7\text{ V}$

3V inverter after the first cycle

Again, choose $W_p = 2W_n = 6\,\mu m$, $L_n = L_p = 1.5\,\mu m$

this gives $k_p = k_n$ so that

$V_M = 1.5\text{ V}$

$$g_{mn} = g_{mp} = k_n(V_m - V_{TN}) = \left(\frac{W}{L}\right)_n KP(V_m - V_{TO})$$

$$= \left(\frac{3}{1.5}\right)\left(50\times10^{-6}\frac{A}{V^2}\right)(1.5 - 0.7)\text{ V}$$

$$= 8\times10^{-5}\text{ S}$$

$$r_{on} = r_{op} = \frac{1}{\lambda_n I_{Dn}}\quad ;\quad I_{Dn} = \left(\frac{W}{2L}\right)_n KP(V_m - V_{TO})^2(1 + \lambda_n V_M)\quad ;\quad \lambda_n = 7\times10^{-2}\text{V}^{-1}$$

$$= \frac{1}{\frac{3}{2(1.5)}\left(50\times10^{-6}\right)(1.5-0.7)^2(1 + 7\times10^{-2}(1.5))}$$

$$= 3.54\times10^{-5}\text{ A}$$

$$r_{on} = r_{op} = \frac{1}{(7\times10^{-2}\text{V}^{-1})(3.54\times10^{-5}\text{ A})} = 4.04\times10^{5}\,\Omega$$

$$A_v = -(g_{mn} + g_{mp})\,r_{on} \| r_{op} = -1.43\times10^{1} = \underline{-14.3}$$

$$V_{IL} = V_m + \frac{V_{DD} - V_m}{A_V} = 1.5 + \frac{1.5}{-14.3} = 1.395 = \underline{1.4\text{ V}}$$

$$V_{IH} = V_M - \frac{V_m}{A_V} = 1.5 - \frac{1.5}{-14.3} = \underline{1.6\text{ V}}$$

$NM_L = V_{IL} = \underline{1.4\text{ V}}$

$NM_H = 3 - 1.6\text{ V} = \underline{1.4\text{ V}}$

C_L of 3V inverter

$C_L = C_g + C_p$ $\quad C_p = C_{DB} + C_{wire}$ $\quad$ (Assume $C_{wire} = 0$)

Load capacitance of 3V inverter is a combination of the gate capacitance of the NAND gate and C_p of the 3V inverter itself.

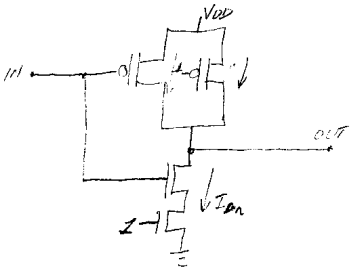
$C_{g(NAND)} = C_{g\,3V\,inverter} = 3.105 \times 10^{-14}$ F

$C_{DB_{3V}} = C_{DB} = 2.64 \times 10^{-14}$ F

$C_L = 5.746 \times 10^{-14}$ F

Same dimensions: $W_p = L_{min} = 2 \times L_n$, $L = 1.5\ \mu m$, as symmetrical 5V inverter

NAND Gate calculations: TREAT AS INVERTER Except for V_m CALCULATION



Since PMOS in parallel, the wide W_p is effectively doubled. So for symmetry, $\left(\frac{W}{L}\right)_p = 2\left(\frac{W}{L}\right)_n$

$W_p = W_n = 3\ \mu m$, $L_n = L_p = 1.5\ \mu m \rightarrow k_p = k_n$

$$V_m = \frac{V_{tn} + 2\sqrt{\frac{k_p}{k_n}}(V_{DD} + V_{tp})}{1 + 2\sqrt{\frac{k_p}{k_n}}} = \frac{V_{tn} + 2V_{DD} + 2V_{tp}}{1 + 2}$$

$$= \frac{1 + 2(3) - 2}{3} = \frac{5}{3} = 1.67\ V$$

$g_{mn} = k_n(V_m - V_{tn}) = \left(\frac{3}{1.5}\right)(50 \times 10^{-6}\ \frac{A}{V^2})(1.67 - 0.7) = 9.7 \times 10^{-5}$ S

$g_{mp} = k_p(V_{DD} - V_m + V_{tp}) = \left(\frac{3}{1.5}\right)(25 \times 10^{-6}\ \frac{A}{V^2})(3 - 1.67 - 0.7) = 3.15 \times 10^{-5}$ S

$I_{Dn} = k_p(V_{DD} - V_m + V_{tp})^2$ $\quad$ (Eq. 5.48)

$= \left(\frac{W}{L}\right)_p KP\,(V_{DD} - V_m + V_{tp})^2 = \left(\frac{3}{1.5}\right)(25 \times 10^{-6}\ \frac{A}{V^2})(3 - 1.67 - 0.7)^2$

$I_{Dn} = 1.9845 \times 10^{-5}\ A = -2I_{Dp}$

$r_{o_n} = \frac{1}{\lambda_n I_{Dn}} = \frac{1}{7 \times 10^{-2}(1.9845 \times 10^{-5}\ A)} = 7.20 \times 10^5\ \Omega$

$r_{o_p} = \frac{1}{\lambda_p I_{Dp}} = \frac{1}{7 \times 10^{-2}\left(\frac{1.9845 \times 10^{-5}\ A}{2}\right)} = 14.4 \times 10^5\ \Omega$

$A_V = -(g_{mn} + g_{mp})\, r_{on} \| r_{op} = (9.7 + 3.15) \times 10^{-5}\ S \left(\frac{(7.2 \times 10^5)(14.4 \times 10^5)\ \Omega^2}{7.2 \times 10^5 + 14.4 \times 10^5\ \Omega}\right) = -61.7$

$V_{IL} = V_M + \frac{V_{out} - V_M}{A_v} = 1.67 + \frac{3 - 1.67}{-61.7} = \underline{1.64\ V}$

$NM_L = 1.64\ V$

$V_{IH} = V_M - \frac{V_M}{A_v} = 1.67 - \frac{1.67}{61.7} = \underline{1.70\ V}$ ← NOT SYM. HAND CALCULATIONS OF NM may not be possible for HAND gate as the eqns provided by text.

$NM_H = 3 - 1.7 = \underline{1.3\ V}$

$C_L = C_G + C_P$

$C_{G_{ASYM\ 5V_{INVERTER}}} = (WL)_p C_{ox_p} + (WL)_n C_{ox_n} = (3\times10^{-6}m)(1.5\times10^{-6}m)\left(\frac{3.45\times10^{-11}\ F}{1.5\times10^{-6}\ m}\right) + (37.5\times10^{-6}m)(1.5\times10^{-6}m)\left(\frac{3.45\times10^{-11}\ F/m}{1.5\times10^{-6}\ m}\right)$

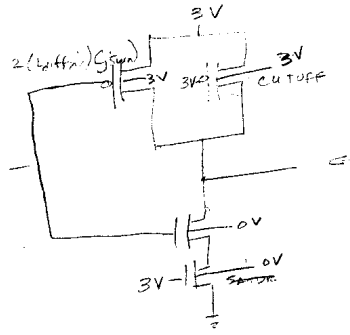
$C_G = 1.397\times10^{-13}\ F$

$C_P = C_{DB} + C_{wire}$

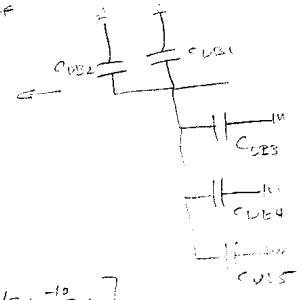
$C_{DB} = 2C_{DB_p} + 3C_{DB_n}$

$= 3\left(W_n L_{diff_n} C_{j_n} + (W_n + 2(L_{diff_n}) C_{j_{SW_n}})\right)$

$+ 2\left(W_p L_{diff_p} C_{j_p} + (W_p + 2(L_{diff_p}) C_{j_{SW_p}})\right)$



DEPLETION CAPACITANCE



WORST CASE SCENARIO WITH BULK OF TOP NMOS TIED TO 0V due to process.

$= 3\left[(3\times10^{-6}m)(6\times10^{-6}m)(1\times10^{-4}\frac{F}{m^2}) + (3\times10^{-6}m + 2(6\times10^{-6}m))(5\times10^{-10}\frac{F}{m})\right]$

$+ 2\left[(3\times10^{-6}m)(6\times10^{-6}m)(3\times10^{-4}\frac{F}{m^2}) + (3\times10^{-6}m + 2(6\times10^{-6}m))(3.5\times10^{-10})\right]$

$= 3\left[9.3\times10^{-15}\right] + 2\left[1.065\times10^{-14}\right] = \underline{4.92\times10^{-14}\ F}$

$C_L = 1.89\times10^{-13}\ F$