Contents

Chapter 1

Implementation

Collaborators: [redacted]

This paper outlines the design for a section of a CMOS Integrated Row Driver that will be utilized in a new display technology. The design team had certain concrete objectives to be reflected in the design of the circuit.

- The propagation delay must be less than 400 ns.
- All output rise and fall times must be less than 200 ns.
- All logic gates within the circuit must have noise margins of at least 1.0V.
- Power dissipitation should be kept at a mimimum, particularly at 1mW for standard input waveforms.

Although meeting such constraints is desireable, some often come at the expense of others. Thus, the team was faced with a number of engineering decisions involving certain tradeoffs.

1.1 Abstract

The fundamental problem addressed by this design is the need to drive a large (200 pF) capacitive load. Because a single buffer has a high input capacitance and knowing that capacitance is purely geometry-dependent, merely utilizing a single inverter to drive a 200 pF capacitor is not a viable solution. Rather, a chain of four inverters of increasing size was implented, using the "4x Approximation" as a guideline. The circuit not only keeps power dissipation relatively small, it timing characteristics indicate that it performs well.

As shown in the table summarizing the results, the average power dissipation beats the requirement by 10 percent and despite this, the propagation delays are significantly below the maximum allowable. Clearly, the results indicate that the designers were cognizant of keeping the power dissipated at a minimum, while maximizing performance.

Chapter 2

Engineering Decisions

2.1 Transistor Length

Given the constraint that the minimum transistor length (L) was 1.5um, it was immediately determined that keeping L at its minimum was advantageous in all respects. Specifically, the drain current varies inversely with L and capacitance increases with L. Hence, there is absolutely no advantage in using L ¿ 1.5um and every transistor in this circuit has a length of 1.5 um. This is reflected in the attached Spice script as well as the hand calculations.

2.2 "N" Inverter Chain

As mentioned in Section 1.1, a buffer chain of length N was needed to drive a large capacitive load. In this implementation, N takes on the value of 4 and this decision was made based on characteristics inherent to the CMOS inverter.

- N cannot be odd, since the output is not an inverted version of Vrs.
- We made the assumption that kp = 2kn, which implies that the p channel transistors are double the size of their n channel counterparts, yielding symmertric rise and fall times.
- We also know that CMOS inverter has a propagation delay of one-half the rise time because its trip-point occurs when Vin = Vm = Vdd/2.
- To meet the 400 ns requirement, we take the worst-case scenario, with a rise time of 200 ns.
- Thus, N = 4.

2.3 The 5 Volt Switch

The circuit uses 2 DC power supplies at 3 and 5 Volts and one of the decisions facing the design team was exactly "which" inverter to implement the switch from 3 to 5 Volts. It was decided that the third inverter was the ideal choice, using the following reasoning.

- The fourth and final inverter CANNOT be the first inverter to switch to 5 Volts. We want a "clean" output for the final inverter. In other words, either 0 Volts or 5 Volts. If the switch were made at the final inverter, it would bring about the possibility of a non-zero input to the final inverter that is less than 5V.
- Thus, we moved in the chain, one inverter to the left. Changing Vdd here turned out to be the optimal choice, as adding more 5V inverters proved detrimental to power consumption.

2.4 Choice of Widths in Inverter Chain

As established in Section 2.1. the transisor length remains constant throughout the inverter change. That means, that in order to scale the size of the inverter, the width "W" is the only parameter that can be altered. While we did not use a constant scale factor, we started with a scale factor of 3. We chose 3 because after calculating the L and W for the final inverter (see Hand Calculations), scaling by four did not give us enough lee-way. Scaling twice resulted in the minimum size transistor.

The only exeption to this rule, of course was the third buffer, the first 5V inverter. In the third inverter, we used the scale factor of 3 to scale Wn. However, rather than scale Wp accordingly, we set Wp to its minimum (3 um). The motivations for this are discussed in the section that follows.

2.5 Assymetry

Three out of the four inverters in the chain are symmetric because kp is twice kn. However, for the third inverter, we intentionally created an assymetric configuration strictly for power consumption sake. We know that Vout is proportional to (kp/kn). Reducing the width of the p channel with respect to the n channel will drive the Voltage vout down, greatlyi reducing the power consumed. This was a critical move that allowed the circuit to meet the power specification of 1 mW.

Chapter 3

Hand Calculations and SPICE simulation

Overall, the results show our calculations correspons well with the SPICE simulation. There is one significant discrepancy, however. Our estimated propagation delays differed significantly from the simulated values generated on SPICE. However, that was more than likely due to timing constraints (no pun intended).

In the following pages, you will find:

1. A summary of the calculated and simulated results.
2. A complete (albeit poorly drawn) schematic of the circuit.
3. Calculated Values for gate and drain capacitance.
4. Calculated Values of Power for each stage.
5. Calculated Values for Delay at each stage.
6. Calculation of Mimimum Noise Margin
7. Spice Code (also found at */ashwin/Public/allnighter/dp1.sp).*
8. Graphs Generated on Awaves

Collaborators: [redacted]

Design Problem #1 -Digital Circuits

Fall 2000

Name(s):_____

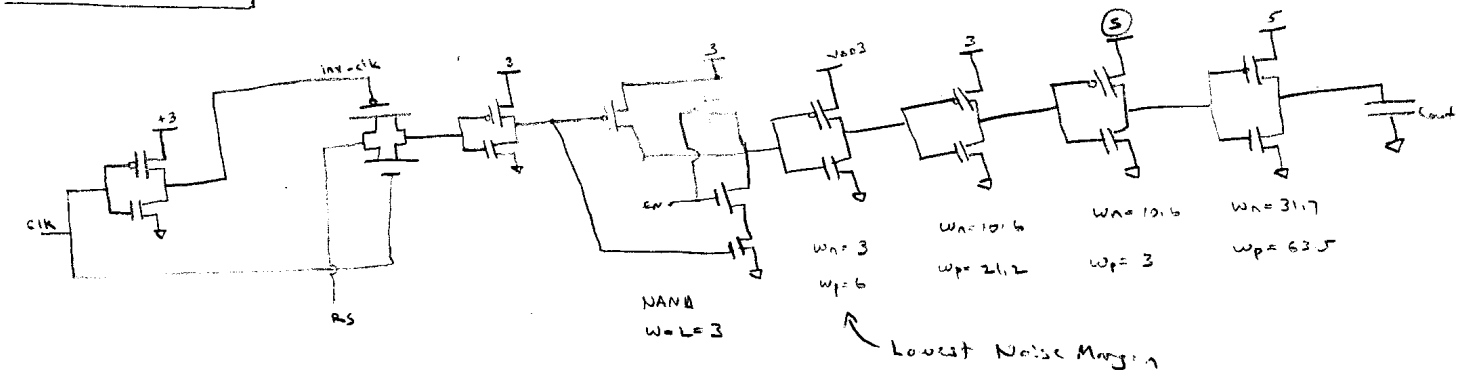
Athena username(s):_____

HSPICE input filename(s):_____

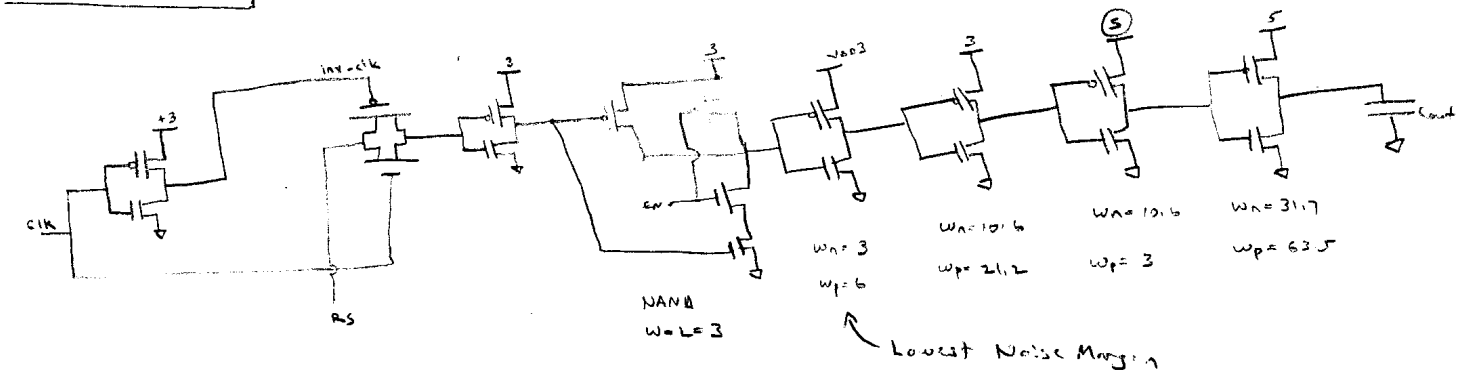
SPECIFICATION	YOUR DESIGN
N (number of inverters at output stage)	4

PARAMETER	SPECIFICATION	YOUR CALCULATED VALUE	YOUR SIMULATED VALUE
OUTPUT t_r	< 200 ns	N/A	125.1 ns
OUTPUT t_f	< 200 ns	N/A	125.1 ns
t_{pd0}	< 400 ns	131.75 ns	44 ns
t_{pd1}	< 400 ns	128.15 ns	63 ns
Average power dissipation	< 1 mW	0.91 mW	0.89 mW
Minimum Noise Margin	> 1.0 Volt	1.29 V	1.055 V

Schematic


inv-clk
3
3
3
Vdd3
3
5
5
+3
CLK
RS
en
NAND
W=L=3
Wn=3
Wp=6
Wn=10.6
Wp=21.2
Wn=10.6
Wp=3
Wn=31.7
Wp=63.5
Cout
Lowest Noise Margin

Schematic


inv-clk
3
3
3
Vdd3
3
5
5
+3
CLK
RS
en
NAND
W=L=3
Wn=3
Wp=6
Wn=10.6
Wp=21.2
Wn=10.6
Wp=3
Wn=31.7
Wp=63.5
Cout
Lowest Noise Margin

Power

Clock Inverter

$C_L = (2.3 \times 10^{-3})(13.5 \times 10^{-12}) =$ **31 fF**

$P = C_L V_{DD}^2 f$

$= (3.1 \times 10^{-15})(3^2)(76.8 \times 10^3\ Hz)$

$=$ **21.4 nW**

Transmission Gate

$C_L = C_0 + C_p + \frac{2}{3}(WL)_p C_{ox} + W_n C_{ox}$

$= 44.8$ fF

→ **P = 31 nW**

Inverter for NAND

P = 21.4 nW same dimensions as clock inverter!

NAND

$C = C_{m3} // (C_{m4} + C_{m2} + C_{m1})$

$= 4.12$ fF

P = 2.8 nW

Inv 1

$C_L = (13.5 \times 10^{-12})(2.3 \times 10^{-3}) = 31.1$ fF

$P = (31.1 \times 10^{-15})(9)(76.8 \times 10^3) =$ **21.4 nW**

Inv 2

$C_L = 110$ fF

$P = (110 \times 10^{-15})(9)(76.8 \times 10^3) =$ **76 nW**

Inv 3

$C_L = 47$ fF

P = 90 nW

Inv 4

$C_L = 328$ fF

P = **631 nW**

Total Power = 895 nW

$(895 \times 10^{-9}\ W)(1024) =$ **0.91 mW**

Delay 1

Clock Inverter

$T_{PD} = C\frac{dV}{dt}$

$dt = \frac{C\,dV}{I_D}$

$= \frac{(44.8\,fF)(2.7-0.3)}{.000112} = \boxed{0.5\,ns}$

Inverter for NAND

$\frac{C\,dV}{I_d}$

$= \frac{(4.12fF)(1.5)}{.000112} = \boxed{0.05\,ns}$

Inv #1

$\frac{C\,dV}{I_D} = \frac{(110\,fF)(2.4)}{.000112} = \boxed{1.4\,ns}$

Inv #2

$\frac{dV}{I_D} = \frac{(47\,fF)(2.4)}{.000242} = \boxed{0.116\,ns}$

Inv #3

$\frac{C\,dV}{I_D} = \frac{(328\,fF)(4)}{.000133} = \boxed{0.62\,ns} = \Delta t_1$

$\frac{(328\,fF)(4)}{.000189} = \boxed{4.3\,ns} = \Delta t_0$

Inv #4

$\frac{C\,dV}{I_D} = \frac{(200\times10^{-12}\,F)(4)}{.004} = \boxed{125\,ns}$

Noise Margin for Inv #3

$V_M = \frac{V_{TR} + \sqrt{\frac{k_p}{r_n}}(V_{DD} + V_{Tp})}{1 + \sqrt{\frac{k_p}{k_n}}}$

$\frac{1 + 0.38(5+1)}{1+0.38} = \boxed{2.38\,V} = V_M$

$g_{mn} = k_n(V_M - V_{Tn})$

$= \left(\frac{W}{L}\right)_n \cdot 50\times10^{-6} \cdot (V_M - V_{Tn})$

$= 3.53\times10^{-4} \cdot (1.38)$

$= \boxed{4.9\times10^{-4}}$ $= g_{mn}$

$g_{mp} = k_p(V_{DD} - V_M + V_{TO})$

$= (5\times10^{-5})(5 - 2.38 - 1)$

$= \boxed{8.1\times10^{-5}}$ $= g_{mp}$

$r_{on} = 1/\lambda_n I_{Dn}$

$= \left[(7\times10^{-2})(.00132)\right]^{-1} = \boxed{10741}$ $= r_o$

$r_{op} = 1/\lambda_p I_{Dp}$

$= 1/\left[(9\times10^{-2})(.00133)\right] = \boxed{10741}$ $= r_{op}$

$A_V = -(g_{mn} + g_{mp})(r_{on} \| r_{op})$

$= -(4.9\times10^{-4} + 8.1\times10^{-5}) \cdot (5370.5)$

$= \boxed{-3.1}$

$NM_L = V_M + (V_{DD} - V_M)/A_V$

$= 2.38 + (5 - 2.38)/-3.1$

$= \boxed{1.54}$

$NM_H = V_{DD} - V_M + V_M/A_V$

$= 5 - 2.38 + 2.38/-3.1$

$= \boxed{1.85}$

Estimate Propagation Delay!

$V_{IH} = V_M - \frac{V_M}{A_V}$

$= 2.38 - \frac{2.38}{-3.1}$

$= \boxed{3.15\ V}$

$NM_H = V_{OH} - V_{IH}$

$1.85 = V_{OH} - 3.15 \longrightarrow V_{OH} = 5$

$t_{phl} = \frac{(C_0 + C_p) V_{OH}/2}{k_p/2 (V_{DD} - V_{tp})^2}$ NAND

$\frac{(10.7 \times 10^{-15})(1.5\ V)}{(25 \times 10^{-6})(3 - 0.7)^2} = \boxed{0.112\ ns}$

PASS GATE

$t_{pd} = \frac{C_L \cdot \frac{V_{DD}}{2}}{I_{DLM} + I_{DLHP}}$

$= \frac{(44.8 \times 10^{-15}\ F)(\frac{3}{2})}{(.000148 + (.000265)}$

$= \boxed{0.16\ ns}$

$I_{DLHn} = \frac{(2.50 \times 10^{-6})}{2}(3 - 0.7)^2 + \frac{k_n}{2}(V_{DD} - \frac{V_{DD}}{2} - V_{tn})^2$

$= .000148\ A$

$I_{DHLP} = \frac{\frac{6}{1.5}(25 \times 10^{-6})}{2}(3 - 0.7)^2$

$= .000265\ A$

$\tau_{pd0} = .56ns + 0.16ns + 0.05ns + 0.12ns + 1.4ns + .16ns + 4.3ns + 125ns$

$= \boxed{131.75\ ns}$

$\tau_{pd_1} = 128.15\ ns$

Minimum Noise Margin

Inv 1

$L = 1.5$ $\quad W_n = 3$ $\quad W_p = 6$

$$V_M = \frac{V_{Tn} + \sqrt{\frac{k_p}{k_n}}(V_{DD} - V_{Tp})}{1 + \sqrt{\frac{k_p}{k_n}}} \qquad \text{since} \quad \frac{k_p}{k_n} = \frac{\left(\frac{W}{L}\right)_p (25\times10^{-6})}{\left(\frac{W}{L}\right)_n (50\times10^{-6})}$$

$$V_M = \frac{0.7 + (3 - 0.7)}{2} = 1.5\ V \;//\; V_M \qquad \frac{k_p}{k_n} = 1$$

$$g_{mn} = k_n(V_M - V_{Tn}) = (100\times10^{-6})(1.5 - 0.7) = 8\times10^{-5} \;//\; g_{mn}$$

$$g_{mp} = k_p(V_{DD} - V_M + V_{Tp}) = 50\times10^{-6}(3 - 1.5 - 0.7) = 4\times10^{-5} \;//\; g_{mp}$$

$$r_{on} = \frac{1}{\lambda I_D} = \frac{1}{(7\times10^{-3})(.1\,.0012)} = 119048$$

$r_{op} = r_{on} = 119047$

$r_{on} // r_{op} = 59524$

$$A_v = -(g_{mn} + g_{mp})(r_{on} // r_{op}) = -7.14 \;//\; A_v$$

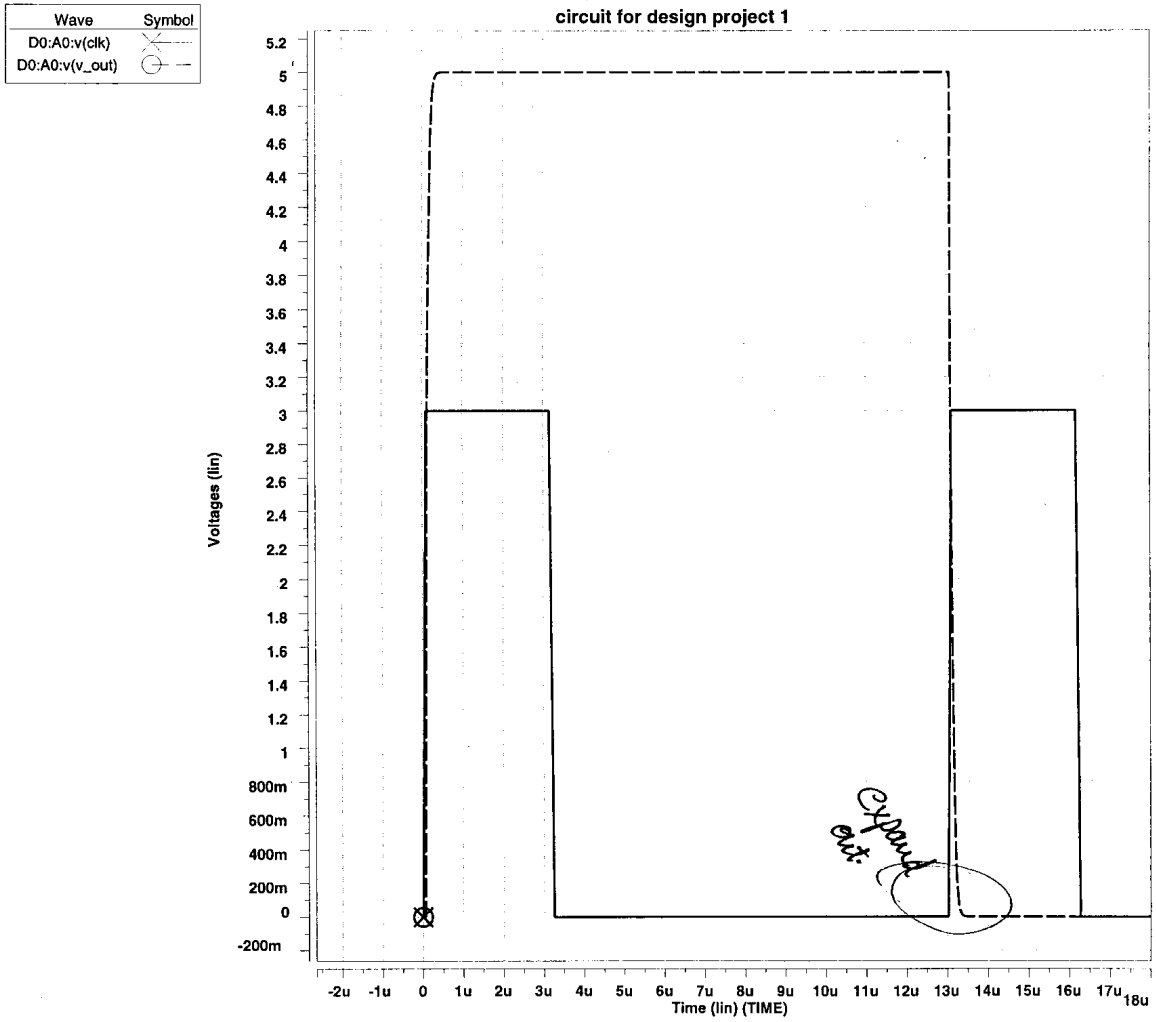
$$NM_L = V_M + (V_{DD} - V_M)/A_v = 1.5 + (3 - 1.5)/-7.14$$

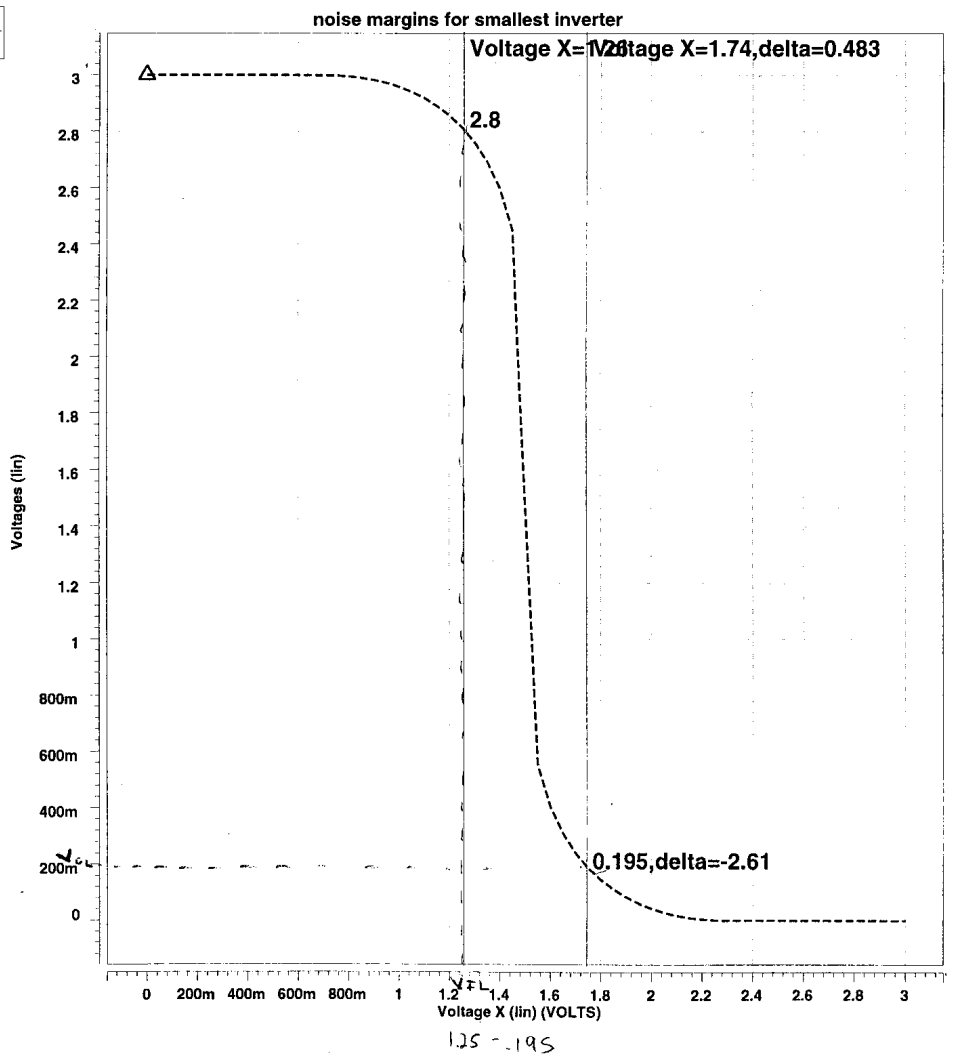
$$\boxed{NM_L = 1.29 = NM_H}$$ minimum!

All SPICE Code

```
*Simulated power dissipation from output file*
pdiss=  8.6840E-07  from=  0.0000E+00     to=  1.3330E-02

******************
*My MOSFET Models*
******************

.model NMOSL NMOS LEVEL=1 TOX=1.5E-08 VTO=0.7 KP=50E-06 LAMBDA=7E-02 CJ=1E-04
+ CJSW=5E-10 PB=0.9 *Low VT NMOS

.model PMOSL PMOS LEVEL=1 TOX=1.5E-08 VTO=-0.7 KP=25E-06 LAMBDA=7E-02 CJ=3E-04
+ CJSW=3.5E-10 PB=0.9 *Low VT PMOS

.model NMOSH NMOS LEVEL=1 TOX=1.5E-08 VTO=1.0 KP=50E-06 LAMBDA=7E-02 CJ=1E-04
+ CJSW=5E-10 PB=0.9 *High VT PMOS

.model PMOSH PMOS LEVEL=1 TOX=1.5E-08 VTO=-1.0 KP=25E-06 LAMBDA=7E-02 CJ=3E-04
+ CJSW=3.5E-10 PB=0.9 *High VT PMOS


*****************************
*Circuit for Design Project 1*
*****************************

.options post
.op
.inc 'mos_models' *includes the my mosfet models

vdd_3 vdd3 0 dc 3 *supply voltage vdd=3v *vdd for low vt
vdd_5 vdd5 0 dc 5 *supply voltage vdd=5v *vdd for high vt

vrs rs 0 pulse(0 3 0 100n 100n 6.5u 13.33m) *vrs pulse
vclk clk 0 pulse(0 3 0 100n 100n 3.055u 13.02u) *clock

venable enable 0 dc 3 *enable voltage = 3v

******************
*initial inverter*
******************
mninv1 inv_clk clk 0 0 nmosl l=1.5u w=3u pd=15u ps=15u ad=18p as=18p
mpinv1 inv_clk clk vdd3 vdd3 pmosl l=1.5u w=6u pd=18u ps=18u ad=36p as=36p

*************************
* the transmission gate *
*************************
mninv2tgate rs clk tg_out 0 nmosl l=1.5u w=3u pd=15u ps=15u ad=18p as=18p
mpinv2tgate tg_out inv_clk rs vdd3 pmosl l=1.5u w=6u pd=15u ps=15u ad=36p as=36p

************************
*inverter for nand gate*
************************
mninv3 tg_inv tg_out 0 0 nmosl l=1.5u w=3u pd=15u ps=15u ad=18p as=18p
mpinv3 tg_inv tg_out vdd3 vdd3 pmosl l=1.5u w=6u pd=18u ps=18u ad=36p as=36p

***************
*the nand gate*
***************
mninv4nand 1 tg_inv 0 0 nmosl l=1.5u w=3.0u pd=15u ps=15u ad=18p as=18p
mninv5nand nand_out enable 1 0 nmosl l=1.5u w=3.0u pd=15u ps=15u ad=18p as=18p
mpinv4nand nand_out tg_inv vdd3 vdd3 pmosl l=1.5u w=3.0u pd=15u ps=15u ad=18p as=18p
mpinv5nand nand_out enable vdd3 vdd3 pmosl l=1.5u w=3.0u pd=15u ps=15u ad=18p as=18p

*****************************
*buffer chain w/ 4 inverters*
```

```
************************
*Noise margins for Vout*
************************

.options post
.op
.inc 'mos_models' *includes the my mosfet models

vdd_3 vdd3 0 dc 3 *supply voltage vdd=3v *vdd for low vt
vdd_5 vdd5 0 dc 5 *supply voltage vdd=5v *vdd for high vt

mninv9 v_out 4 0 0 nmosh l=1.5u w=31.7u pd=43.7u ps=43.7u ad=190p as=190p
mpinv9 v_out 4 vdd5 vdd5 pmosh l=1.5u w=63.5u pd=75u ps=75u ad=381p as=381p

Vin 4 0 dc 0

.dc vin 0 5 .05

.end
```


Wave
Symbol
D0:A0:v(clk)
D0:A0:v(v_out)
circuit for design project 1
Voltages (lin)
5.2
5
4.8
4.6
4.4
4.2
4
3.8
3.6
3.4
3.2
3
2.8
2.6
2.4
2.2
2
1.8
1.6
1.4
1.2
1
800m
600m
400m
200m
0
-200m
-2u
-1u
0
1u
2u
3u
4u
5u
6u
7u
8u
9u
10u
11u
12u
13u
14u
15u
16u
17u
18u
Time (lin) (TIME)
expand
axis



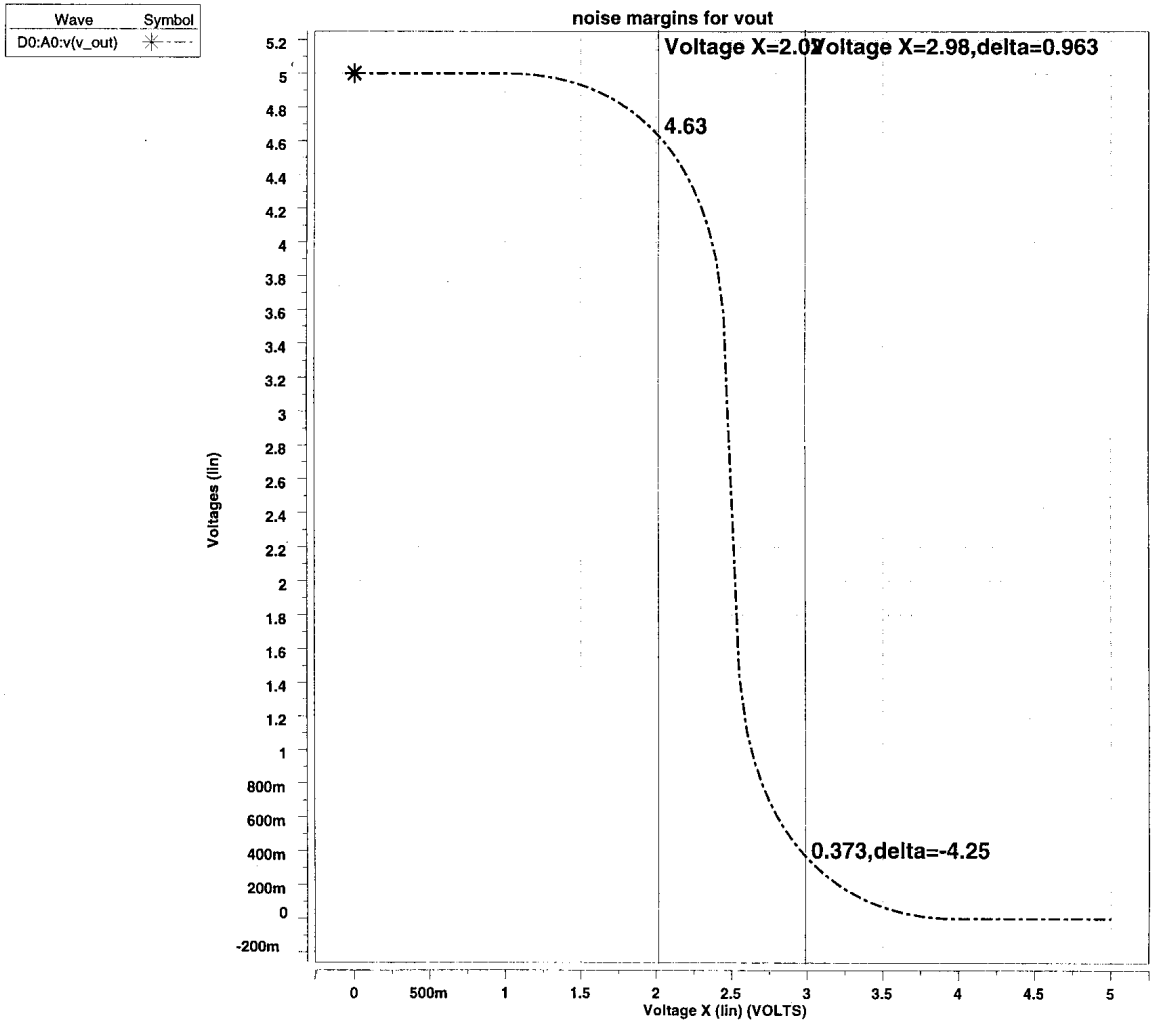
Minimum Noise Margin

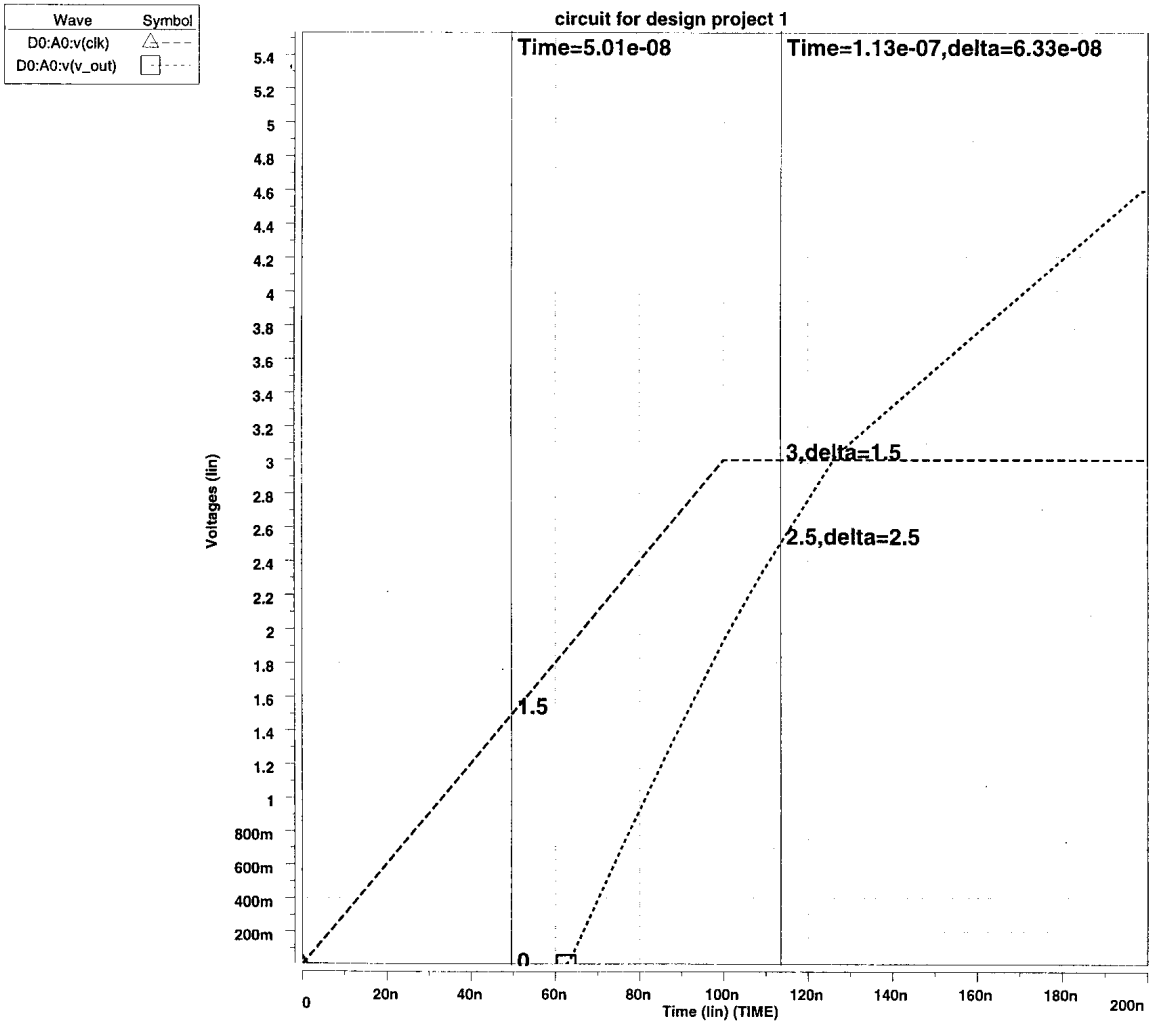
$NM_L = V_{IL} - V_{OL}$

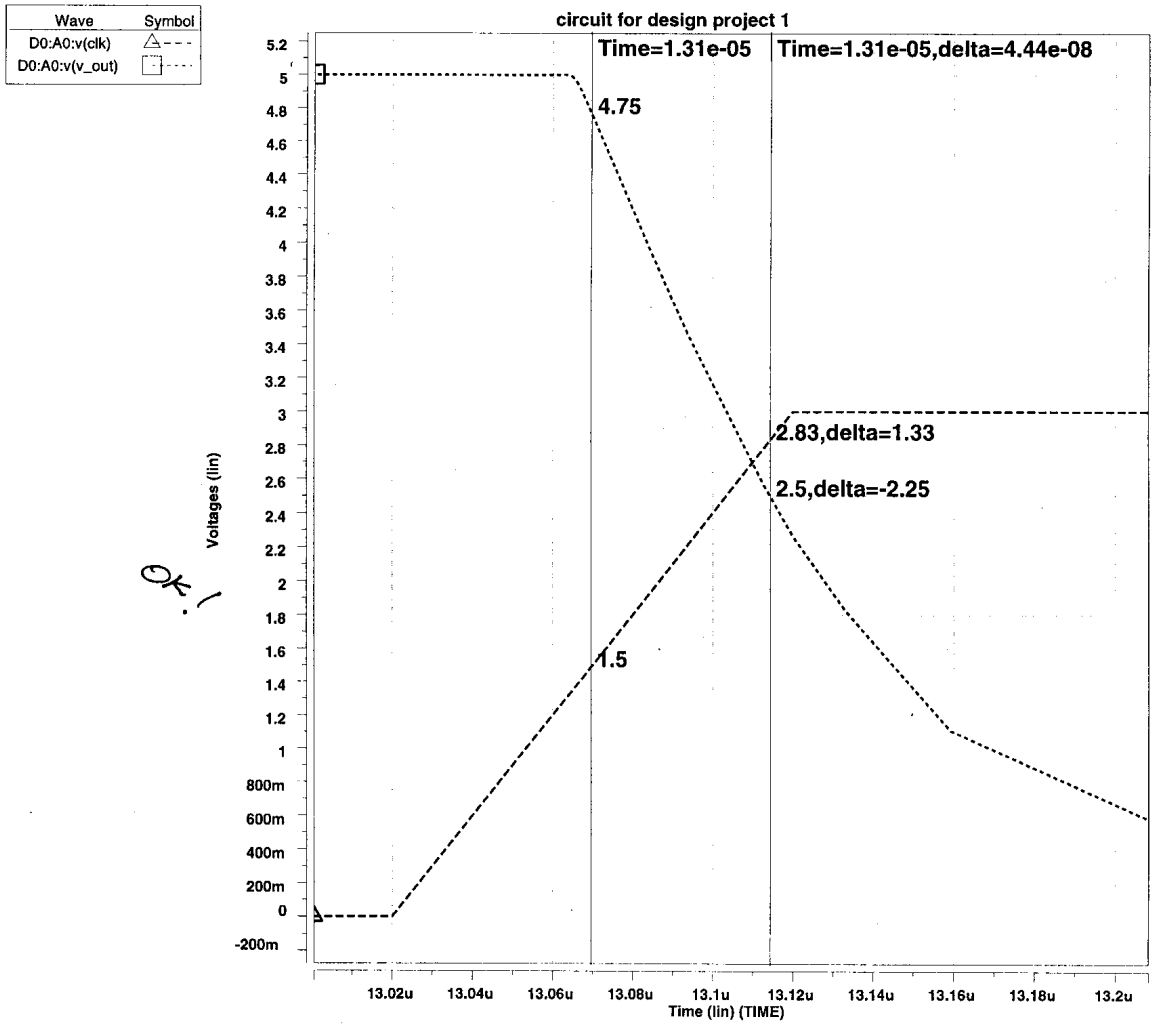
$= 1.25 - 0.195$

$= \boxed{1.055\ V}$

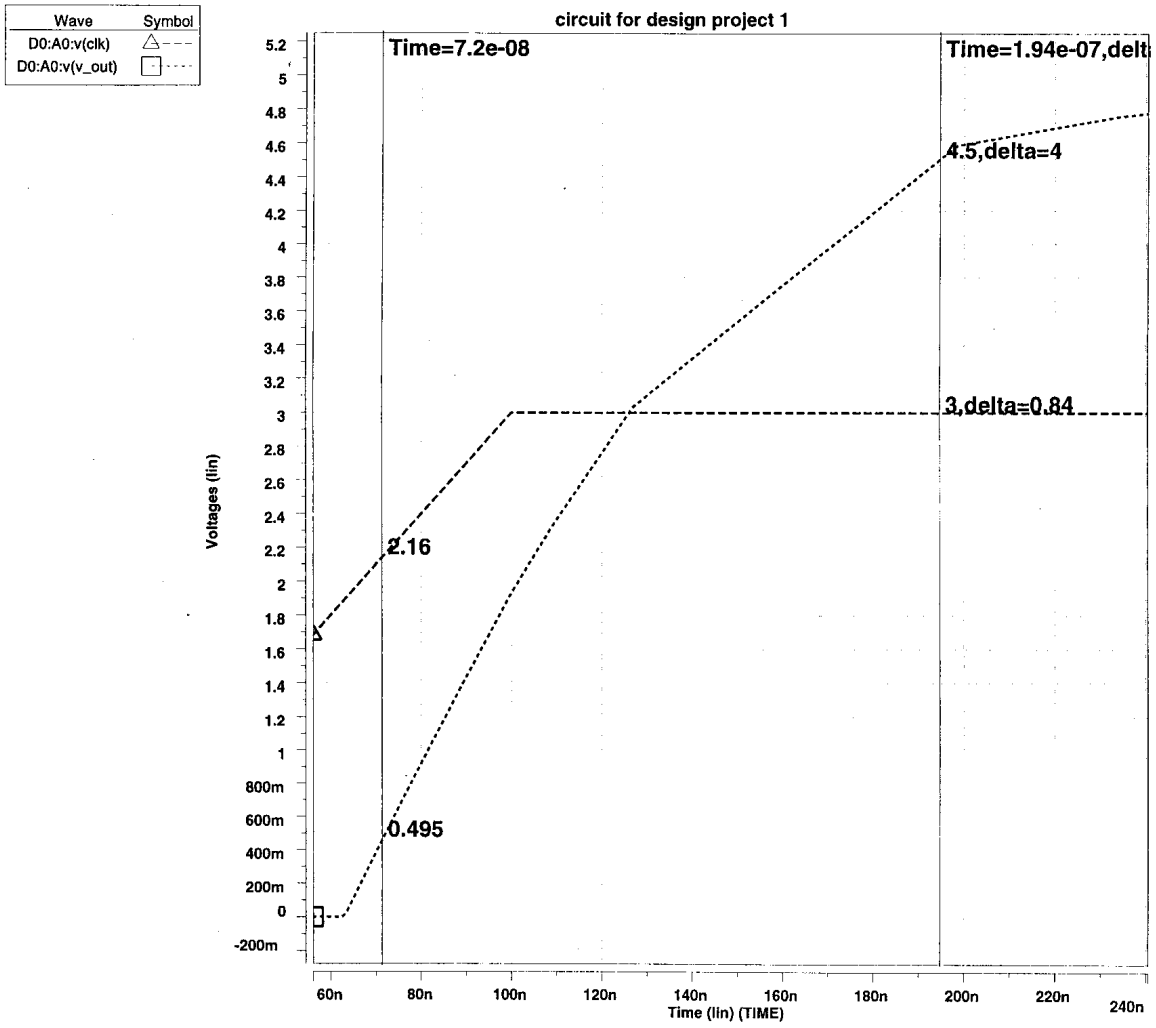
1.25 - .195

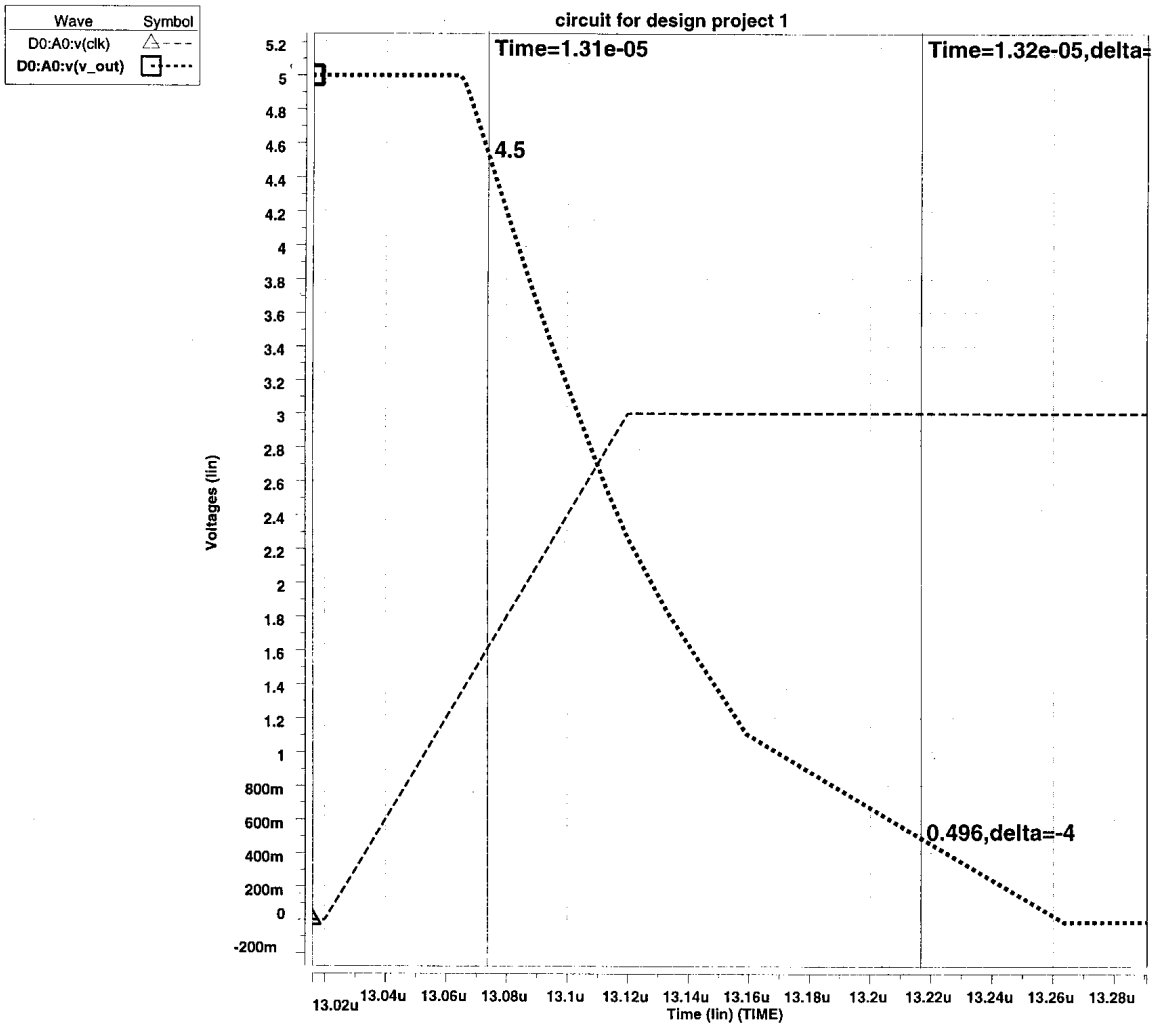

Wave
Symbol
D0:A0:v(v_out)
noise margins for vout
Voltage X=2.02
Voltage X=2.98,delta=0.963
4.63
0.373,delta=-4.25
Voltages (lin)
Voltage X (lin) (VOLTS)
5.2
5
4.8
4.6
4.4
4.2
4
3.8
3.6
3.4
3.2
3
2.8
2.6
2.4
2.2
2
1.8
1.6
1.4
1.2
1
800m
600m
400m
200m
0
-200m
0
500m
1
1.5
2
2.5
3
3.5
4
4.5
5


Wave
Symbol
D0:A0:v(clk)
D0:A0:v(v_out)
circuit for design project 1
Time=5.01e-08
Time=1.13e-07,delta=6.33e-08
3,delta=1.5
2.5,delta=2.5
1.5
0
Voltages (lin)
Time (lin) (TIME)
5.4
5.2
5
4.8
4.6
4.4
4.2
4
3.8
3.6
3.4
3.2
3
2.8
2.6
2.4
2.2
2
1.8
1.6
1.4
1.2
1
800m
600m
400m
200m
0
20n
40n
60n
80n
100n
120n
140n
160n
180n
200n


Wave
Symbol
D0:A0:v(clk)
D0:A0:v(v_out)
circuit for design project 1
Time=1.31e-05
Time=1.31e-05,delta=4.44e-08
4.75
2.83,delta=1.33
2.5,delta=-2.25
1.5
Voltages (lin)
5.2
5
4.8
4.6
4.4
4.2
4
3.8
3.6
3.4
3.2
3
2.8
2.6
2.4
2.2
2
1.8
1.6
1.4
1.2
1
800m
600m
400m
200m
0
-200m
13.02u
13.04u
13.06u
13.08u
13.1u
13.12u
13.14u
13.16u
13.18u
13.2u
Time (lin) (TIME)

Ok. 1


Wave
Symbol
D0:A0:v(clk)
D0:A0:v(v_out)
circuit for design project 1
Time=7.2e-08
Time=1.94e-07,delt
4.5,delta=4
3,delta=0.84
2.16
0.495
Voltages (lin)
5.2
5
4.8
4.6
4.4
4.2
4
3.8
3.6
3.4
3.2
3
2.8
2.6
2.4
2.2
2
1.8
1.6
1.4
1.2
1
800m
600m
400m
200m
0
-200m
60n
80n
100n
120n
140n
160n
180n
200n
220n
240n
Time (lin) (TIME)


Wave
Symbol
D0:A0:v(clk)
D0:A0:v(v_out)
circuit for design project 1
Time=1.31e-05
Time=1.32e-05,delta=
4.5
0.496,delta=-4
Voltages (lin)
5.2
5
4.8
4.6
4.4
4.2
4
3.8
3.6
3.4
3.2
3
2.8
2.6
2.4
2.2
2
1.8
1.6
1.4
1.2
1
800m
600m
400m
200m
0
-200m
13.02u
13.04u
13.06u
13.08u
13.1u
13.12u
13.14u
13.16u
13.18u
13.2u
13.22u
13.24u
13.26u
13.28u
Time (lin) (TIME)