Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science
6.012 Electronic Devices and Circuits
Fall 2000

Design Problem #2 – Amplifiers
Handed out: 11/21/2000
Due: 12/8/2000

1.0 Introduction

In this project you will design a two-stage amplifier consisting of two cascaded common source stages as shown in Figure 1. The NMOS transistor M_{n1} is in a common source configuration with the PMOS M_{p1} as the supply current. The source input resistance is 1 kΩ. M_{n2} is configured as the second common source stage with M_{p2} as the supply current of that stage. The load is a 1 pF capacitance.

Your assignment will be to design for V_{BIAS}, V_A, V_B, and the (W/L) of each of the four field effect transistors. Your design must meet specifications relating to voltage gain, bandwidth, total voltage swing, and power dissipation. You can modify the given design if you see a better way to meet the specifications.

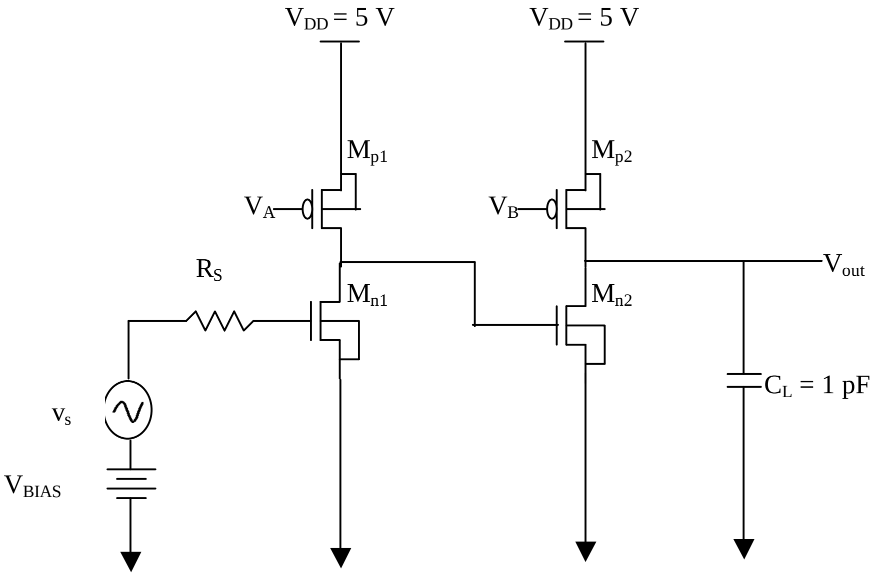

Figure 1: Circuit topology of two-stage amplifier.

2.0 Design Specifications

Your amplifier must be designed to meet these specifications:

1. Voltage gain, $|A_v| = v_{out}/v_s > 7500$ (77.5 dB)
2. a) 3dB frequency, $f_{3dB} > 100$ kHz.
   b) Unity gain frequency, $f_{UNITY} > 40$ MHz (see Figure 2).
3. The output voltage swing, $(V_{outmax} - V_{outmin}) > 3$ volts (see Figure 3).
4. The total power dissipation, $P_D < 100\ \mu W$.

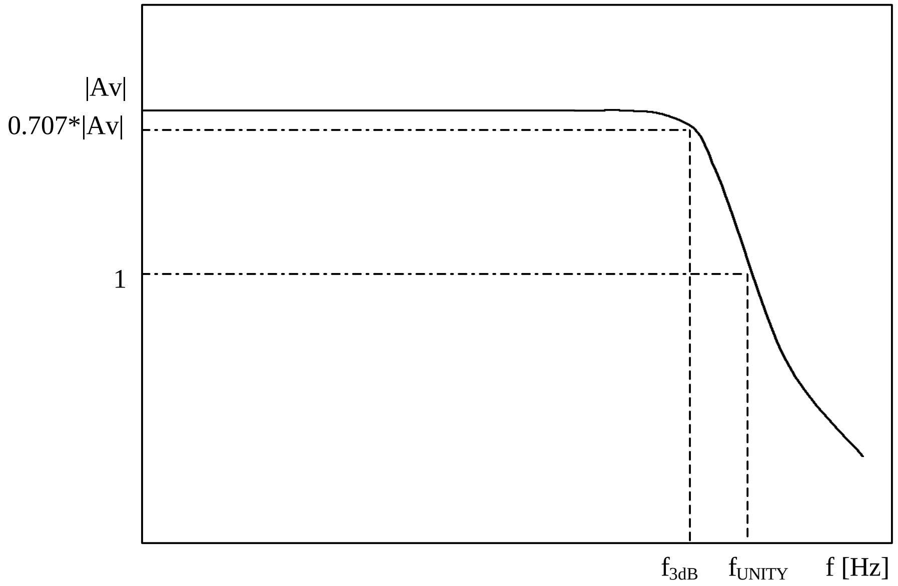

Figure 2: Gain vs. frequency.

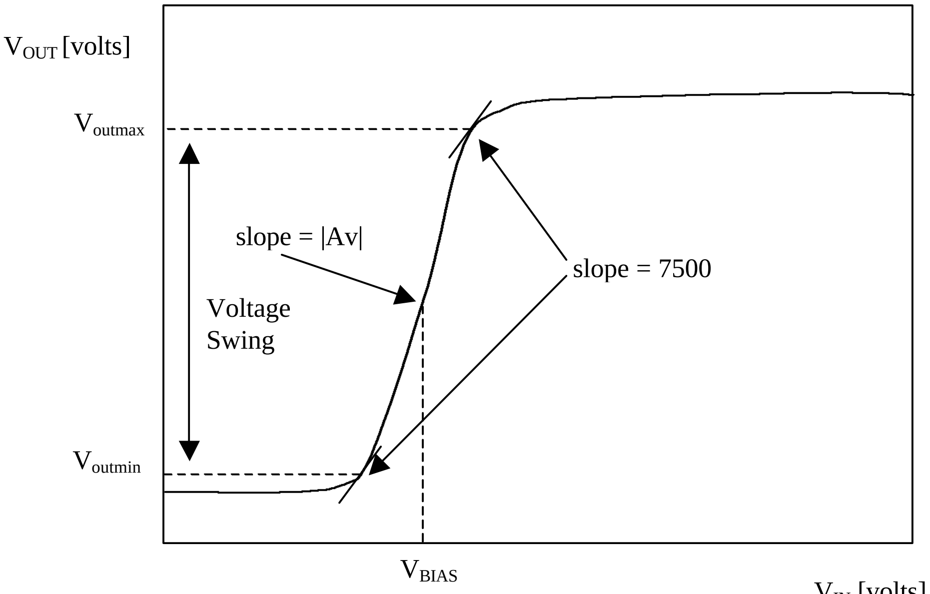

Figure 3: V_{OUT} vs. V_{IN}.

3.0 HSPICE model parameters

The device parameters for your FETs are described in Table 1. Your fabrication process is capable of a minimum length, L_{min} = 1.5 µm, and a minimum width, W_{min} = 6 µm, for both NMOS and PMOS. Please note that some of the parameters that are given to you will be different from those in design problem #1.

Parameter	NMOS	PMOS
μC_{ox}	50 $\mu A/V^2$	25 $\mu A/V^2$
V_T	0.7 V	-0.7 V
C_{ox}	2 $fF/\mu m^2$	2 $fF/\mu m^2$
C_{ov}	0.5 fF/µm	0.5 fF/µm
C_{jo}	0.1 $fF/\mu m^2$	0.3 $fF/\mu m^2$
C_{jsw}	0.5 fF/µm	0.35 fF/µm
W_{min}	6 µm	6 µm
L_{min}	1.5 µm	1.5 µm
L_{diff}	6 µm	6 µm
λ	(0.1 µm/L) V^{-1}	(0.1 µm/L) V^{-1}

Table 1: Device Parameters.

Also keep in mind that λ depends on the channel length, L. So, you will need to have a different model for each transistor with a different length. The models shown below are for a transistor with length L=1.5µm.

```
.MODEL N1 NOMS LEVEL=1 VTO=0.7 TOX=1.5E-08 UO=220
+LAMBDA=6.7E-02 GAMMA=0.6 CGSO=1E-9 CGDO=1E-9 CH=1.0E-04
+CJSW=5.0E-10 PB=0.95

.MODEL N1 NOMS LEVEL=1 VTO=0.7 TOX=1.5E-08 UO=220
+LAMBDA=6.7E-02 GAMMA=0.6 CGSO=1E-9 CGDO=1E-9 CH=3.0E-04
+CJSW=3.5E-10 PB=0.9
```

4.0 HSPICE Analysis

Before attempting an AC simulation on HSPICE, you will need to do a DC sweep on the input voltage to find the exact value for V_{BIAS} such that the circuit is operating in its high-gain region. V_{BIAS} is the input voltage where the output is in the middle of the high-gain region. The range of V_{BIAS} is very small for high gain circuits, so you will need to make very small steps in order to increase the accuracy. To do a DC sweep you will need SPICE cards similar to the following:

```
vin 1 0 ac=1,0 dc=X
.dc vin 0 5 0.001
```

In the first line, a vin between nodes 1 and 0 is specified, with an ac small signal magnitude of 1 V and phase of 0 and a DC offset of X V. When doing a DC sweep, the specified AC and DC values on this line are irrelevant. The next line sweeps the vin source from 0 to 5 V in steps of 1 mV. Figure 3 shows a sample transfer characteristic and you could find the value for V_{BIAS} from the characteristics. You could also determine the voltage swing from this graph by measuring the range of output values for which the circuit will have the specified gain. You will need to repeat this procedure (finding V_{BIAS}) every time you change your design. You will need to hand in this DC transfer characteristic graph. Clearly demarcate the maximum and minimum voltage as well as the output voltage range on the transfer characteristic

To simulate the gain and bandwidth of your amplifier, an AC analysis must be done as follows:

```
vin 1 0 ac=1,0 dc=X
.ac vin dec  40 1 1g
```

The second line specifies an AC analysis from 1 Hz to 40 GHz with 40 points per decade. You must plot the gain as a function of frequency and clearly show the f3dB point as well as the f_{UNITY} point. A_v must be labeled on the plot.

In analog circuits, power dissipation is completely static. The power supply current times the power supply voltage. To determine the current through each of the MOSFETs as well as the total power dissipation, include:

```
.op
```

5.0 Report

You are expected to submit a complete report. Your report must describe your design in a clear (neatness counts), concise, and complete manner. The report must be divided in the following parts:

Design Summary (1 page only)
Report on all of the design variables, as well as the key results of the hand calculations and simulations.

Approach (1 page only)
Explain your thought process and approach. Discuss design tradeoffs that you discovered.

Circuit Schematic (1 page only)
Neatly draw your final circuit, labeling the transistor names, nodes, and device sizes.

Hand Calculations (4 pages maximum)
Show your final circuit hand calculations for gain, f_{3dB}, f_{UNITY}, output swing, and power. If you use MATLAB, Excel, or any other software, show the formulas used and the final outputs. Make sure all of the calculations are neat and easy to follow.

Final HSPICE input files (1 page maximum)
In addition to a hard copy, please make the file available in your public directory.

HSPICE output Plots (2 pages maximum)
Include the transfer characteristic for the amplifier circuit (v_{out} vs. v_s) as well as the gain vs. frequency plot. Clearly label V_{BIAS}, gain, f_{3dB}, f_{UNITY}, and voltage swing on these plots.

6.0 Grading

Most of the points will be allocated for a design that meets all the specifications accompanied with a well-written report. The remainder of the points will be allocated for beating the specifications. You are expected to beat the specifications. Points will be given for low power dissipation, a large gain, and a large f_{3dB} and f_{UNITY}. If you believe that you can exceed the design specifications more effectively by modifying the topology of the amplifier, you are welcome to do so. If you do, please discuss it in the report. Those who improve the design will be rewarded.