Lecture 12
Digital Circuits (II)
MOS INVERTER CIRCUITS

Outline

- NMOS inverter with resistor pull-up
  - –Transient Characteristics
- NMOS inverter with current-source pull-up
- Complementary MOS (CMOS) Inverter

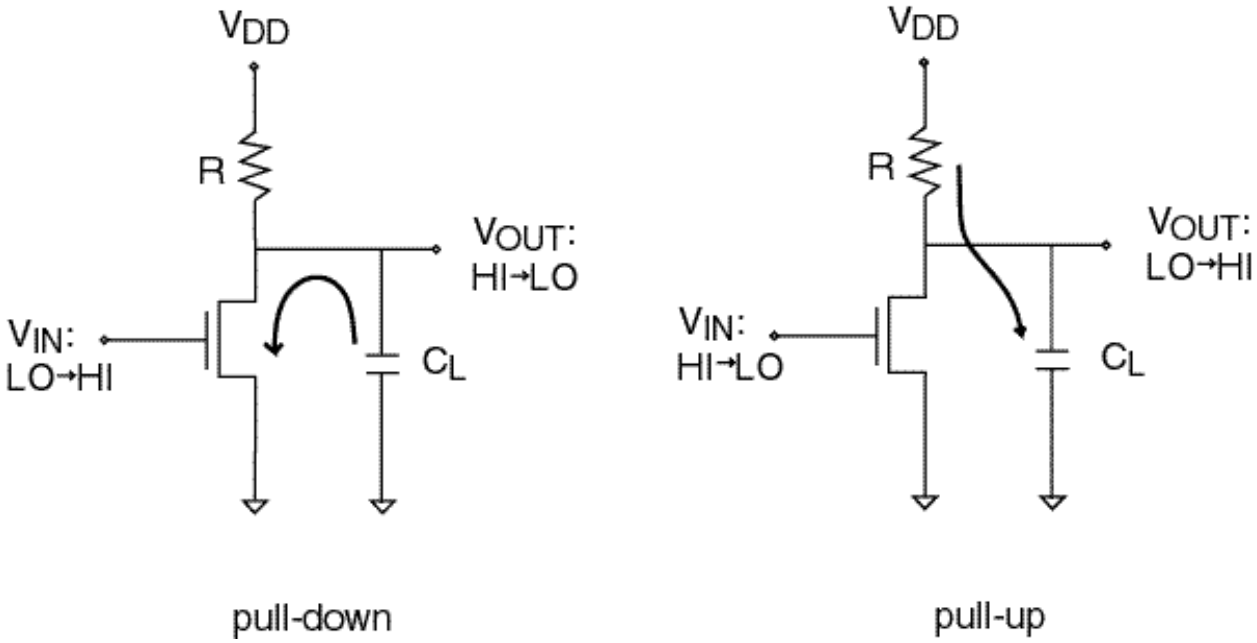
Reading Assignment:
Howe and Sodini; Chapter 5, Sections 5.3
Howe and Sodini; Chapter 13 Section 13.5.3 (Design #1)

Summary of Key Concepts

- In NMOS inverter with resistor pull-up, there is a **trade-off between noise margin and speed**
- Trade-off resolved using current source pull-up
  - Use PMOS as current source.
- In NMOS inverter with current-source pull-up: if V_{IN} = High, there is **power consumption** even if inverter is idle.
- Complementary MOS: NMOS and PMOS switch-on alternatively.
  - No current path between power supply and ground
  - **No power consumption while idle**

1. NMOS inverter with resistor pull-up: Dynamics

- C_L ***pull-down*** limited by current through transistor
  - [shall study this issue in detail with CMOS]
- C_L ***pull-up*** limited by resistor ($t_{PLH} \approx RC_L$)
- Pull-up slowest



1. NMOS inverter with resistor pull-up: Inverter design issues

Noise margins ↑ $|A_v|$ ↑

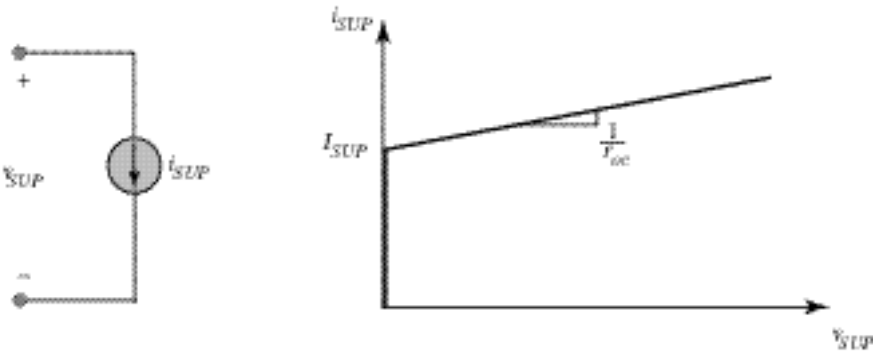
- R ↑ $|RC_L|$ ↑ slow switching
- g_m ↑ $|W|$ ↑ big transistor
  - (slow switching at input)

Trade-off between speed and noise margin.

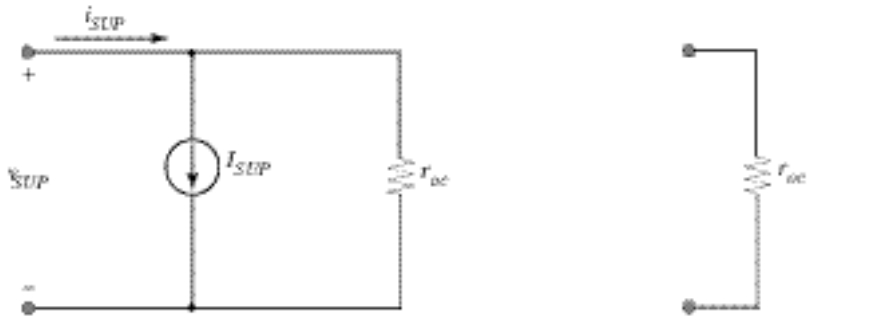
use ***current source*** as pull-up

2. NMOS inverter with current-source pull-up

I—V characteristics of current source:



Equivalent circuit models :

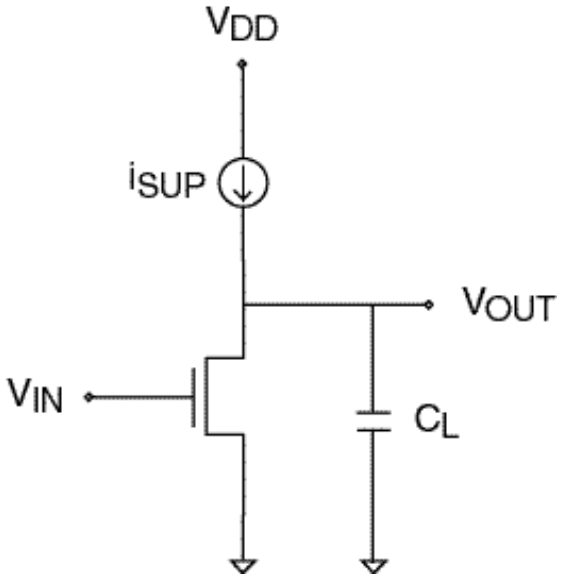


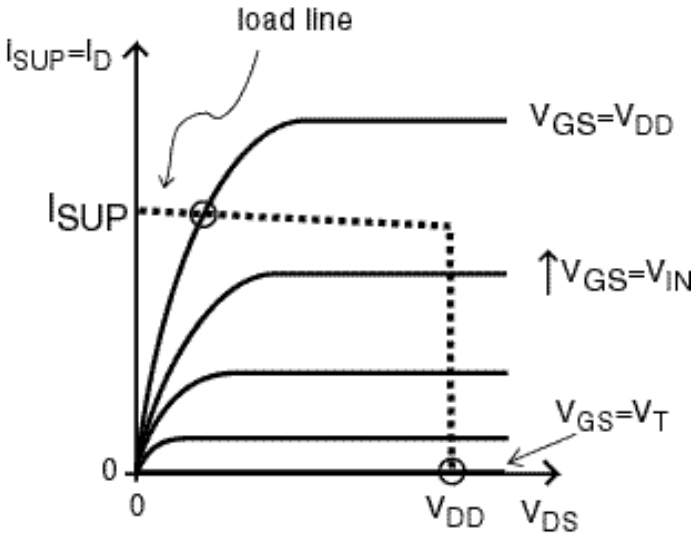
large-signal model small-signal model

- High current throughout voltage range
  - $i_{SUP} \leq I_{SUP}$
- High small-signal resistance $r_{oc.}$

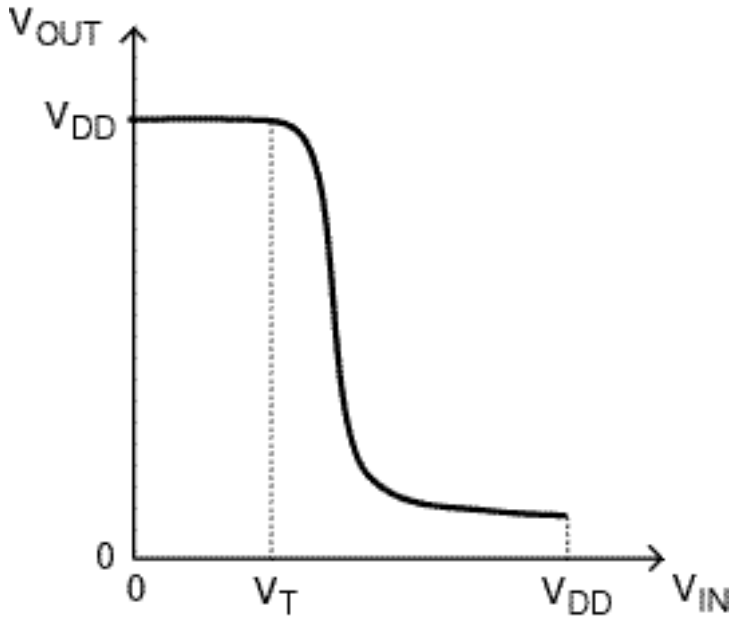
NMOS inverter with current-source pull-up

Static Characteristics





Inverter characteristics :



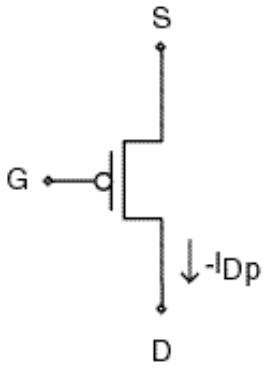
High r_{oc} high noise margins

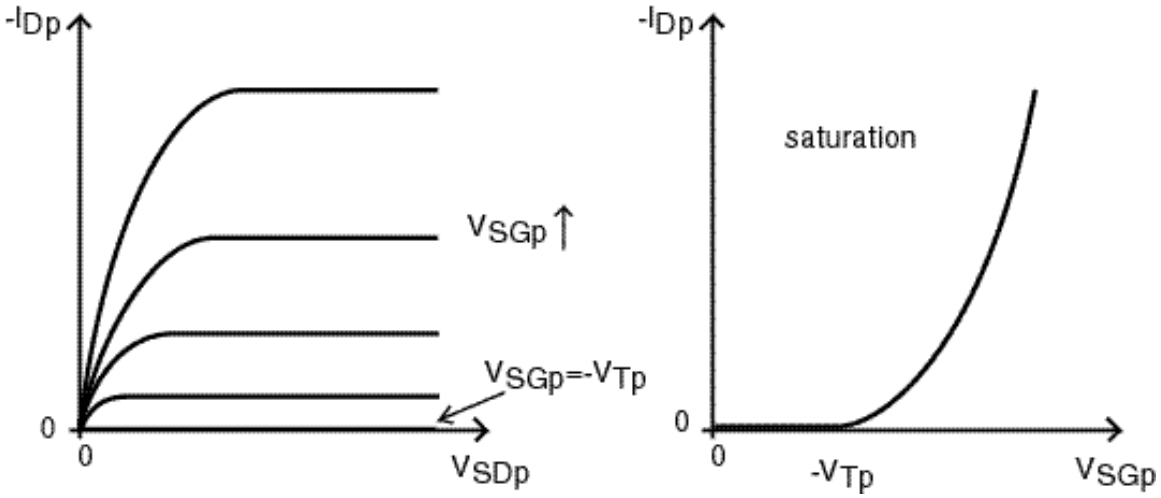
NMOS inverter with current-source pull-up
Dynamics

Faster pull-up because capacitor charged at constant current.

PMOS as current-source pull-up

I-V characteristics of PMOS:





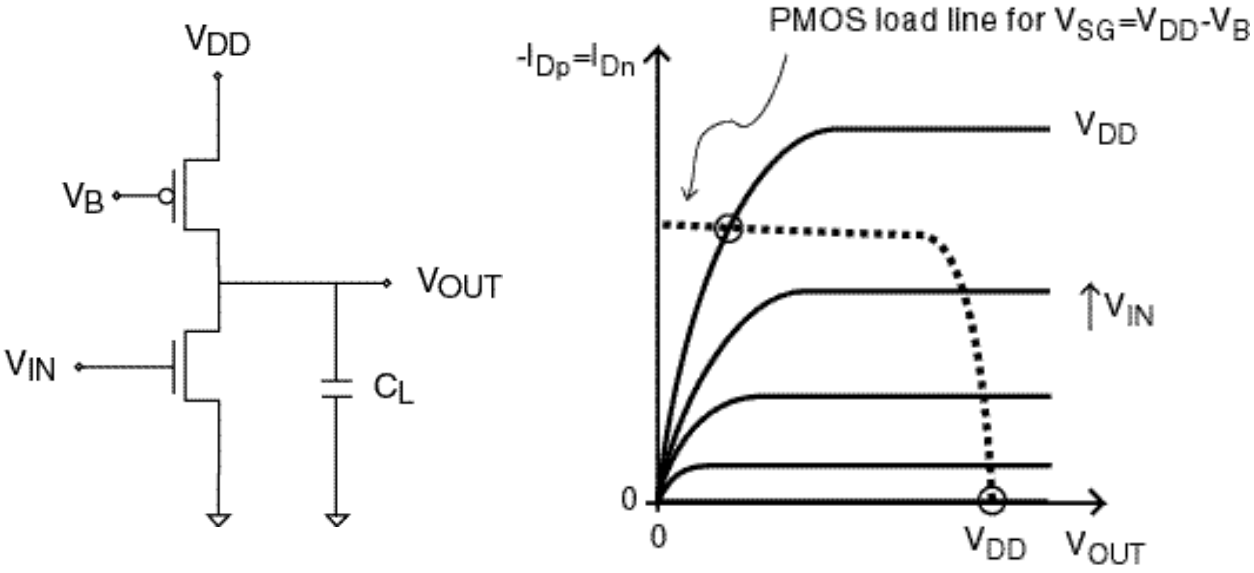
Note: enhancement-mode PMOS has $V_{Tp} < 0$.

In saturation:

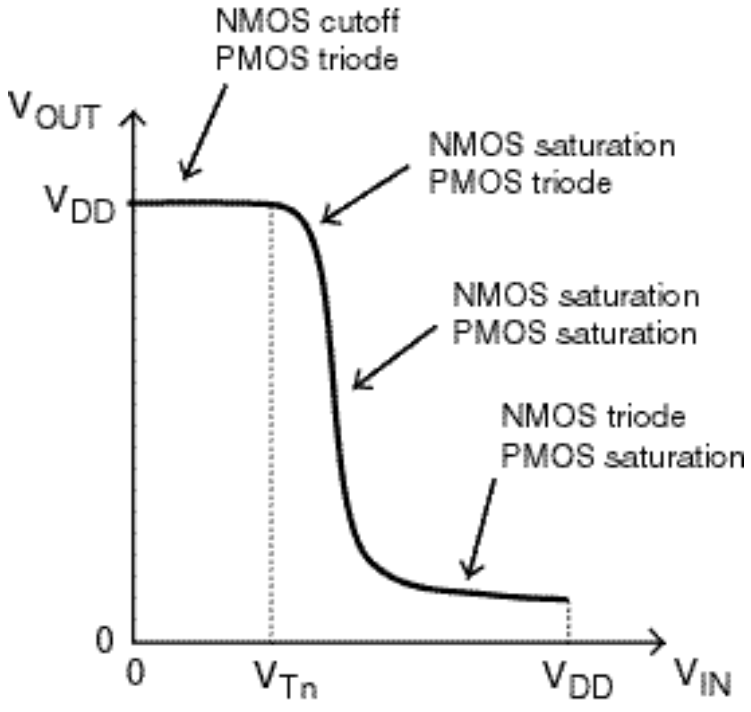
$$-I_{Dp} \quad \left(V_{SG} + V_{Tp}\right)^2$$

PMOS as current-source pull-up:

Circuit and load-line diagram of inverter with PMOS current source pull-up:



Inverter characteristics:



PMOS as current-source pull-up: Noise margin

- Compute $V_M = V_{IN} = V_{OUT}$
- Compute $|A_v(V_M)|$

At V_M both transistors are saturated:

$$I_{Dn} = \frac{W_n}{2L_n}\mu_n C_{ox}\left(V_M - V_{Tn}\right)^2$$

$$-I_{Dp} = \frac{W_p}{2L_p}\mu_p C_{ox}\left(V_{DD} - V_B + V_{Tp}\right)^2$$

And:

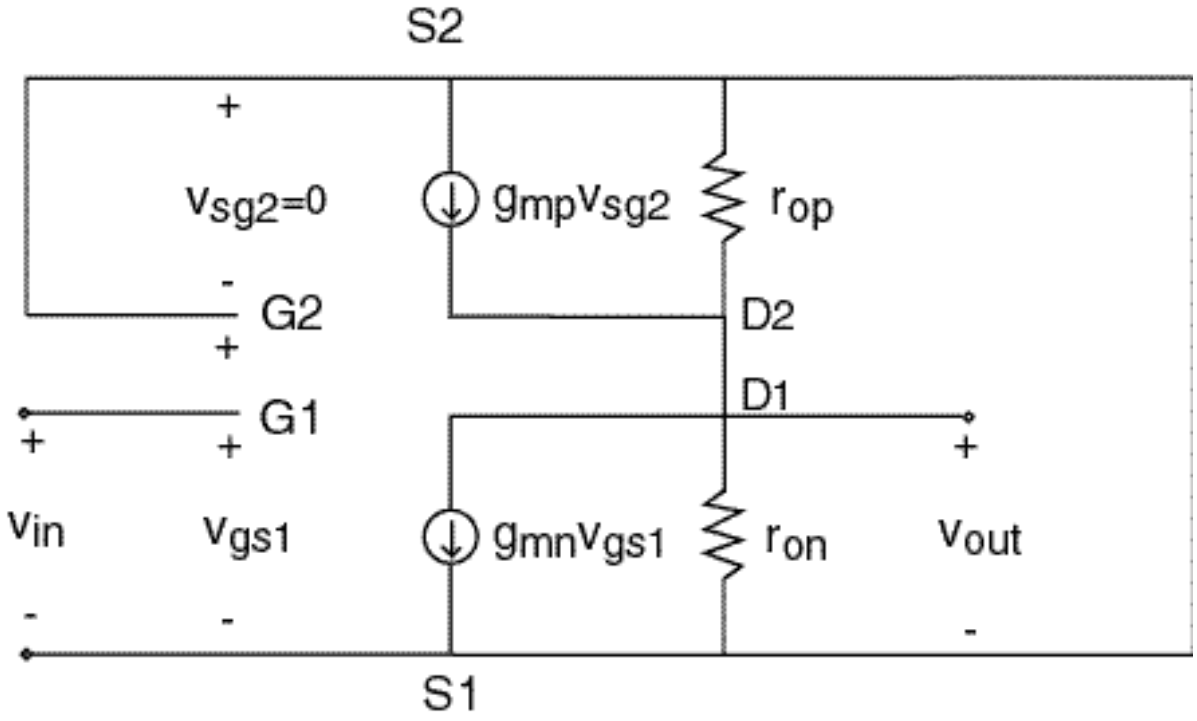
$$I_{Dn} = -I_{Dp}$$

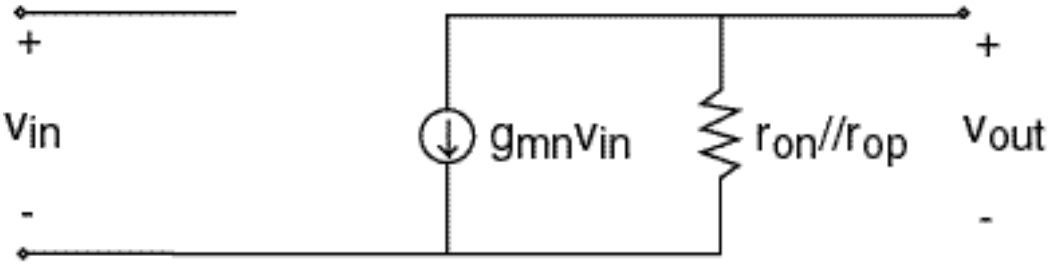
Then:

$$V_M = V_{Tn} + \sqrt{\frac{\mu_p \frac{W_p}{L_p}}{\mu_n \frac{W_n}{L_n}}}\left(V_{DD} - V_B + V_{Tp}\right)$$

PMOS as current-source pull-up:

Small-signal equivalent circuit model for V_M





$$A_v - g_{mn}\left(r_{on} // r_{op}\right)$$

PMOS as current-source pull-up:

NMOS inverter with current-source pull-up allows ***fast switching*** with high ***noise margins***

But…

When $V_{IN} = V_{DD}$, there is a direct current path between supply and ground

power is consumed even if the inverter is idle.

Ideally, we would like to have a current source that is ***itself*** switchable, i.e it shuts off when input is high

CMOS!

3. Complementary MOS (CMOS) Inverter

Circuit schematic:

- $V_{IN} = 0$ $V_{OUT} = V_{DD}$
  - $V_{GSn} = 0 < V_{Tn}$ **NMOS OFF**
  - $V_{SGp} = V_{DD} > -V_{Tp}$ **PMOS ON**
- $V_{IN} = V_{DD}$ $V_{OUT} = 0$
  - $V_{GSn} = V_{DD} > V_{Tn}$ **NMOS ON**
  - $V_{SGp} = 0 < -V_{Tp}$ **PMOS OFF**

No power consumption while idle in any logic state!

What did we learn today?

Summary of Key Concepts

- In NMOS inverter with resistor pull-up, there is a **trade-off between noise margin and speed**
- Trade-off resolved using current source pull-up
  - **Use PMOS as current source**.
- In NMOS inverter with current-source pull-up: if V_{IN} = High, there is power consumption even if inverter is idling.
- Complementary MOS: **NMOS and PMOS switch-on alternatively**.
  - No current path between power supply and ground
  - **No power consumption while idling**