Lecture 13
Digital Circuits (III)
CMOS CIRCUITS

Outline

- Complementary MOS (CMOS) Inverter: **introduction**
- CMOS inverter: **noise margins**
- CMOS Inverter: **propagation delay**

Reading Assignment:
Howe and Sodini; Chapter 5, Sections 5.4, 5.5 & 5.7

Summary of Key Concepts

Key features of CMOS inverter:

- No current between power supply and ground while inverter is idle in any logic state
- "rail-to-rail" logic
  - Logic levels are 0 and V_{DD}.
- High $|A_v|$ around the logic threshold
  - Good noise margins.

CMOS inverter logic threshold and noise margins engineered through W_n/L_n and W_p/L_p.

Key dependencies of propagation delay:

- $V_{DD} \uparrow \quad t_p \downarrow$
- $L \downarrow \quad t_p \downarrow$

1. Complementary MOS (CMOS) Inverter

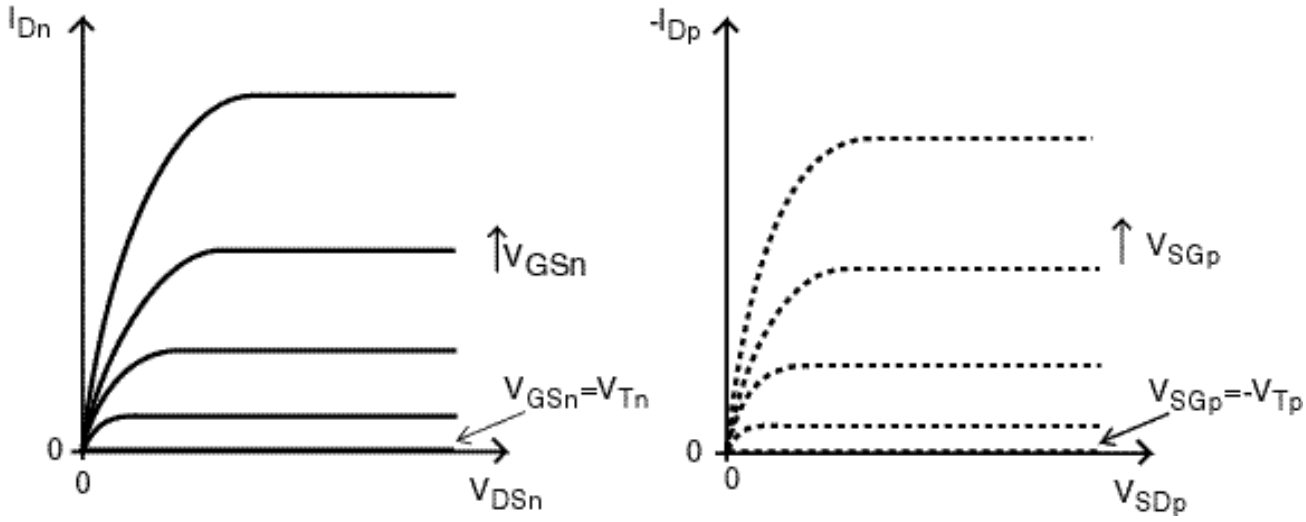
Circuit schematic:

- $V_{IN} = 0$ $V_{OUT} = V_{DD}$
  - $V_{GSn} = 0$ ($< V_{Tn}$) **NMOS OFF**
  - $V_{SGp} = V_{DD}$ ($> -V_{Tp}$) **PMOS ON**
- $V_{IN} = V_{DD}$ $V_{OUT} = 0$
  - $V_{GSn} = V_{DD}$ ($> V_{Tn}$) **NMOS ON**
  - $V_{SGp} = 0$ ($< -V_{Tp}$) **PMOS OFF**

No power consumption while idle in any logic state!

CMOS Inverter (Contd.):

Output characteristics of both transistors:



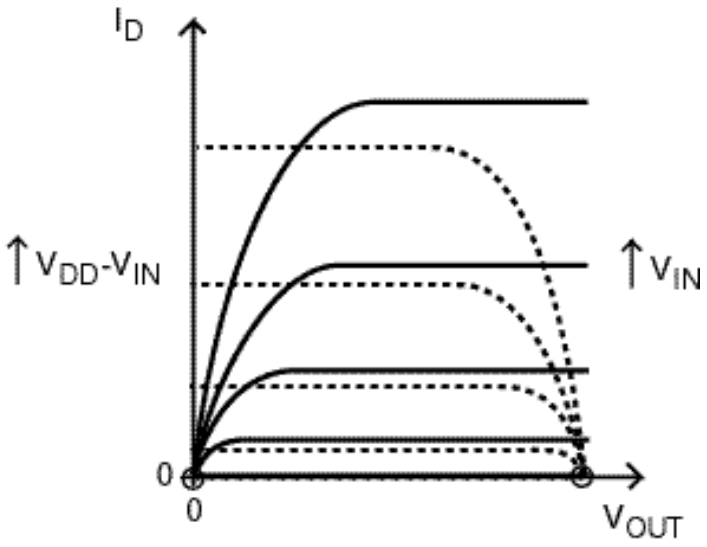
Note:

$V_{IN} = V_{GSn} = V_{DD} - V_{SGp}$ $\quad V_{GSp} = V_{DD} - V_{IN}$

$V_{OUT} = V_{DSn} = V_{DD} - V_{SDp}$ $\quad V_{SDp} = V_{DD} - V_{OUT}$

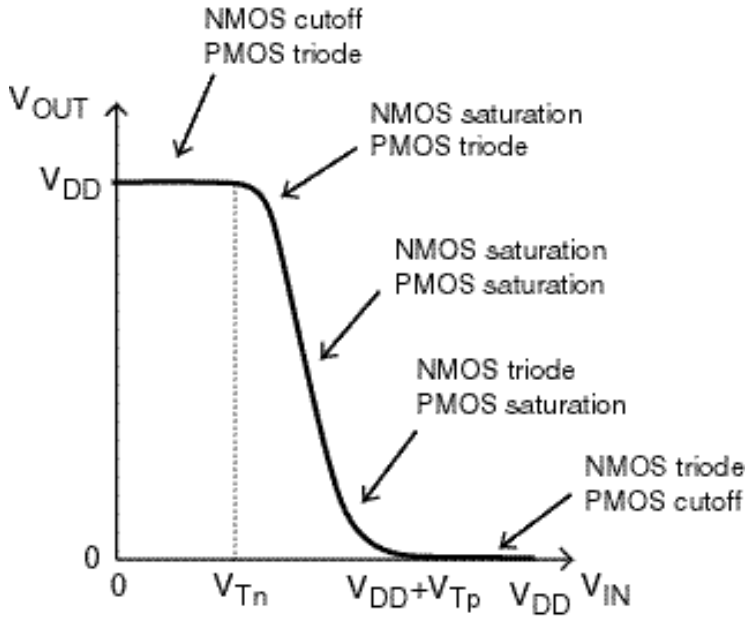
$I_{Dn} = -I_{Dp}$

Combine into single diagram of I_D vs. V_{OUT} with V_{IN} as parameter



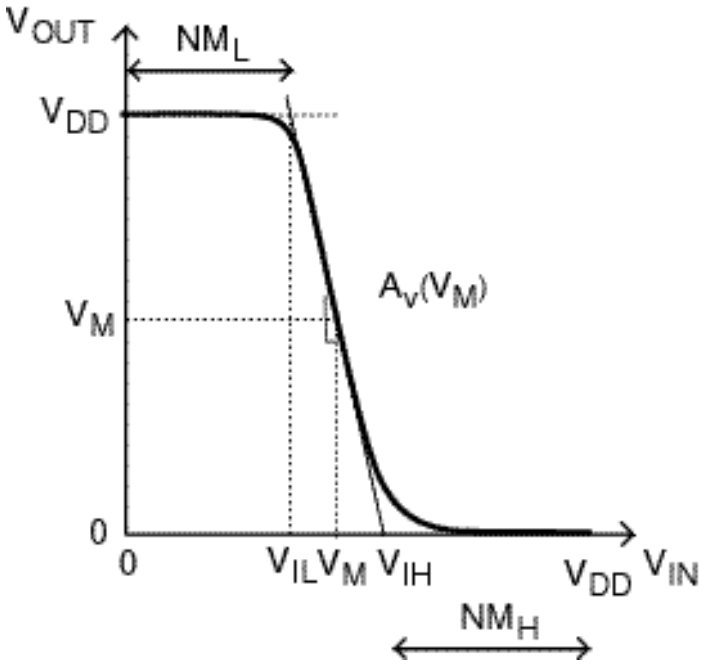
- *No current while idle in any logic state*

Inverter Characteristics:



- *"rail-to-rail" logic: logic levels are 0 and V_{DD}*
- *High $|A_v|$ around logic threshold*
  good noise margins

2. CMOS inverter: noise margins



- Calculate V_M
- Calculate $A_v(V_M)$
- Calculate NM_L and NM_H

Calculate V_M ($V_M = V_{IN} = V_{OUT}$)

At V_M both transistors are saturated:

$$I_{Dn} = \frac{W_n}{2L_n}\mu_n C_{ox}\left(V_M - V_{Tn}\right)^2$$

$$-I_{Dp} = \frac{W_p}{2L_p}\mu_p C_{ox}\left(V_{DD} - V_M + V_{Tp}\right)^2$$

CMOS inverter: noise margins (contd.)

Define:

$$k_n = \frac{W_n}{L_n}\mu_n C_{ox}; \qquad k_p = \frac{W_p}{L_p}\mu_p C_{ox}$$

Since :

$$I_{Dn} = -I_{Dp}$$

Then:

$$\frac{1}{2}k_n\left(V_M - V_{Tn}\right)^2 = \frac{1}{2}k_p\left(V_{DD} - V_M + V_{Tp}\right)^2$$

Solve for V_M:

$$V_M = \frac{V_{Tn} + \sqrt{\frac{k_p}{k_n}}\left(V_{DD} + V_{Tp}\right)}{1 + \sqrt{\frac{k_p}{k_n}}}$$

Usually, V_{Tn} and V_{Tp} fixed and $V_{Tn} = -V_{Tp}$
V_M engineered through k_p/k_n ratio.

CMOS inverter: noise margins (contd..)

- **Symmetric case**: $k_n = k_p$

$$V_M = \frac{V_{DD}}{2}$$

This implies:

$$\frac{k_p}{k_n} = 1 = \frac{\frac{W_p}{L_p}\mu_p C_{ox}}{\frac{W_n}{L_n}\mu_n C_{ox}} \approx \frac{\frac{W_p}{L_p}\mu_p}{\frac{W_n}{L_n}2\mu_p} \qquad \frac{W_p}{L_p} \approx 2\frac{W_n}{L_n}$$

Since usually $L_p \approx L_n$ $\quad W_p \approx 2W_n$

- **Asymmetric case**: $k_n >> k_p$, or $\frac{W_n}{L_n} >> \frac{W_p}{L_p}$

$$V_M \approx V_{Tn}$$

NMOS turns on as soon as V_{IN} goes above V_{Tn}.

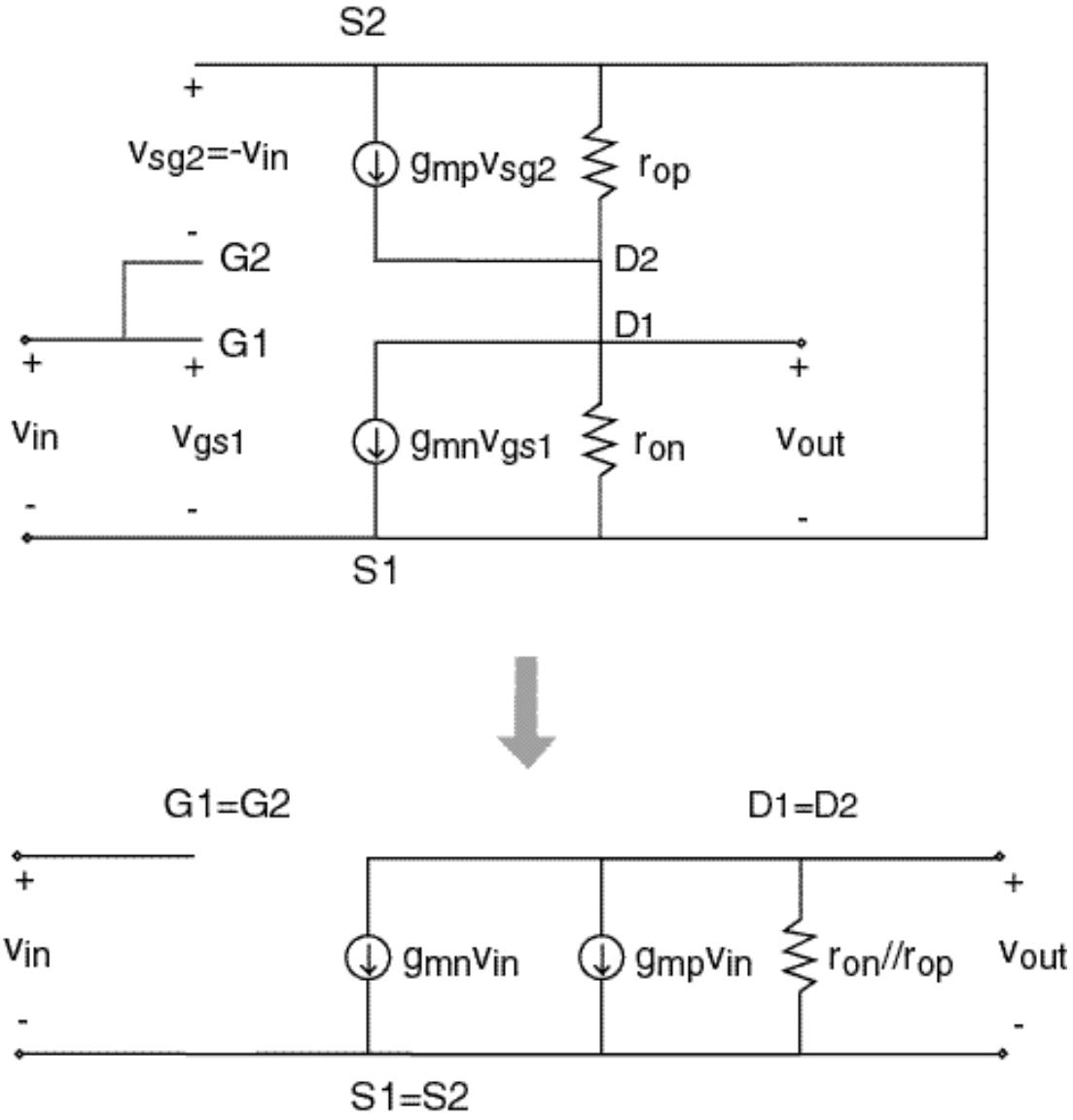
- **Asymmetric case**: $k_n << k_p$, or $\frac{W_n}{L_n} << \frac{W_p}{L_p}$

$$V_M \approx V_{DD} + V_{Tp}$$

PMOS turns on as soon as V_{IN} goes below $V_{DD} + V_{Tp}$.

CMOS inverter: noise margins (contd…)
Calculate $A_v(V_M)$

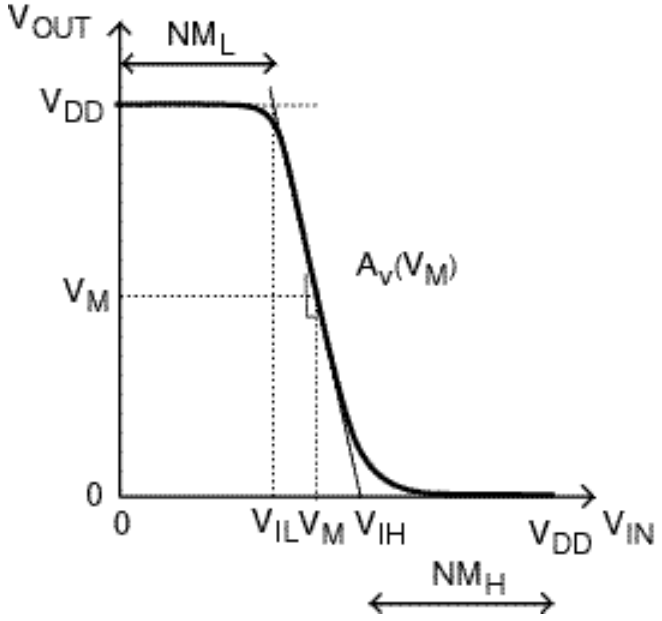
- Small signal model:



$$A_v = -(g_{mn} + g_{mp})(r_{on} // r_{op})$$

This can be rather large.

CMOS inverter: calculate noise margins (contd.)



- Noise-margin low, NM_L:

$$|A_v| = \frac{V_{DD} - V_M}{V_M - V_{IL}}$$

Then:

$$V_{IL} = V_M - \frac{V_{DD} - V_M}{|A_v|}$$

Therefore:

$$NM_L = V_{IL} - V_{OL} = V_{IL} = V_M - \frac{V_{DD} - V_M}{|A_v|}$$

In the limit of $|A_v| \rightarrow \infty$:

$$NM_L \rightarrow V_M$$

CMOS inverter: calculate noise margins (contd.)

- Noise-margin-high, NM_H:

$$|A_v| = \frac{V_M}{V_{IH} - V_M}$$

Then:

$$V_{IH} = V_M\left(1 + \frac{1}{|A_v|}\right)$$

Therefore:

$$NM_H = V_{OH} - V_{IH} = V_{DD} - V_M\left(1 + \frac{1}{|A_v|}\right)$$

In the limit of $|A_v| \rightarrow \infty$:

$$NM_H \rightarrow V_{DD} - V_M$$

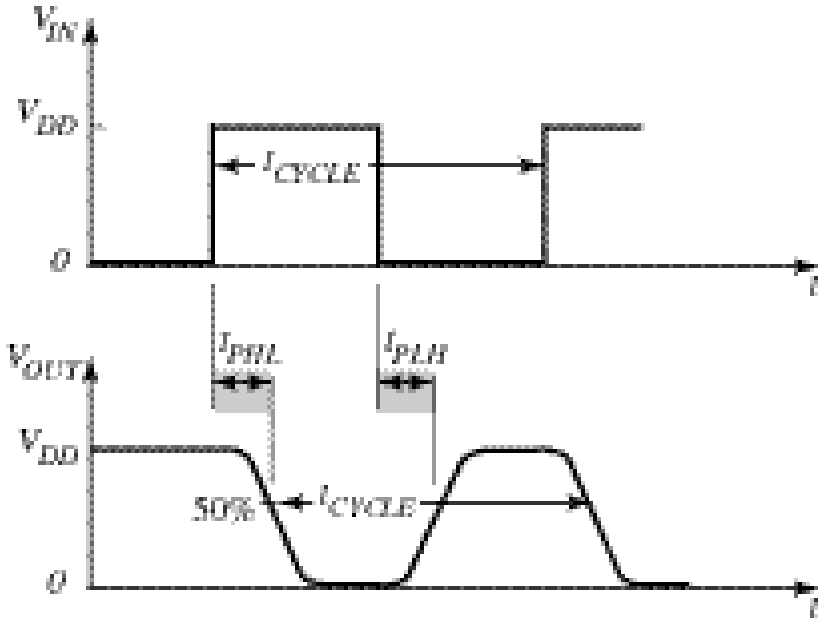
3. CMOS inverter: Propagation delay

Inverter propagation delay: time delay between input and output signals; figure of merit of logic speed.

Typical propagation delays: <1 ns.

Complex logic system has 10-50 propagation delays per clock cycle.

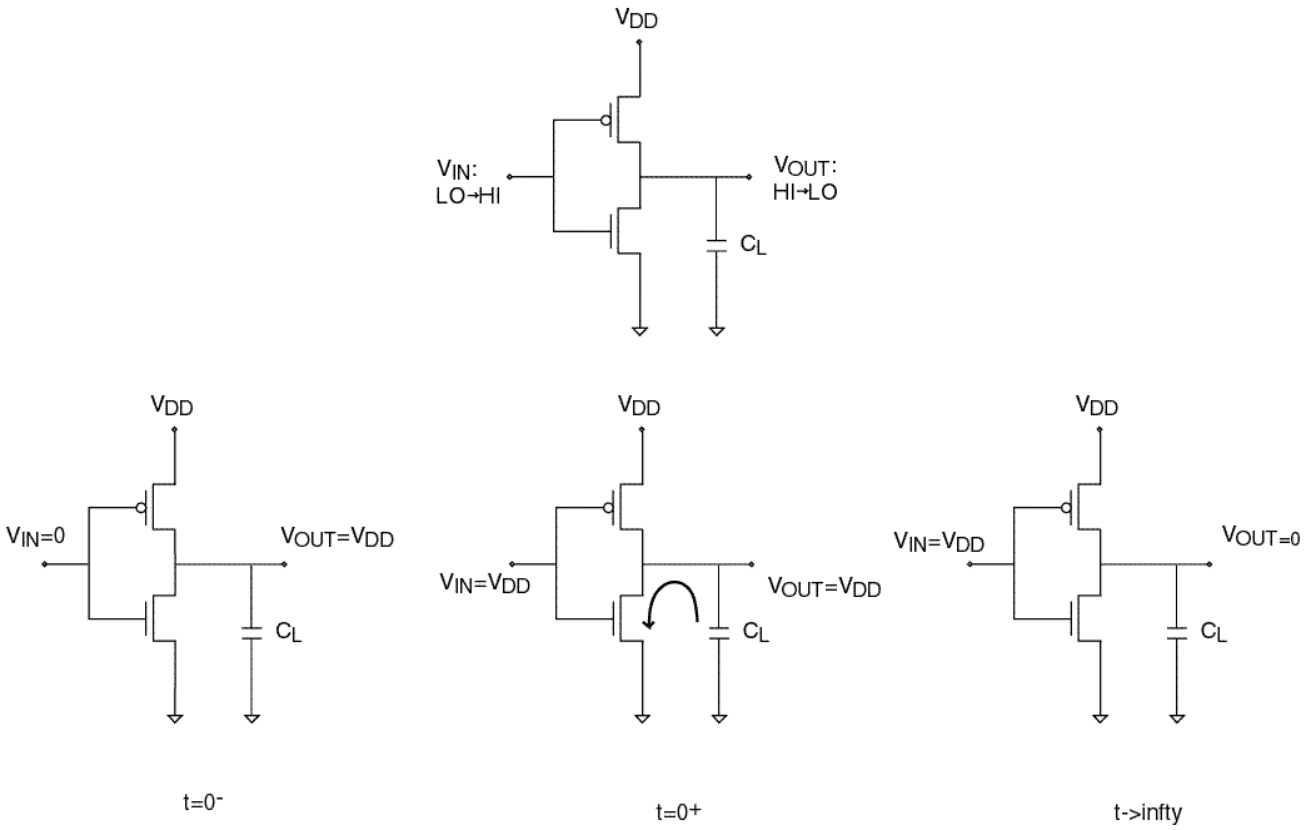
Estimation of t_p: use square-wave at input



Average propagation delay:

$$t_p = \frac{1}{2}\left(t_{PHL} + t_{PLH}\right)$$

CMOS inverter:
Propagation delay high-to-low



During early phases of discharge, NMOS is saturated and PMOS is cut-off.

Time to discharge ***half*** of charge stored in C_L:.

$$t_{pHL} \approx \frac{\frac{1}{2}\,\textbf{charge on } C_L \text{ @} t = 0^-}{\textbf{discharge current}}$$

CMOS inverter:
Propagation delay high-to-low (contd.)

Charge in C_L at $t=0^-$:

$$Q_L\left(t = 0^-\right) = C_L V_{DD}$$

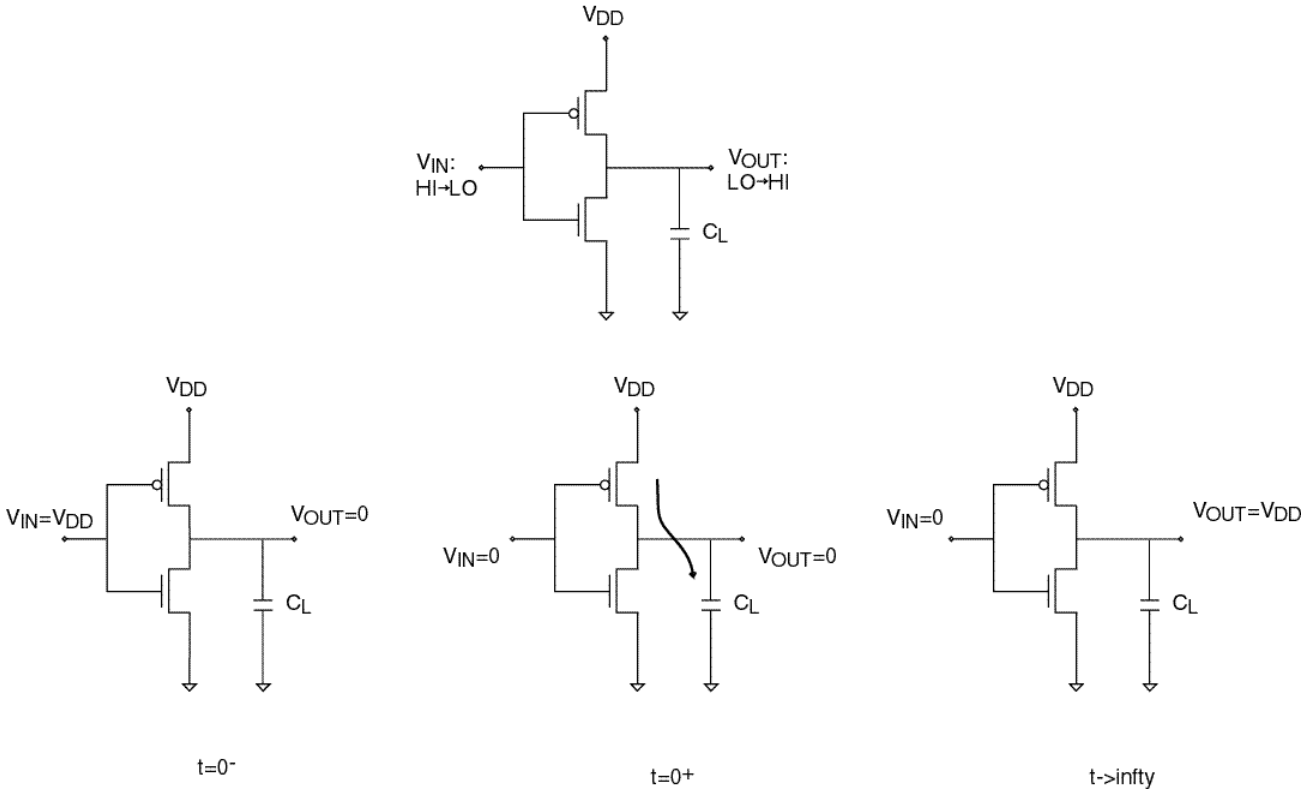
Discharge Current (NMOS in saturation):

$$I_{Dn} = \frac{W_n}{2L_n}\mu_n C_{ox}\left(V_{DD} - V_{Tn}\right)^2$$

Then:

$$t_{PHL} \approx \frac{C_L V_{DD}}{\frac{W_n}{L_n}\mu_n C_{ox}\left(V_{DD} - V_{Tn}\right)^2}$$

CMOS inverter:
Propagation delay low-to-high



During early phases of discharge, PMOS is saturated and NMOS is cut-off.

Time to charge to ***half*** of final charge on C_L:.

$$t_{PLH} \approx \frac{\frac{1}{2}\text{charge on } C_L \text{ @ } t=\infty}{\text{charge current}}$$

CMOS inverter:
Propagation delay high-to-low (contd.)

Charge in C_L at $t=\infty$:

$$Q_L(t=\infty) = C_L V_{DD}$$

Charge Current (PMOS in saturation):

$$-I_{Dp} = \frac{W_p}{2L_p}\mu_p C_{ox}\left(V_{DD} + V_{Tp}\right)^2$$

Then:

$$t_{PLH} \approx \frac{C_L V_{DD}}{\frac{W_p}{L_p}\mu_p C_{ox}\left(V_{DD} + V_{Tp}\right)^2}$$

Key dependencies of propagation delay:

- $V_{DD} \uparrow \quad t_p \downarrow$
  - Reason: $V_{DD} \uparrow \quad Q(C_L) \uparrow$, but also $I_D \uparrow$
  - Trade-off: $V_{DD} \uparrow$ more power consumed.
- $L \downarrow \quad t_p \downarrow$
  - Reason: $L \downarrow \quad I_D \uparrow$
  - Trade-off: manufacturing cost!

Components of load capacitance C_L:

- ***Following logic gates***: must add capacitance of each gate of every transistor the output is connected to.
- ***Interconnects wire*** that connects output to input of following logic gates
- ***Own drain-to-body capacitances***

$$C_L = C_G + C_{wire} + C_{DBn} + C_{DBp}$$

See details in Howe & Sodini Section 5.4.3

What did we learn today?

Summary of Key Concepts

Key features of CMOS inverter:

- No current between power supply and ground while inverter is idle in any logic state
- "rail-to-rail" logic
  - Logic levels are 0 and V_{DD}.
- High $|A_v|$ around the logic threshold
  - Good noise margins.

CMOS inverter logic threshold and noise margins engineered through W_n/L_n and W_p/L_p.

Key dependencies of propagation delay:

- $V_{DD} \uparrow \quad t_p \downarrow$
- $L \downarrow \quad t_p \downarrow$