Lecture 6

PN Junction and MOS Electrostatics(III)

Metal-Oxide-Semiconductor Structure

Outline

1. Introduction to MOS structure
2. Electrostatics of MOS in thermal equilibrium
3. Electrostatics of MOS out of thermal equilibrium

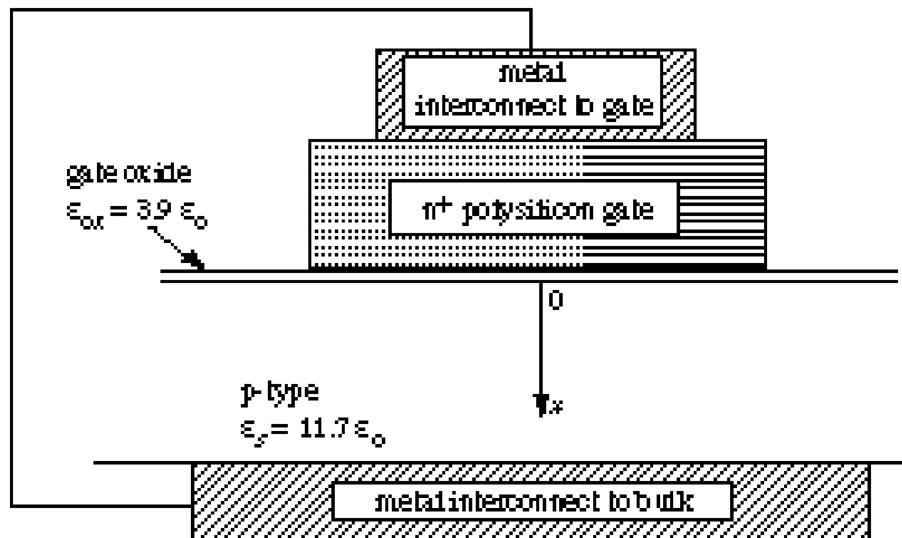
Reading Assignment:
Howe and Sodini, Chapter 3, Sections 3.7-3.8

Summary of Key Concepts

- Charge redistribution in MOS structure in thermal equilibrium
  - SCR in semiconductor
  - ***Þ built-in potential across MOS structure.***
- In most cases, we can use depletion approximation in semiconductor SCR
- Application of voltage modulates depletion region width in semiconductor
  - **No current flows**

1. Introduction

Metal-Oxide-Semiconductor structure

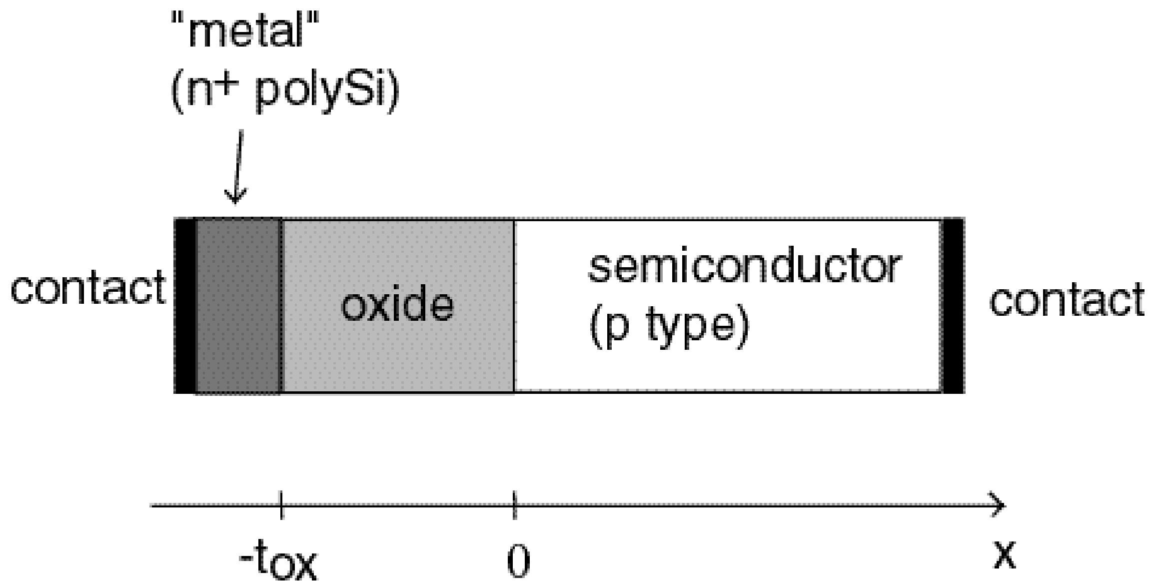


MOS at the heart of the electronics revolution:

- Digital and analog functions
  - Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is key element of Complementary Metal-Oxide-Semiconductor (CMOS) circuit family
- Memory function
  - Dynamic Random Access Memory (DRAM)
  - Static Random Access Memory (SRAM)
  - Non-Volatile Random Access Memory (NVRAM)
- Imaging
  - Charge Coupled Device (CCD) camera
- Displays
  - Active Matrix Liquid Crystal Displays (AMLCD)
- …

2. MOS Electrostatics in equilibrium

Idealized 1D structure:

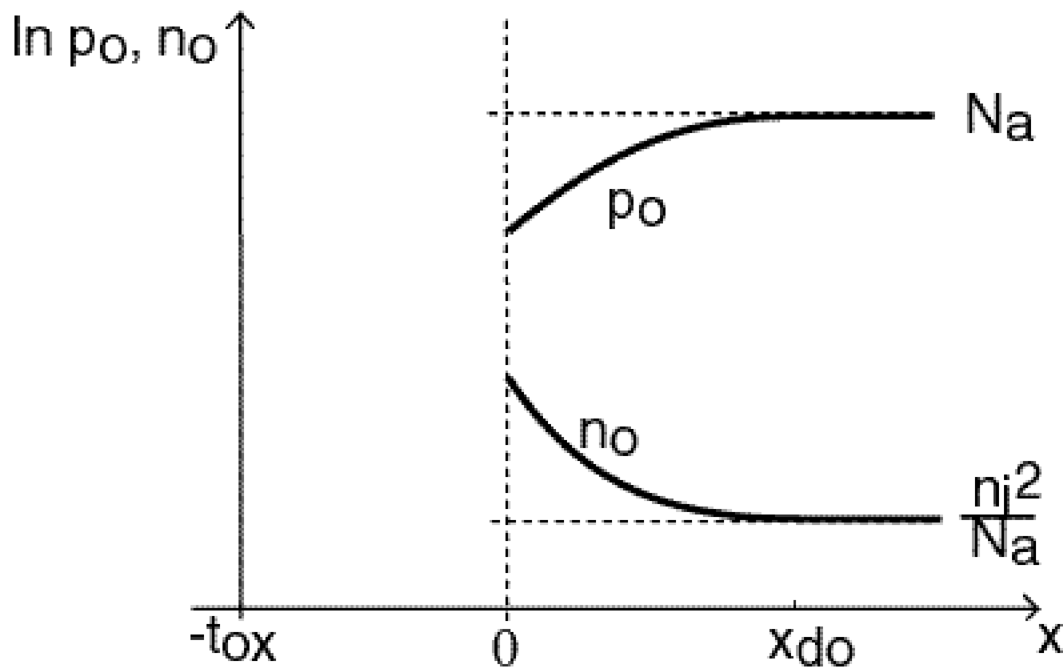


- **Metal**: does not tolerate volume charge
  - ⇒ charge can only exist at its surface
- **Oxide**: insulator and does not have volume charge
  - ⇒ no free carriers, no dopants
- **Semiconductor**: can have volume charge
  - ⇒ Space charge region (SCR)

Oxide "leaks": given enough time, thermal equilibrium can be established by charge exchange between metal and semiconductor

MOS structure: sandwich of dissimilar materials
⇒ carrier transfer ⇒ space-charge region in equilibrium
⇒ built-in potential

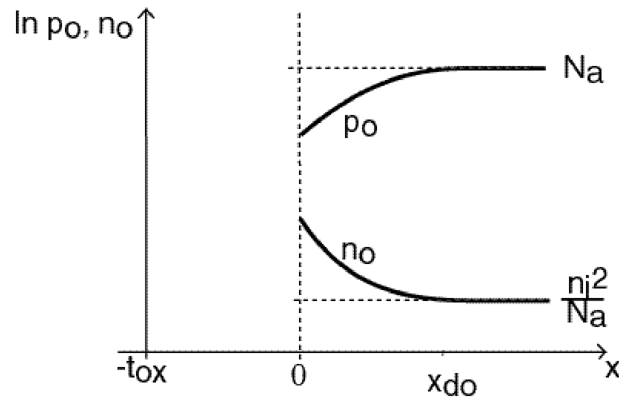
For most metals on p-Si, equilibrium achieved by electrons diffusing from metal to semiconductor and holes from semiconductor to metal:

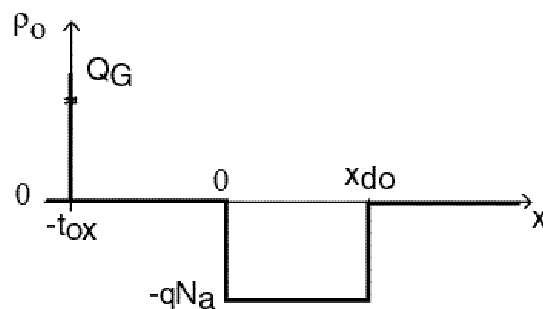


Remember: $n_o p_o = n_i^2$

Fewer holes near Si / SiO_2 interface
⇒ ionized acceptors exposed ***(volume charge)***

Space Charge Density





- In semiconductor: space-charge region close Si /SiO_2 interface
  - can do ***depletion approximation***
- In metal: sheet of charge at metal /SiO_2 interface
  - ***Space-charge region***
- Overall charge neutrality

$$\mathbf{x} = -\mathbf{t}_{\mathbf{ox}}; \qquad \sigma = \mathbf{Q}_{\mathbf{G}}$$

$$-\mathbf{t}_{\mathbf{ox}} < \mathbf{x} < 0; \qquad \rho_{\mathbf{o}}(\mathbf{x}) = 0$$

$$0 < \mathbf{x} < \mathbf{x}_{\mathbf{do}}; \qquad \rho_{\mathbf{o}}(\mathbf{x}) = -\mathbf{q}\mathbf{N}_{\mathbf{a}}$$

$$\mathbf{x}_{\mathbf{do}} < \mathbf{x}; \qquad \rho_{\mathbf{o}}(\mathbf{x}) = 0$$

Electric Field

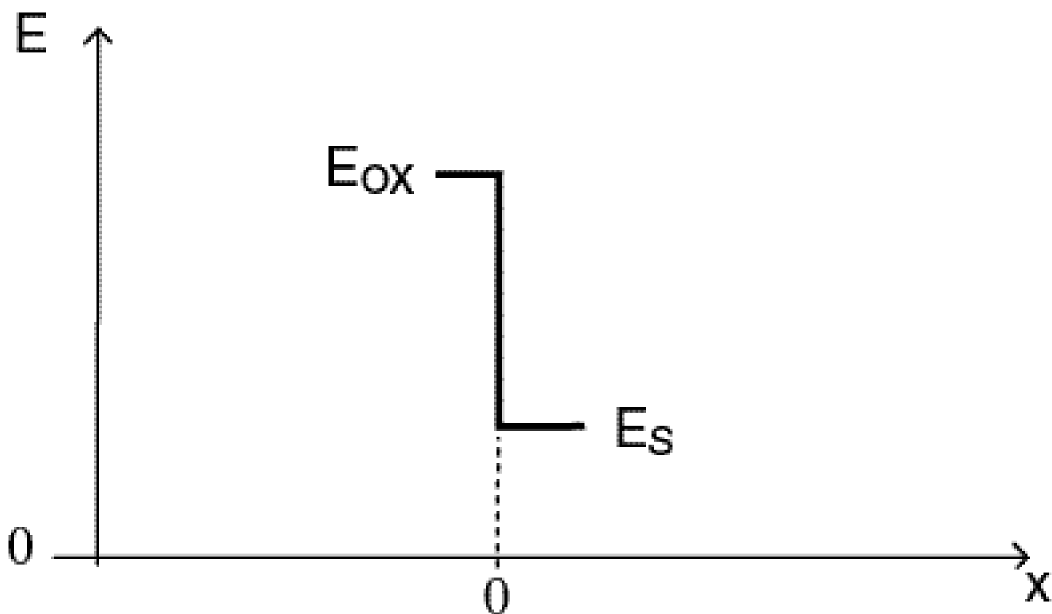
Integrate Gauss's equation

$$\mathbf{E_o}(\mathbf{x}_2) - \mathbf{E}(\mathbf{x}_1) = \frac{1}{\varepsilon}\int_{\mathbf{x}_1}^{\mathbf{x}_2} \rho(\mathbf{x})\,\mathbf{dx}'$$

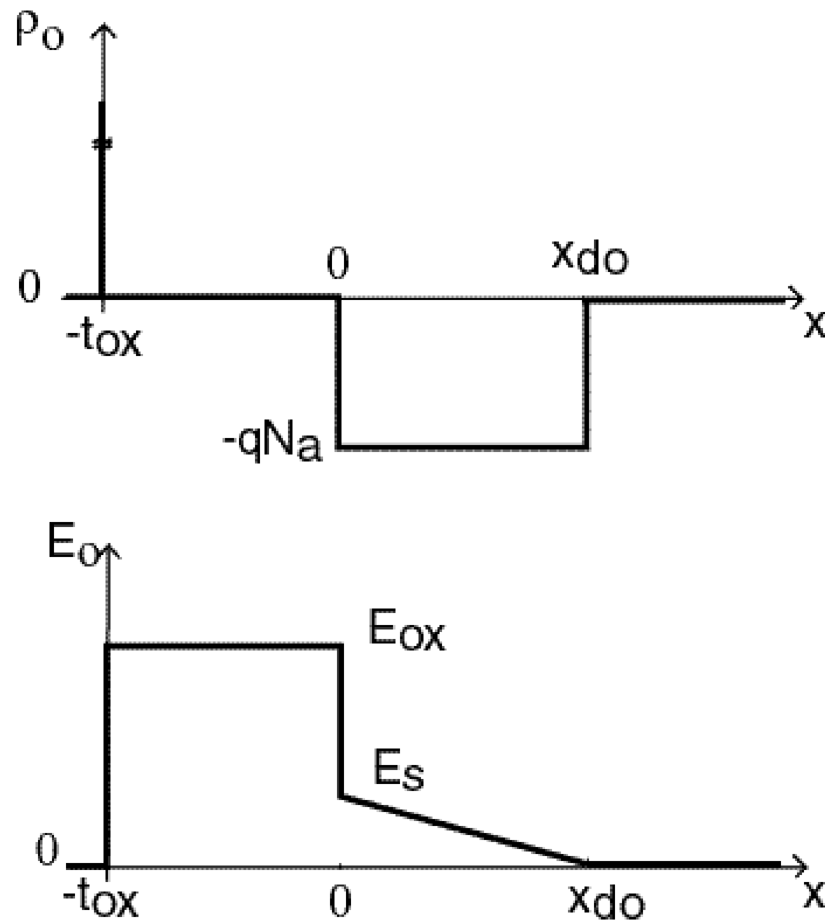
At interface between oxide and semiconductor, there is a change in **permittivity** ⇒ change in electric field

$$\varepsilon_{ox}\mathbf{E}_{ox} = \varepsilon_s\mathbf{E}_s$$

$$\frac{\mathbf{E}_{ox}}{\mathbf{E}_s} = \frac{\varepsilon_s}{\varepsilon_{ox}} \approx 3$$



Start integrating from deep inside semiconductor:



$$\mathbf{x_{do} < x;} \qquad \mathbf{E_o(x)} = 0$$

$$0 < \mathbf{x} < \mathbf{x_{do}}; \qquad \mathbf{E_o(x) - E_o(x_{do})} = \frac{1}{\boldsymbol{\varepsilon_s}} \int_{\mathbf{x_{do}}}^{\mathbf{x}} -\mathbf{qN_a\, dx'} = -\frac{\mathbf{qN_a}}{\boldsymbol{\varepsilon_s}} \left(\mathbf{x - x_{do}}\right)$$

$$-\mathbf{t_{ox}} < \mathbf{x} < 0; \qquad \mathbf{E_o(x)} = \frac{\boldsymbol{\varepsilon_s}}{\boldsymbol{\varepsilon_{ox}}} \mathbf{E_o(x} = 0^+\mathbf{)} = \frac{\mathbf{qN_a x_{do}}}{\boldsymbol{\varepsilon_{ox}}}$$

$$\mathbf{x} < -\mathbf{t_{ox}}; \qquad \mathbf{E(x)} = 0$$

Electrostatic Potential

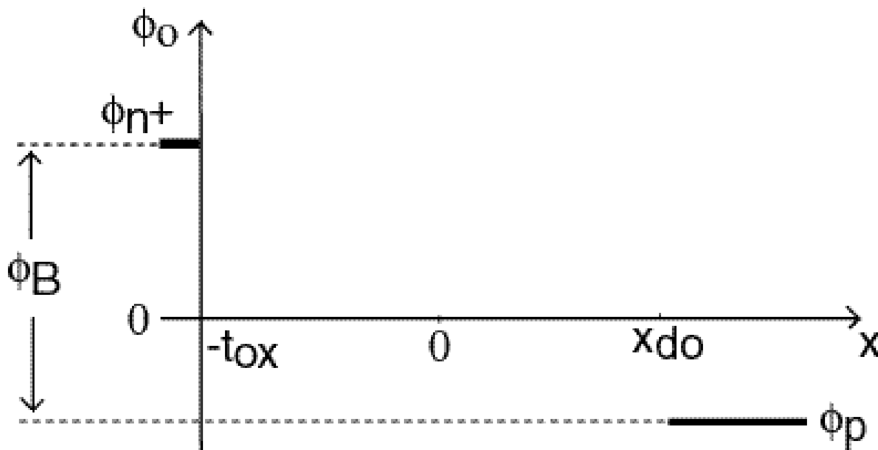
(with $\phi=0$ @ $n_o=p_o=n_i$)

$$\phi = \frac{kT}{q} \bullet \ln \frac{n_o}{n_i} \qquad \phi = -\frac{kT}{q} \bullet \ln \frac{p_o}{n_i}$$

In QNR,s, n_o and p_o are known $\Rightarrow$ can determine ϕ

in p-QNR: $p_o=N_a \Rightarrow \quad \phi_p = -\frac{kT}{q} \bullet \ln \frac{N_a}{n_i}$

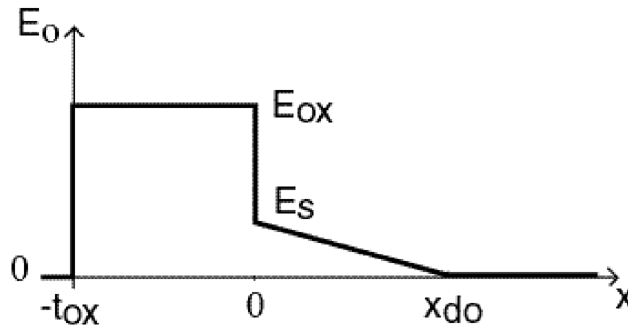
in n^+-gate: $n_o=N_d^+ \Rightarrow \quad \phi_g = \phi_{n^+}$

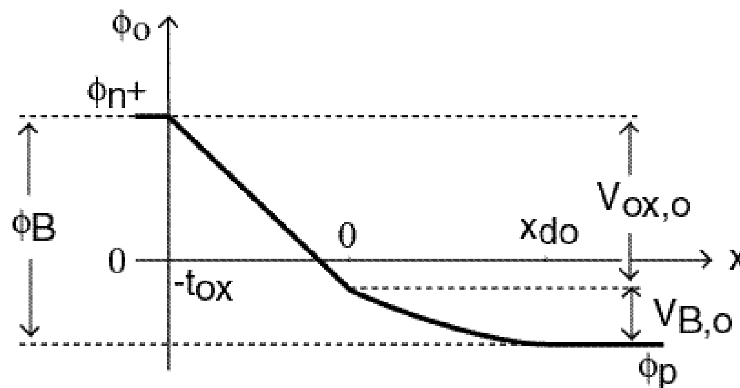


Built-in potential:

$$\phi_B = \phi_g - \phi_n = \phi_{n^+} + \frac{kT}{q} \bullet \ln \frac{N_a}{n_i}$$

To obtain $\phi_o(x)$, integrate $E_o(x)$; start from deep inside semiconductor bulk:





$\mathbf{x_{do} < x}$ $\qquad \phi_o(\mathbf{x}) = \phi_p$

$0 < \mathbf{x} < \mathbf{x_{do}}$ $\qquad \phi_o(\mathbf{x}) - \phi_o(\mathbf{x_{do}}) = -\int_{\mathbf{x_{po}}}^{\mathbf{x}} -\frac{\mathbf{qN_a}}{\varepsilon_s}\left(\mathbf{x' + x_{po}}\right)\mathbf{dx'}$

$$\phi_o(\mathbf{x}) = \phi_p + \frac{\mathbf{qN_a}}{2\varepsilon_s}\left(\mathbf{x - x_{do}}\right)^2$$

$-\mathbf{t_{ox}} < \mathbf{x} < 0$ $\qquad \phi_o(\mathbf{x}) = \phi_p + \frac{\mathbf{qN_a x_{do}^2}}{2\varepsilon_s} + \frac{\mathbf{qN_a x_{do}}}{\varepsilon_{ox}}(-\mathbf{x})$

$\mathbf{x} < -\mathbf{t_{ox}}$ $\qquad \phi_o(\mathbf{x}) = \phi_{n^+}$

Almost done ….

Still do not know x_{do} $\Rightarrow$ need one more equations

Potential difference across structure has to add up to ϕ_B:

$$\phi_B = V_{B,o} + V_{ox,o} = \frac{qN_a x_{do}^2}{2\varepsilon_s} + \frac{qN_a x_{do} t_{ox}}{\varepsilon_{ox}}$$

Solve quadratic equation:

$$x_{do} = \frac{\varepsilon_s}{\varepsilon_{ox}} t_{ox} \left[\sqrt{1 + \frac{2\varepsilon_{ox}^2 \phi_B}{\varepsilon_s q N_a t_{ox}^2}} - 1 \right] = \frac{\varepsilon_s}{C_{ox}} \left[\sqrt{1 + \frac{2C_{ox}^2 \phi_B}{\varepsilon_s q N_a}} - 1 \right]$$

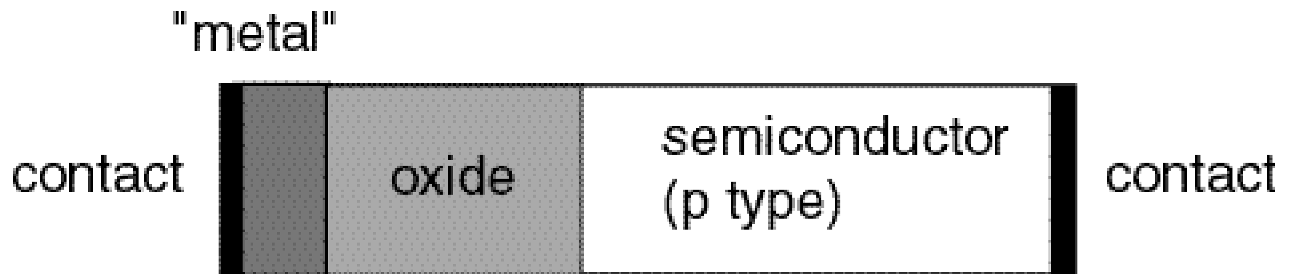
where C_{ox} is the capacitance per unit area of oxide

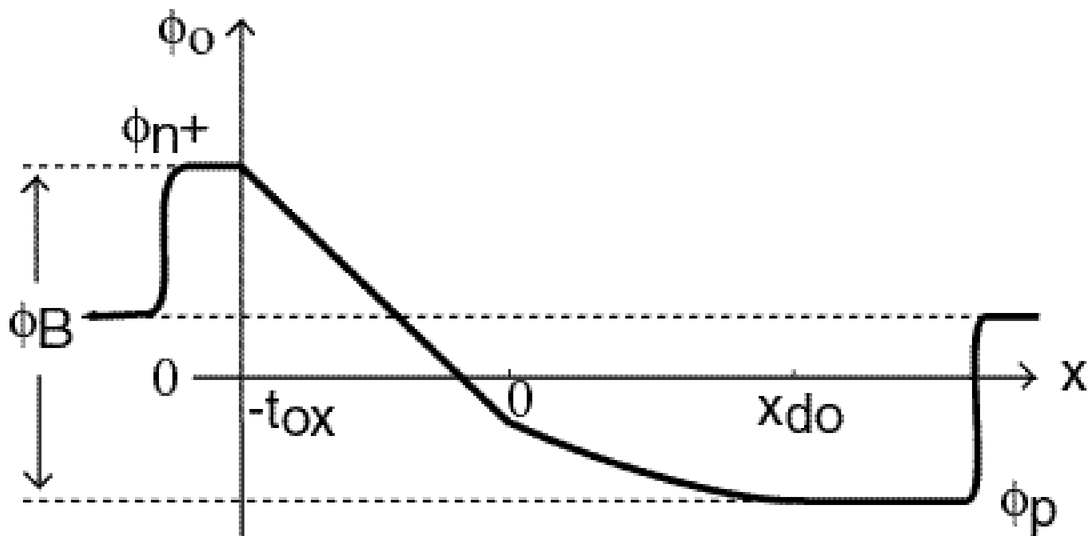
$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

Now problem is completely solved!

There are also contact potentials

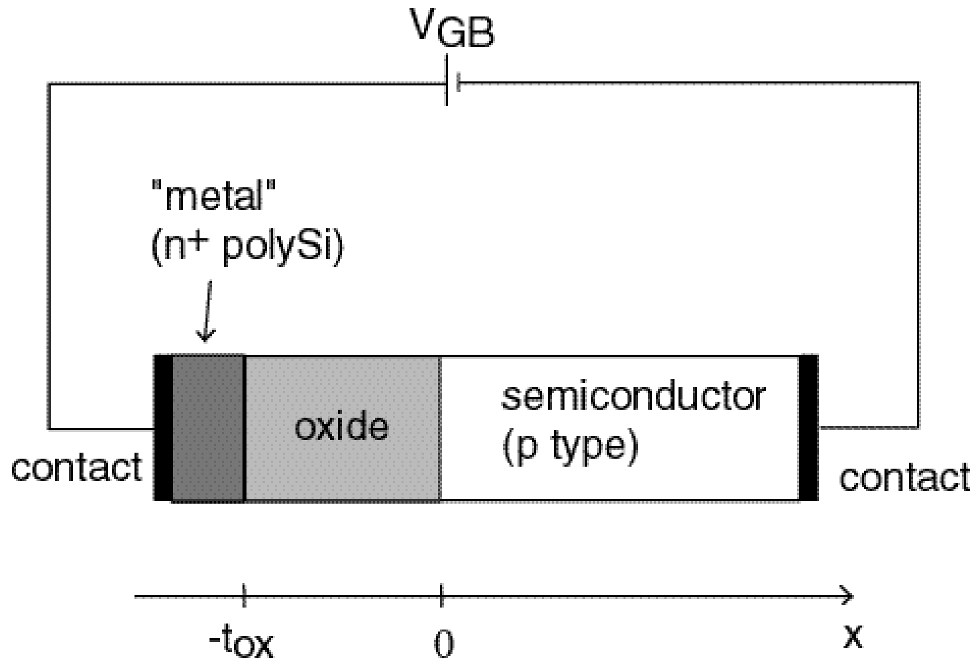
⇒total potential difference from contact to contact is zero!





3. MOS out of equilibrium

Apply voltage to gate with respect to semiconductor:



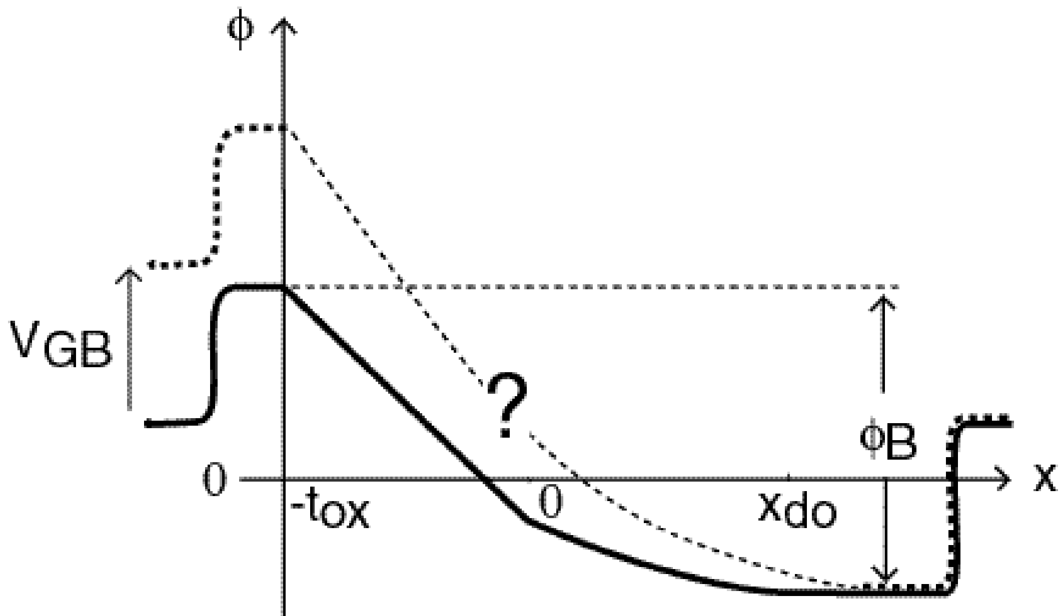
Electrostatics of MOS structure affected
$\Rightarrow$ potential difference across entire structure now $\neq 0$

How is potential difference accommodated?

Potential can drop in:

- gate contact
- n^+-polysilicon gate
- oxide
- semiconductor SCR
- semiconductor QNR
- semiconductor contact

Potential difference shows up across oxide and SCR in semiconductor

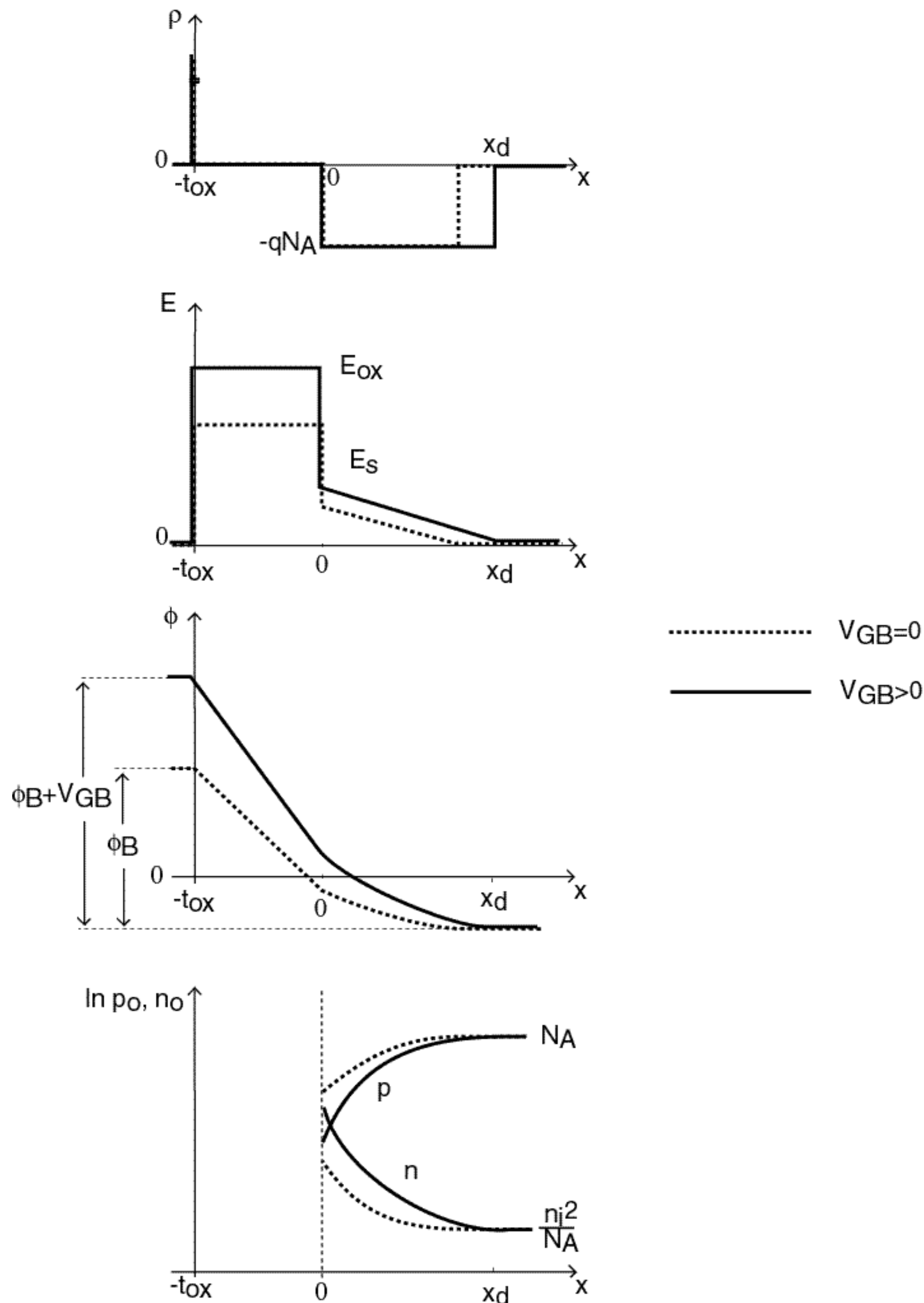


Oxide is an insulator ⇒ no current anywhere in structure

In SCR, quasi-equilibrium situation prevails
⇒ New balance between drift and diffusion

- Electrostatics qualitatively identical to thermal equilibrium (*but amount of charge redistribution is different*)
- $\mathbf{np = n_i^2}$

Apply V_{GB}>0: potential difference across structure increases
⇒ SCR expands into semiconductor substrate:



Simple way to remember:
with V_{GB}>0, gate attracts electrons and repels holes.

Qualitatively, physics unaffected by application of V_{GB} >0. Use mathematical formulation in thermal equilibrium, but:

$$\phi_B \rightarrow \phi_B + V_{GB}$$

For example:

$$x_d(V_{GB}) = \frac{\varepsilon_s}{C_{ox}}\left[\sqrt{1+\frac{2C_{ox}^2\left(\phi_B + V_{GB}\right)}{\varepsilon_s q N_a}} - 1\right]$$

$$V_{GB}\uparrow \rightarrow x_d\uparrow$$

What did we learn today?

Summary of Key Concepts

- Charge redistribution in MOS structure in thermal equilibrium
  - SCR in semiconductor
  - **⇒ built-in potential across MOS structure**.
- In most cases, we can do depletion approximation in semiconductor SCR
- Application of voltage modulates depletion region width in semiconductor
  - **No current flows**