

Lecture 9

MOSFET(II)

MOSFET I-V CHARACTERISTICS(contd.)

Outline

1. The saturation regime
2. Backgate characteristics

Reading Assignment:

Howe and Sodini, Chapter 4, Section 4.4

Announcements:

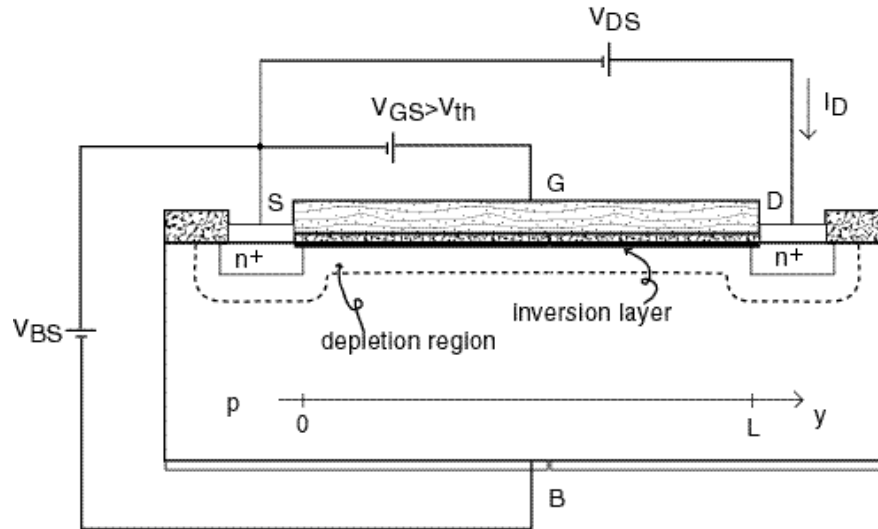
1. Quiz#1: October 11, 7:30-9:30PM, Walker Memorial; covers Lectures #1-9; open book; **must have calculator**
2. No Lecture on Tuesday: Columbus holiday
3. No Recitation on Wednesday: instructors available in their offices during recitation times
4. TA Quiz Review: Monday, October 9, 7:00 PM.
Room TBA

Summary of Key Concepts

- MOSFET in saturation ($V_{DS} \geq V_{DSsat}$): *pinch-off* point at drain-end of channel
 - Electron concentration small, but
 - Electrons move very fast;
 - Pinch-off point does not represent a barrier to electron flow
- I_{Dsat} increases slightly in saturation regime due to *channel length modulation*
- Backbias affects V_T of MOSFET

1. The Saturation Regime

Geometry of problem



Key Assumption (thus far): $V_{BS} = 0 \Rightarrow V_{GS} = V_{GB}$

Regimes of operation:

- **Cut-off:** $V_{GS} < V_T$, $V_{GD} < V_T$:
 - No inversion layer anywhere underneath the gate

$$I_D = 0$$

- **Linear:** $V_{GS} > V_T$, $V_{GD} > V_T$ and $V_{DS} > 0$:
 - allows inversion layer to electrically connect *source* and *drain*
 - Inversion layer everywhere under the gate

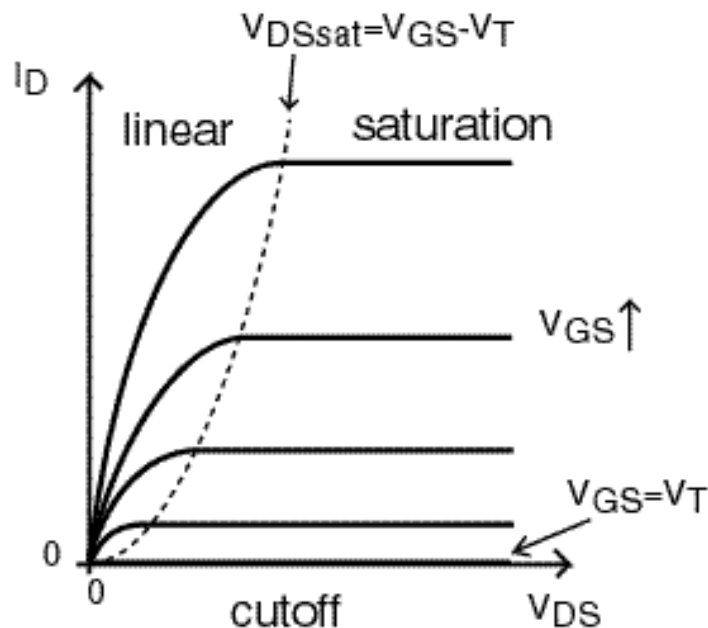
$$I_D = \frac{W}{L} \cdot \mu_n C_{ox} \left[V_{GS} - \frac{V_{DS}}{2} - V_T \right] \cdot V_{DS}$$

The Saturation Regime (contd.)

- **Saturation:** $V_{GS} > V_T$, $V_{GD} < V_T$ and $V_{DS} > 0$:
 - Inversion layer “pinched-off” at drain end of channel

$$I_D = \frac{W}{2L} \cdot \mu_n C_{ox} [V_{GS} - V_T]^2$$

Output characteristics:



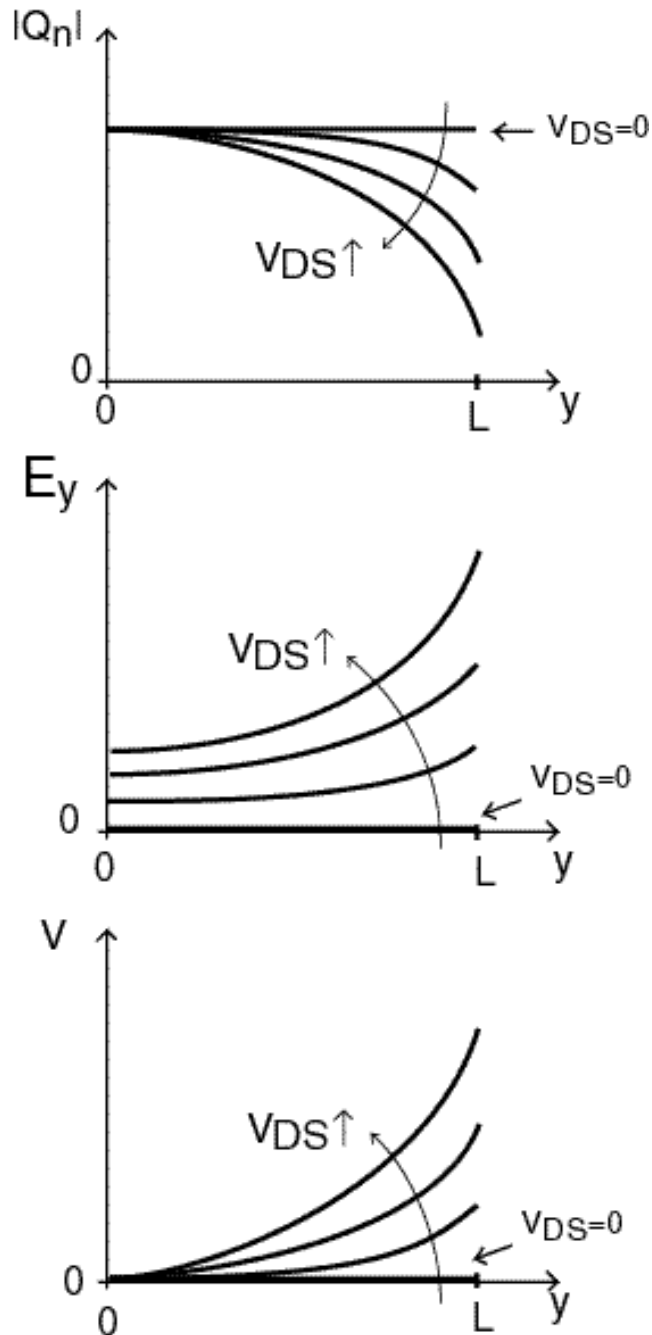
- **Last lecture:** To derive the above equations for I_D , we used for $Q_n(y)$, the charge-control relation at location y :

$$Q_n(y) = -C_{ox} [V_{GS} - V(y) - V_T]$$

for $V_{GS} - V(y) \geq V_T$. **Note that we assumed that (a) $V_{BS} = 0 \Rightarrow V_{GS} = V_{GB}$, and (b) V_T is independent of y . See discussion on body effect in Section 4.4 of text.**

The Saturation Regime (contd..)

Review of Q_n , E_y , and V in linear regime as V_{DS} increases:



Ohmic drop along channel de-biases inversion layer
 \Rightarrow **current saturation.**

The Saturation Regime (contd.)

What happens when $V_{DS} = V_{GS} - V_T$?

Charge control relation at drain:

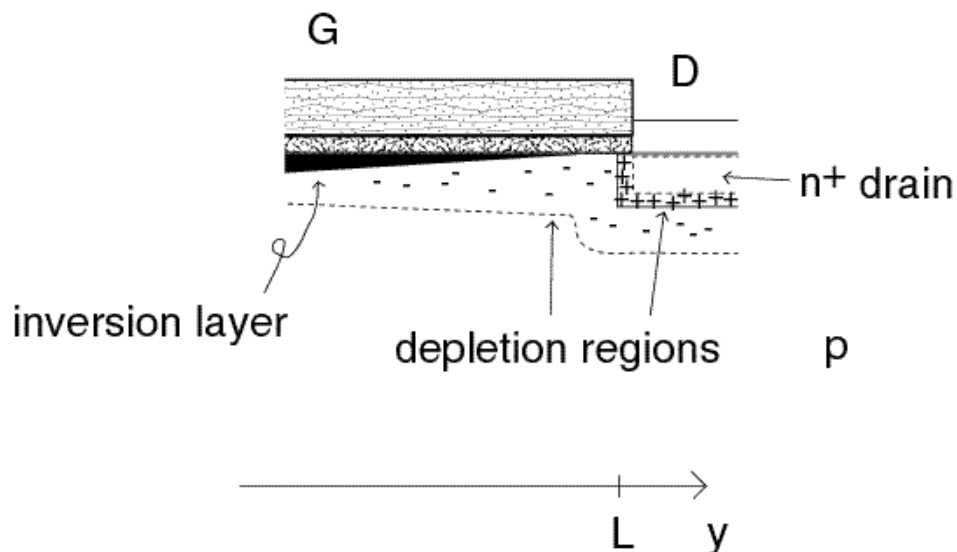
$$Q_n(L) = -C_{ox} [V_{GS} - V_{DS} - V_T] = 0$$

No inversion layer at the drain end of channel ???!!!

⇒ *Pinch-off*.

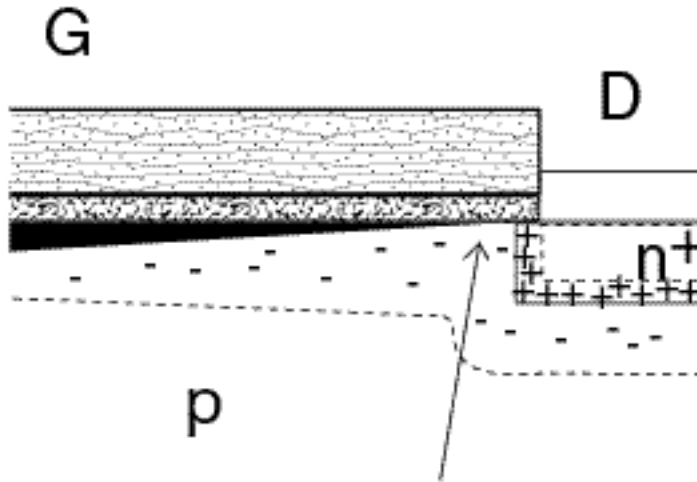
At pinch-off:

- Charge control equation inaccurate around V_T ;
- Electron concentration small but not zero;
- Electrons move fast because electric field is very high;
- Dominant electrostatic feature
 - Acceptor charge
- There is no barrier to electron flow (**on the contrary!**).



The Saturation Regime (contd...)

Voltage at pinch-off point ($V=0$ at source):



$$V(L) = V_{DSsat} = V_{GS} - V_T$$

Drain current at pinch-off:

$$\propto \text{lateral electric field} \propto V_{DSsat} = V_{GS} - V_T$$

$$\propto \text{electron concentration} \propto V_{GS} - V_T$$

$$\Rightarrow I_{DSsat} \propto [V_{GS} - V_T]^2$$

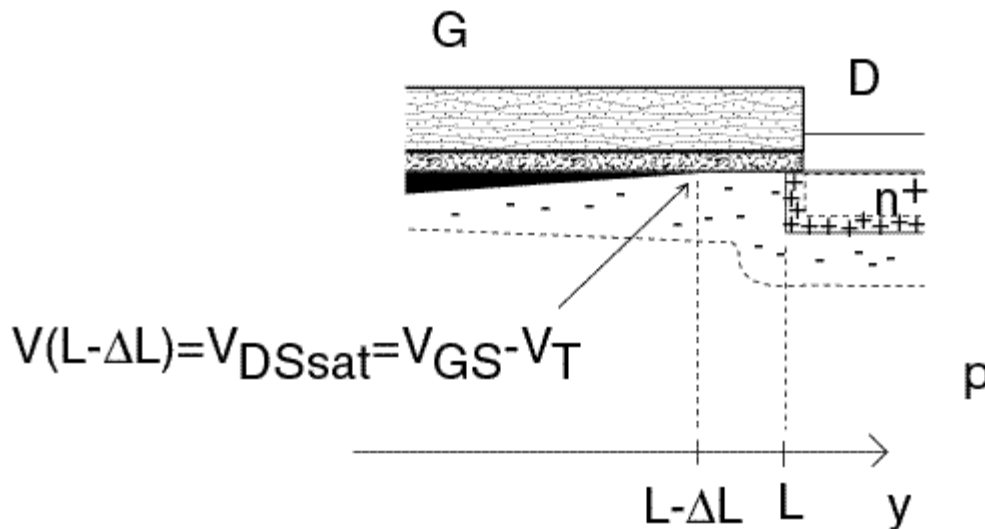
Also, $L \downarrow \Rightarrow E_y \uparrow$:

$$I_{Dsat} \propto \frac{1}{L}$$

The Saturation Regime (contd.)

What happens if $V_{DS} > V_{GS} - V_T$?

Depletion region separating pinch-off and drain widens (just like in a reverse-biased pn junction)



To first order, I_D does not increase past pinch-off:

$$I_D = I_{DSsat} \propto \frac{W}{2L} \cdot \mu_n C_{ox} \cdot [V_{GS} - V_T]^2$$

To second order, electrical channel length affected:

$L \downarrow \Rightarrow I_D \uparrow$:

$$I_D \propto \frac{1}{L - \Delta L} \approx \frac{1}{L} \left[1 + \frac{\Delta L}{L} \right]$$

The Saturation Regime (contd.)

Experimental finding:

$$\Delta I_D \propto V_{DS} - V_{DSsat}$$

Hence

$$\frac{\Delta I_D}{I_D} = \lambda [V_{DS} - V_{DSsat}]$$

with

$$\lambda \propto \frac{1}{L}$$

Typically,

$$\lambda = \frac{0.1 \mu\text{m} \cdot \text{V}^{-1}}{L}$$

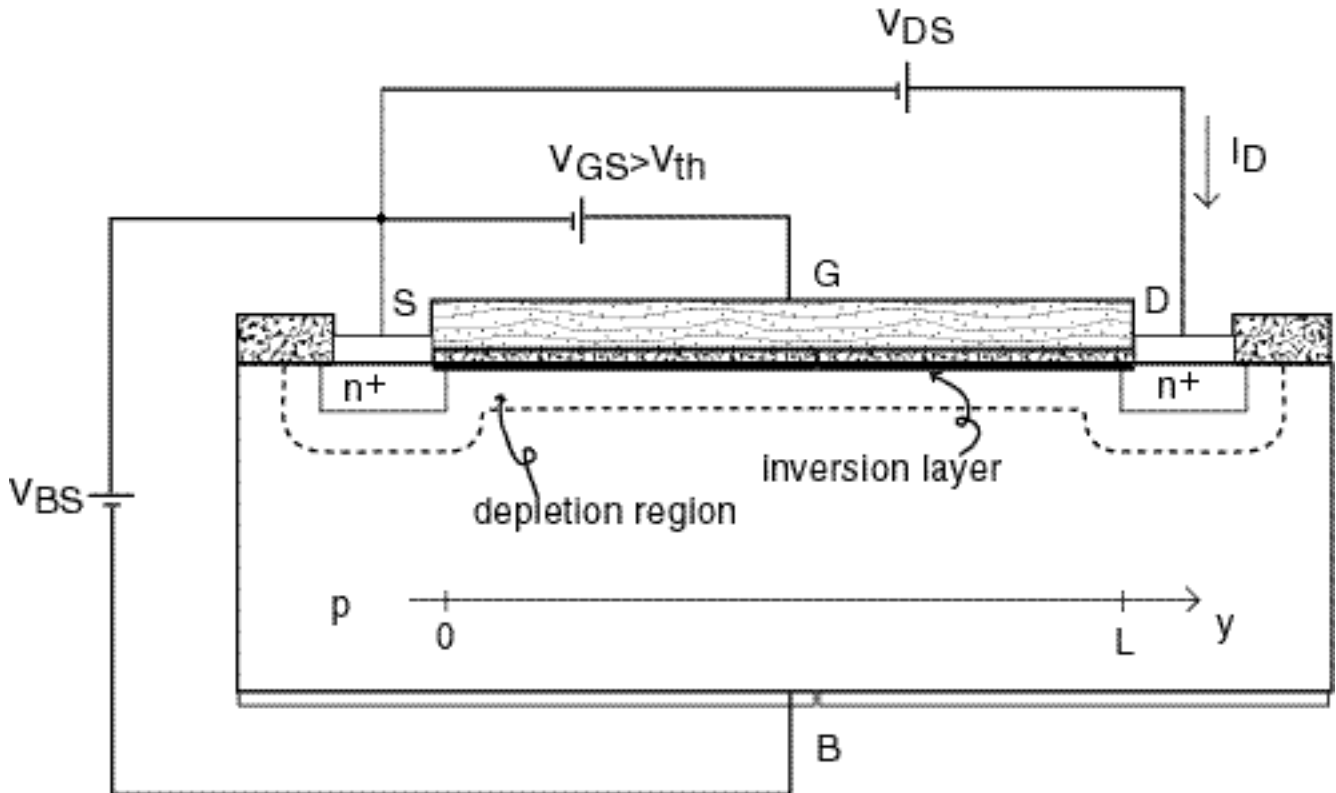
For $L = 1 \mu\text{m}$, increase of V_{DS} of 1V past V_{DSsat} results in increase in I_D of 10%.

Improved model for the drain current in saturation:

$$I_D = \frac{W}{2L} \cdot \mu_n C_{ox} (V_{GS} - V_T)^2 [1 + \lambda (V_{DS} - V_{DSsat})]$$

2. Backgate Characteristics

There is a fourth terminal in a MOSFET: the *body*.
What does it do?



Key Assumption (thus far): $V_{BS} = 0 \Rightarrow V_{GS} = V_{GB}$

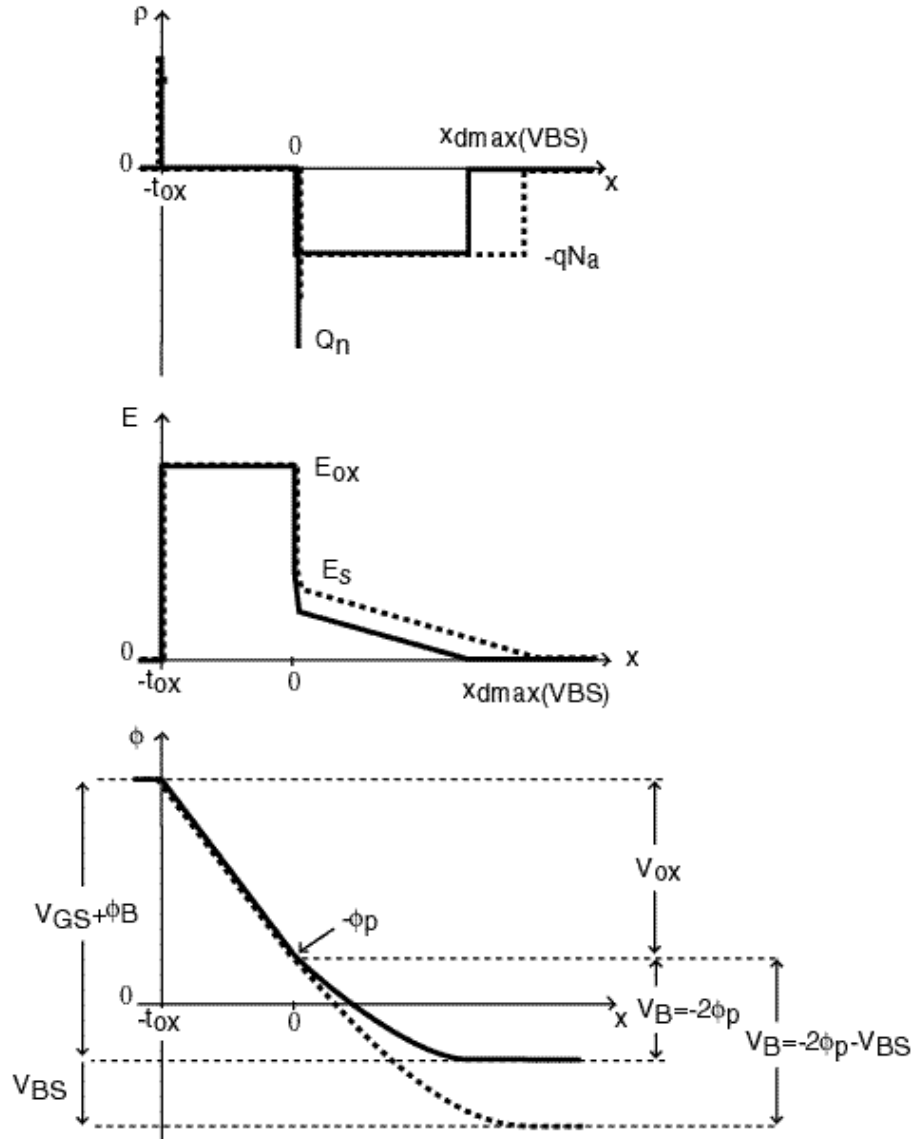
- Body contact allows application of bias to body with respect to inversion layer, V_{BS} .
- Only interested in $V_{BS} < 0$ (pn diode in reverse bias).
- Interested in effect on inversion layer
 \Rightarrow examine for $V_{GS} > V_T$ (keep it constant).

Backgate Characteristics (Contd.)

Application of $V_{BS} < 0$ increases potential build-up across semiconductor:

$$-2\phi_p \Rightarrow -2\phi_p - V_{BS}$$

Depletion region must widen to produce required extra field:



Backgate Characteristics (Contd.)

Consequences of application of $V_{BS} < 0$:

- $-2\phi_p \Rightarrow -2\phi_p - V_{BS}$
- $|Q_B| \uparrow \Rightarrow x_{dmax} \uparrow$
- Since V_{GS} is constant, V_{ox} unchanged
 - $\Rightarrow E_{ox}$ unchanged
 - $\Rightarrow |Q_S| = |Q_G|$ unchanged
- $|Q_S| = |Q_n| + |Q_B|$ unchanged, but $|Q_B| \uparrow \Rightarrow |Q_n| \downarrow$
 - \Rightarrow inversion layer charge is reduced!

For the same applied gate-to-source voltage V_{GS} , application of $V_{BS} < 0$ reduces the density of electrons in the inversion layer, in other words $V_T \uparrow$

Backgate Characteristics (Contd.)

How does V_T change with V_{BS} ?

In V_T formula change $-2\phi_p$ to $-2\phi_p - V_{BS}$:

$$V_T^{GB}(V_{BS}) = V_{FB} - 2\phi_p - V_{BS} + \frac{1}{C_{ox}} \sqrt{2\epsilon_s q N_a (-2\phi_p - V_{BS})}$$

In MOSFETs, interested in V_T between **gate** and source:

$$V_{GB} = V_{GS} - V_{BS} \Rightarrow V_T^{GB} = V_T^{GS} - V_{BS}$$

Then:

$$V_T^{GS} = V_T^{GB} + V_{BS}$$

And:

$$V_T^{GS}(V_{BS}) = V_{FB} - 2\phi_p + \frac{1}{C_{ox}} \sqrt{2\epsilon_s q N_a (-2\phi_p - V_{BS})} \equiv V_T(V_{BS})$$

In the context of the MOSFET, V_T is always defined in terms of **gate-to-source voltage**.

Backgate Characteristics (Contd.)

$$V_T(V_{BS}) = V_{FB} - 2\phi_p + \frac{1}{C_{ox}} \sqrt{2\epsilon_s q N_a (-2\phi_p - V_{BS})}$$

Define *backgate effect parameter* [units: $V^{-1/2}$]:

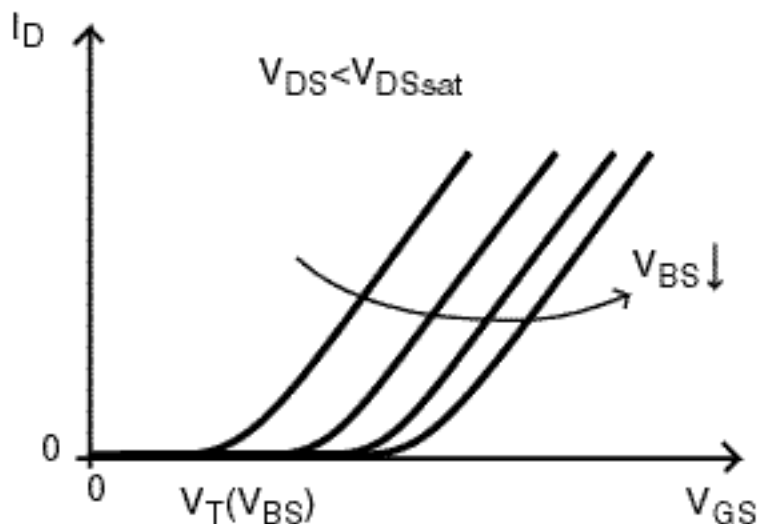
$$\gamma = \frac{1}{C_{ox}} \sqrt{2\epsilon_s q N_a}$$

And:

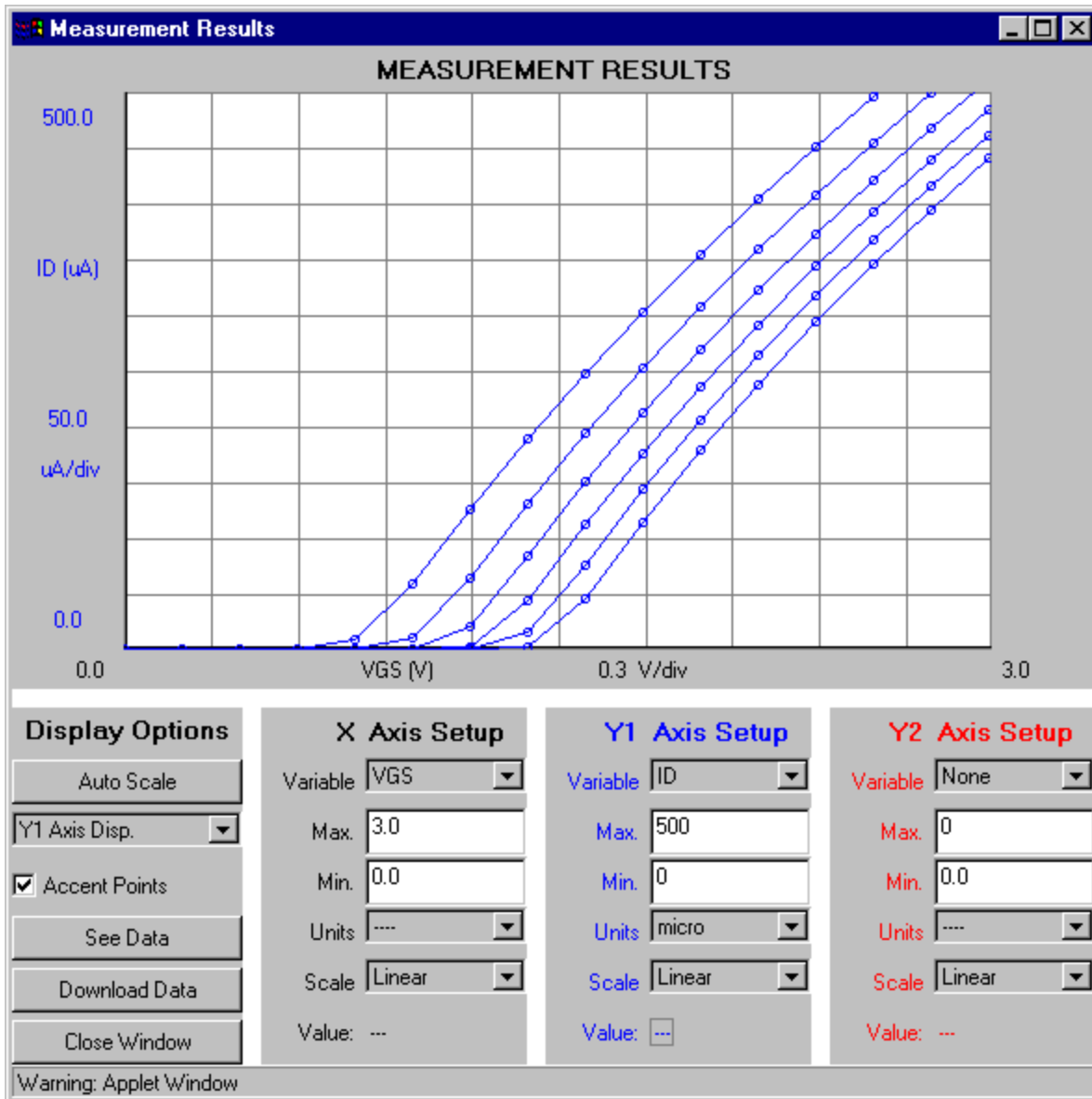
$$V_{T0} = V_T(V_{BS} = 0)$$

Then:

$$V_T(V_{BS}) = V_{T0} + \gamma \left[\sqrt{-2\phi_p - V_{BS}} - \sqrt{-2\phi_p} \right]$$



Backgate Characteristics (Contd.)



What did we learn today?

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