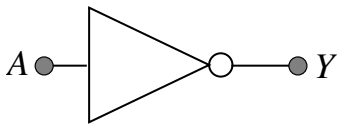
I. Digital Integrated Circuits - Logic Concepts

A. Logic Fundamentals:

- **binary** mathematics: only operate on **0** and **1** (Boolean algebra)
- simplest function -- inversion

$$B = \bar{A}$$

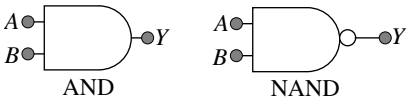
- symbol for the inverter



INPUT A	OUTPUT Y
0	1
1	0

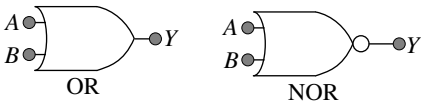
B. Other Logic Functions

- AND and NAND = “not AND”
- OR and NOR = “not OR”
- XOR



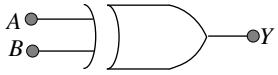
INPUT		OUTPUT *Y*	
A	*B*	AND	NAND
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

(a)



INPUT		OUTPUT *Y*	
A	*B*	OR	NOR
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

(b)



INPUT		OUTPUT *Y*
A	*B*	XOR
0	0	0
0	1	1
1	0	1
1	1	0

(c)

- One gate can have many inputs

$$C = \overline{ABC\ldots XYZ}$$

- Practical limitations ... set by need to maintain both adequate switching speed and valid logic levels
- *fan-in* -- maximum number logic gates connected to the input
- *fan-out* -- maximum number of logic gates connected to the output

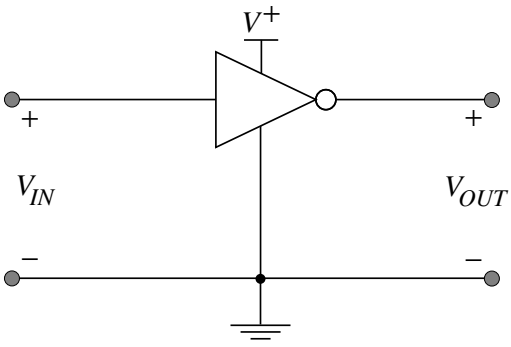
C. An Ideal Inverter

- Let the logical variable be represented by a voltage.
- Let the "**1**" correspond to a high voltage (say, 5 V) and the "**0**" correspond to the low voltage (say, 0 V).
- Voltage transfer curve for an inverter yields 0 V when a high voltage is input and the high voltage, V^+, when a low voltage is input.

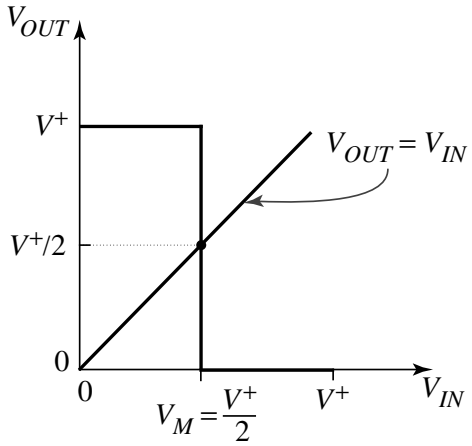
$$V_{IN} > V_M = V^+/2 \text{ --> } V_{OUT} = 0$$

$$V_{IN} < V_M = V^+/2 \text{ --> } V_{OUT} = V^+$$

- The ideal inverter returns correct logical outputs (0 V or V^+) even when the input voltage is corrupted by noise, voltage spikes, etc. which are nearly half the supply voltage!



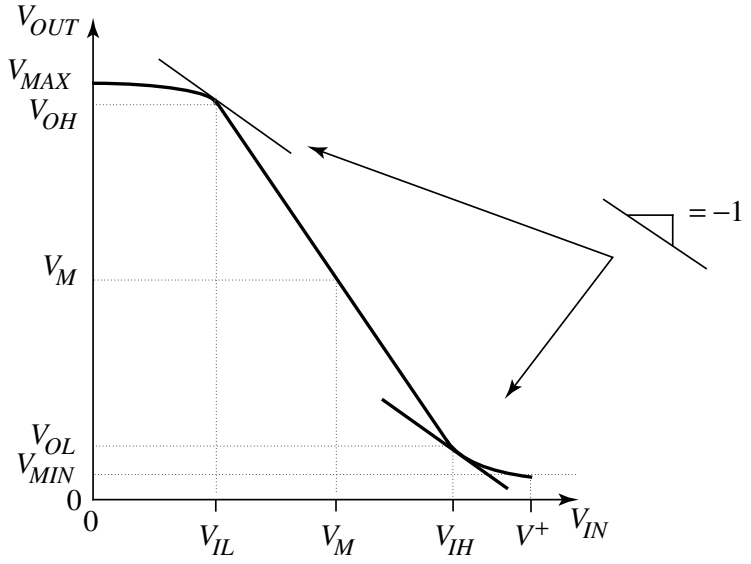
(a)



(b)

D. Real Inverters

- Inverters which we can build are approximations to the ideal inverter. A typical inverter characteristic is:



On the output and input axes, several voltages are defined:

V_M = input voltage for which $V_{OUT} = V_{IN}$

V_{OL} = "voltage output low" = max. output voltage for a valid "0"

V_{OH} = "voltage output high" = min. output voltage for a valid "1"

V_{IL} = "voltage input low" = smaller input voltage where slope equals -1

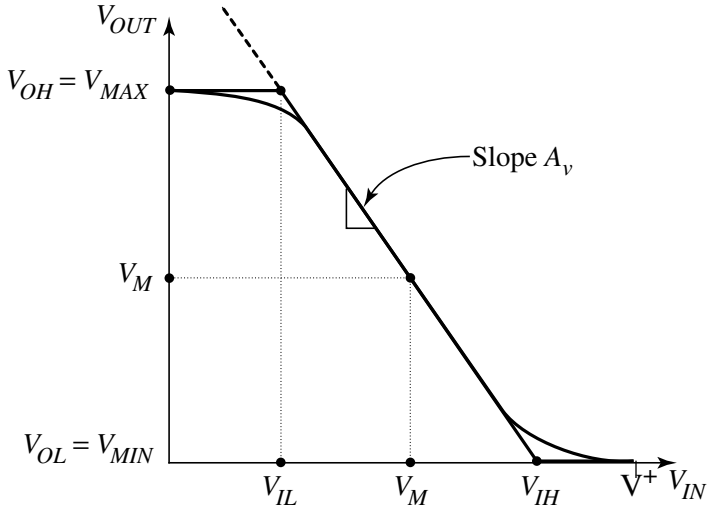
V_{IH} = "voltage input high" = larger input voltage where slope equals -1

$V_{MAX} = V_{OUT}$ for $V_{IN} = 0$ V; usually, $V_{MAX} = V^+$, the supply voltage

$V_{MIN} = V_{OUT}$ for $V_{IN} = V^+$ and is the minimum output voltage

E. Inverter Transfer Function - Hand Calculations

- Problem: evaluating where slope = -1 is an algebraic mess.
- Adopt more convenient definitions of V_M, V_{IL},V_{IH} (new in H&S)



- Use small-signal model to evaluate tangent to transfer curve

$V_{OL} = V_{MIN}$ and $V_{OH} = V_{MAX}$

V_M = Input voltage V_{IN} at which $V_{OUT} = V_{IN}$

V_{IL} = intersection of tangent to V_{OUT} (V_{IN}) curve at V_M and the line $V_{OUT} = V_{MAX}$ (= V^+, typically)

V_{IH} = intersetion of tangent to V_{OUT}(V_{IN}) curve at V_M and the line $V_{OUT} = V_{MIN}$ (= 0 V, typically)

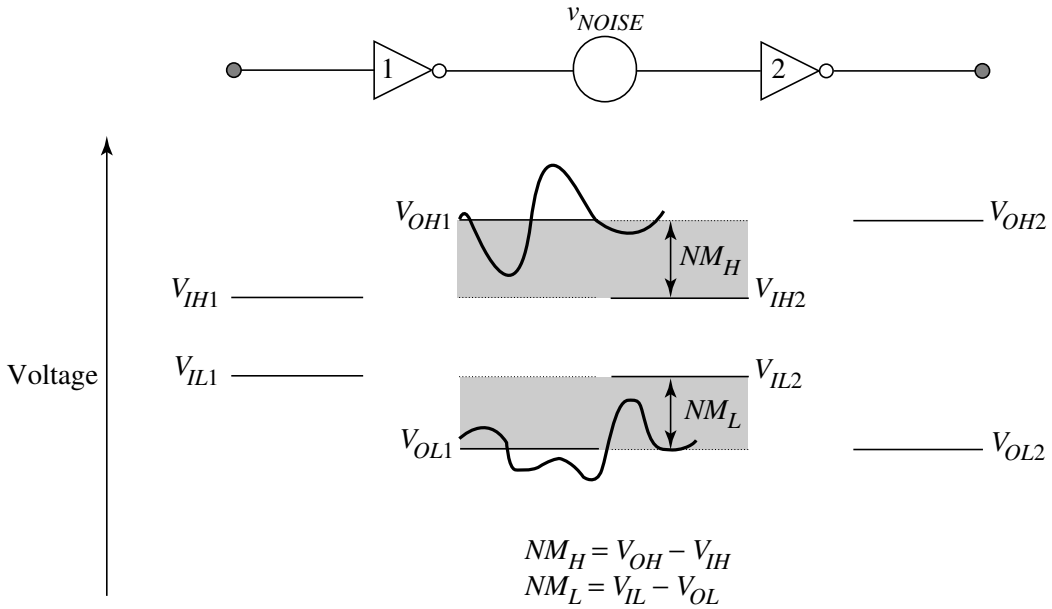
- If $V_{IN} < V_{IL}$, then V_{OUT} is considered a valid "**1**"
- If $V_{IN} > V_{IH}$, then V_{OUT} is considered a valid "**0**"

F. Noise Margins

- Cascade of two logic inverters-- output of #1 is input to #2
- Output of inverter #1 is at least, V_{OH1}
- Margin of V_{OH1} - V_{IH2} to spare before the input to inverter #2 has an invalid high input.

$NM_H = V_{OH} - V_{IH}$ = noise margin (high)

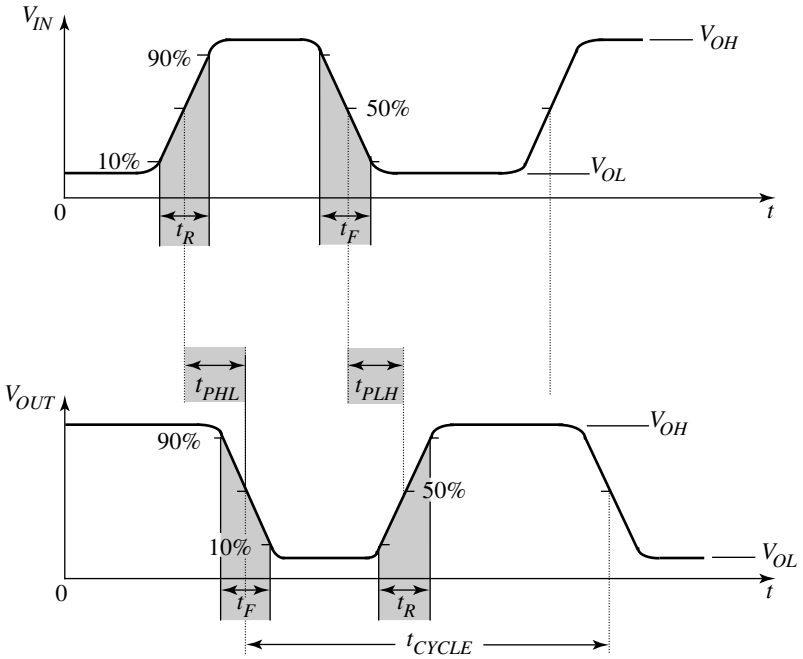
$NM_L = V_{IL} - V_{OL}$ = noise margin (low)



$NM_H = V_{OH} - V_{IH}$
$NM_L = V_{IL} - V_{OL}$

G. Propagation Delay

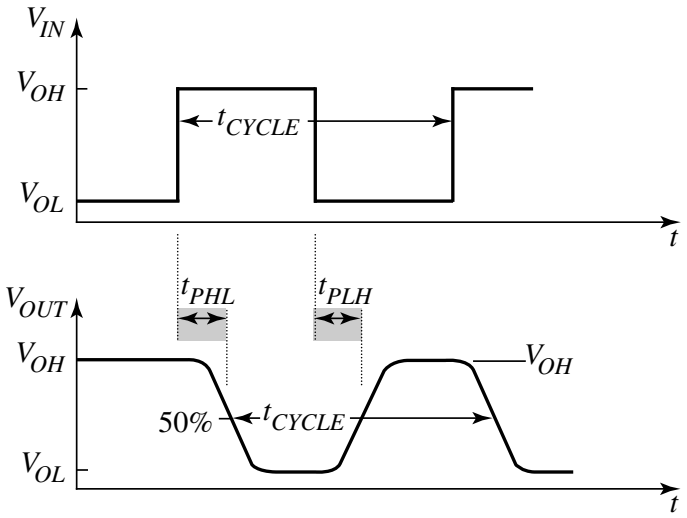
- Time is required for an inverter to change states from "**0**" to "**1**" and vice versa
- Charging and discharging MOSFET and parasitic capacitance



- Definitions:t_R = risetime; t_F = falltime -- both 10% to 90% of total swing
- t_{PHL} = delay between 50% points on the input and output waveforms during the output high-to-low transition
- t_{PLH} = delay between 50% points on the input and output waveforms during the output low-to-high transition

H. Propagation Delay - Hand Calculations

- For hand calculations, make the input waveform ideal
- Find delay in the output waveform before it reaches the 50% point.



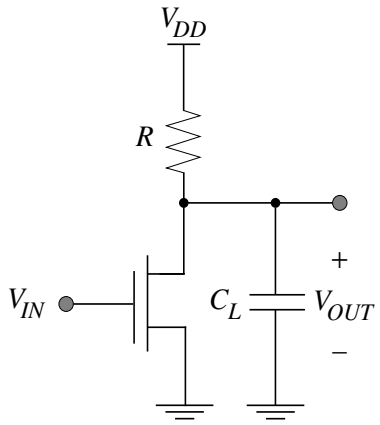
- Transient analysis can only be roughly approximated in hand calculations
- SPICE is essential for accurate analysis.

II. Inverter Circuits: NMOS-Resistor Load

A. MOSFET is an excellent switch:

- open-circuit at control terminal (gate)
- drain-source connection is open for $V_{GS} < V_{Tn}$ (cutoff region)
- drain-source connection is a resistor for $V_{GS} > V_{Tn}$ (triode region)

B. Qualitative Circuit Operation



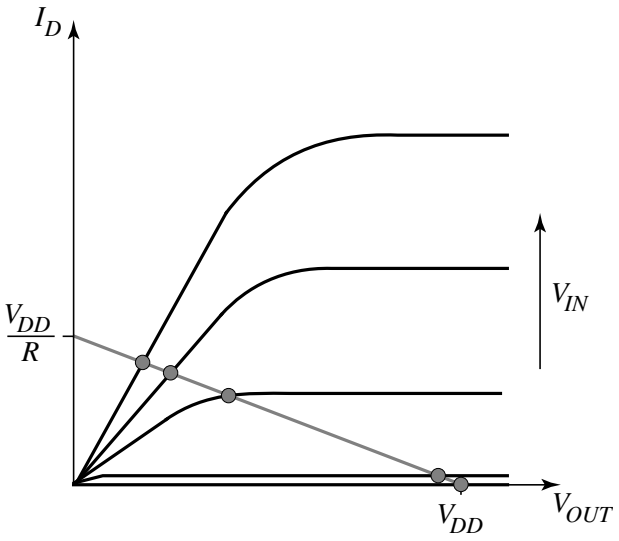
- $V^+ = V_{DD} = 5$ V (typically)
- C_L = load capacitance (from interconnections and from other inverters connected to the output
- $V_{BS} = 0$ V -- bulk-to-source short circuit is typically not shown
- $V_{IN} < V_{Tn}$ MOSFET-**OFF** ---$V_{OUT} = V_{DD}$
- $V_{IN} >> V_{Tn}$ MOSFET - **ON** --- V_{OUT} is small (value is set by resistive divider)

C. Quantitative Calculation of Transfer Characteristic

- Key concept: the static output current is zero
- MOSFET drain current = $I_D = I_R$ = current through resistor

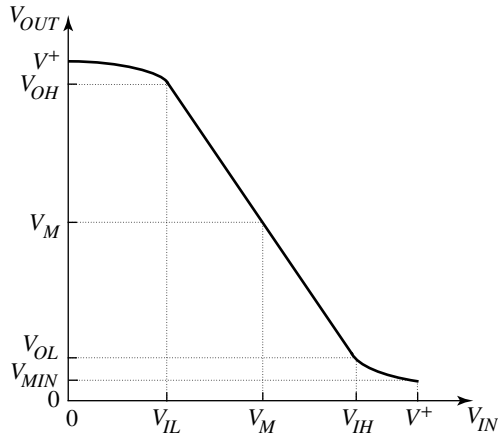
$$I_D = I_R = \frac{V_{DD} - V_{OUT}}{R} = \frac{V_{DD}}{R} - \left[\frac{1}{R}\right] V_{OUT}$$

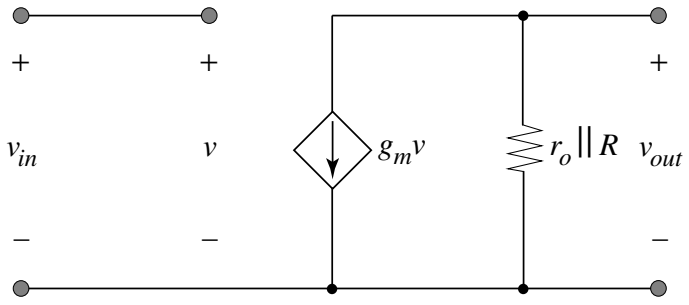
- Plotting these equations on the drain characteristics of the MOSFET since $V_{DS} = V_{OUT}$:



- The transfer characteristic can be found by plotting the intersections between the I_D (V_{IN}, V_{OUT}) characteristics with the "load line" $I_R(V_{OUT})$

D. Transfer Characteristic



E. Small Signal Model

- Use small signal model to calculate the gain v_{out}/v_{in} at V_M
- Gain is the slope of the inverter transfer characteristic at V_M
- Gain $= v_{out}/v_{in} = -g_m(r_O \parallel R) \cong -g_m R$