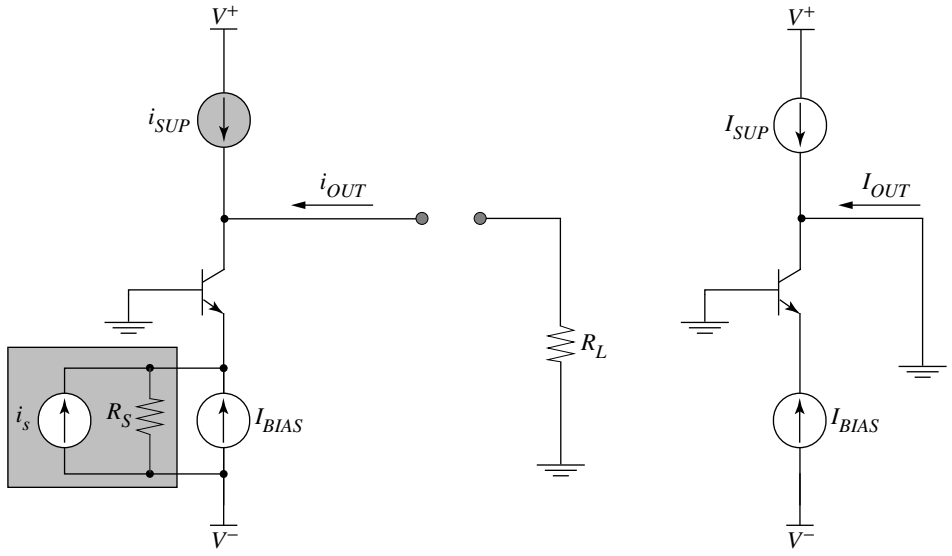
I. Common Base / Common Gate Amplifiers - Current Buffer

A. Introduction

- A current buffer takes the input current which may have a relatively small Norton resistance and replicates it at the output port, which has a high output resistance
- Input signal is applied to the emitter, output is taken from the collector
- Current gain is about unity
- Input resistance is low
- Output resistance is high.



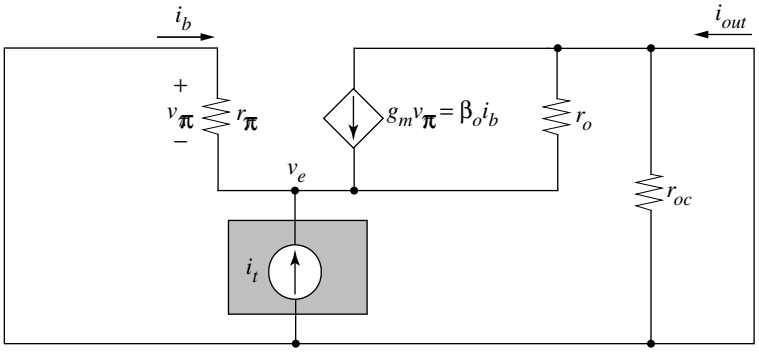
B. Biasing

- $I_{BIAS} = I_{SUP}/\alpha \approx I_{SUP}$

II. Small Signal Two Port Parameters

A. Common Base Current Gain A_i

- Small-signal circuit; apply test current and measure the short circuit output current



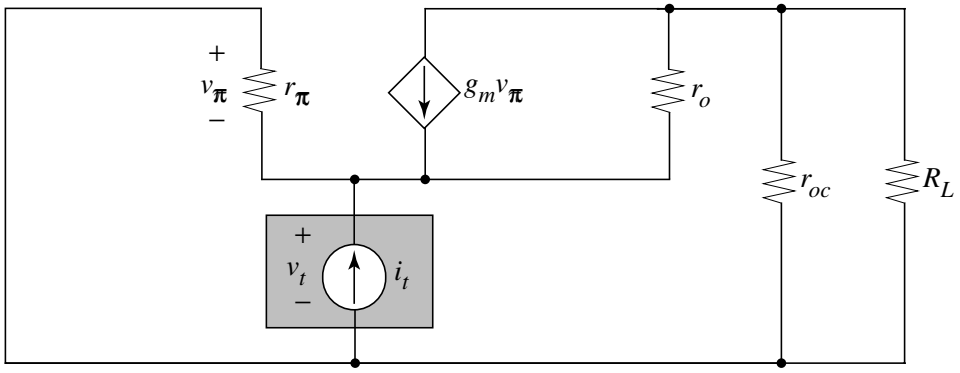
- Analysis -- see Chapter 8, pp. 507-509.
- Result:

$$A_i = \frac{-\beta_o}{1+\beta_o} \cong -1$$

- Intuition: $i_{out} = i_c = (- i_e - i_b) = -i_t - i_b$ and i_b is small

B. Common Base Input Resistance R_i

- Apply test current, with load resistor R_L present at the output



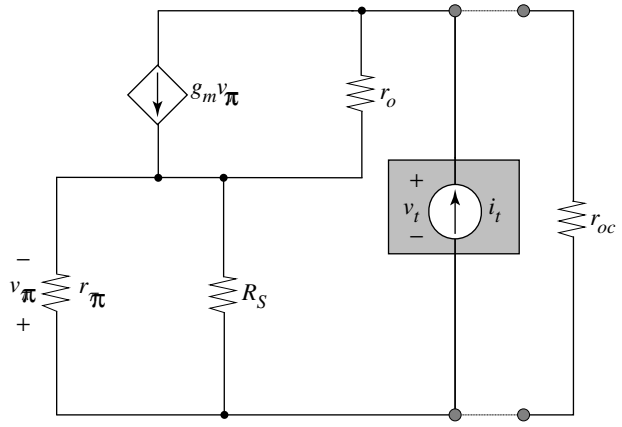
- See pages 509-510 and note that the transconductance generator dominates which yields

$$R_i = \frac{1}{g_m}$$

- A typical transconductance is around 4 mS, with $I_C = 100\ \mu A$
- Typical input resistance is 250 Ω -- very small, as desired for a current amplifier
- R_i can be designed arbitrarily small, at the price of current (power dissipation)

C. Common-Base Output Resistance R_o

- Apply test current with source resistance of input current source in place
- Note r_{oc} as is in parallel with rest of circuit



- Analysis is on pp. 510-511 of Chapter 8, with the final result boiling down to:

$$R_{out} \approx r_{oc} \| r_o \left[1 + g_m \left(r_\pi \| R_s \right) \right]$$

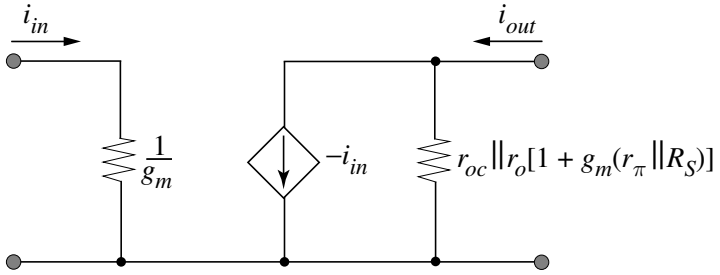
- If the R_S is much greater than r_π, then the output resistance is approximately:

$$R_{out} = r_{oc} \| \left[\beta_o r_o \right]$$

- R_{out} is limited to the small-signal resistance of the current source

D. Common-Base Two-Port Model

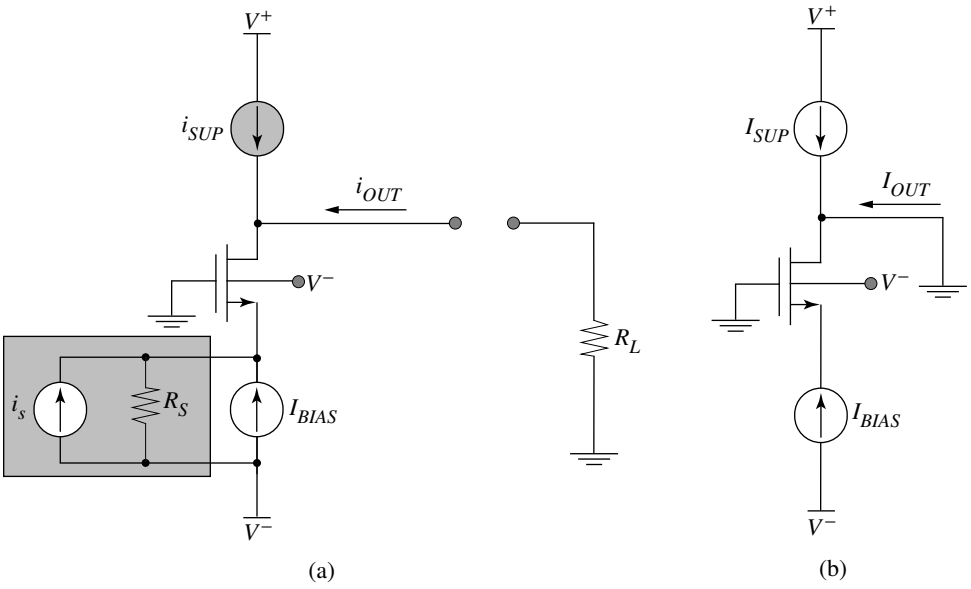
- The output resistance depends on the source resistance -- which means that the CB current buffer is not unilateral
- The two-port formal model is **not** strictly valid
- Error in using the model is **small**
- Conceptual simplification for design is **huge**



- Input resistance << CE Amplifier
- We want a small input resistance since the controlled generator is current controlled
- Output resistance >> CE Amplifier
- We want large output resistance to deliver most of the output current to the load

III. Common-Gate Amplifier

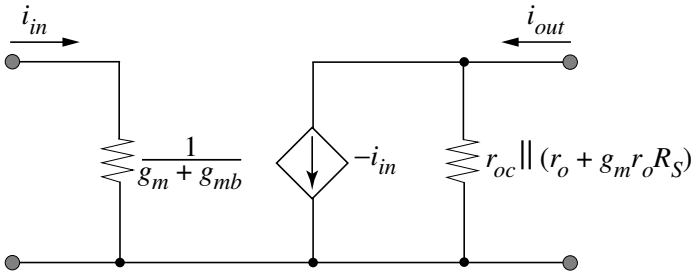
A. Circuit Configuration



- It is sometimes possible to tie the backgate to the source which shorts the backgate transconductance generator in small signal model
- It is obvious that the current gain for this amplifier must be unity, since the gate current for a MOSFET is zero
- The circuit analysis leading to the two port model is very similar to the CB amplifier -- see pp. 513 - 518 of the text.

B. Common-Gate Two-Port Model

- The resulting two port model is shown below:



- The input resistance is the same as for the CB for the case where source and backgate are shorted.
- When this isn't the case, the backgate generator is added in (which helps!):

$$R_i = \frac{1}{g_m} \qquad \text{or} \qquad R_i = \frac{1}{g_m + g_{mb}}$$

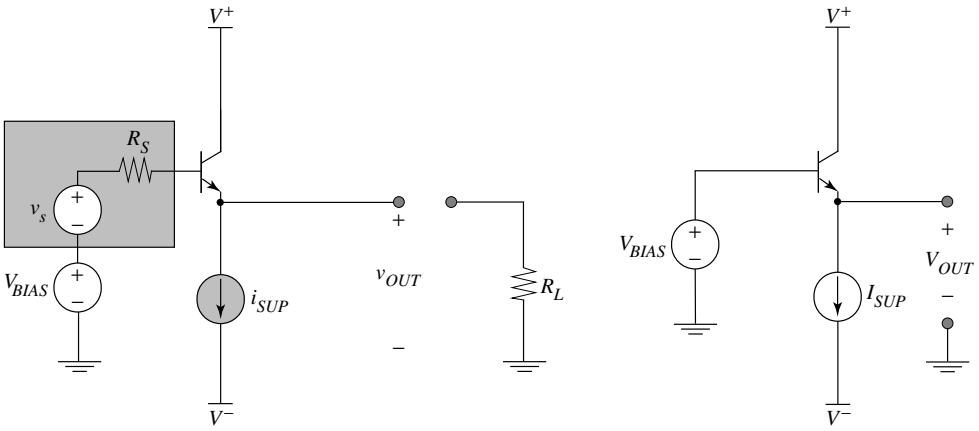
- R_i can be designed to be arbitrarily small, at the price of area, by increasing (W/L) or current
- The output resistance is similar to the CB result with r_π --> infinity

$$R_o = r_{oc} \left\| \left[r_o + g_m r_o R_S \right] \right.$$

IV. Common Collector/Drain Amplifier - Voltage Buffer

A. Introduction

- A voltage buffer takes the input voltage which may have a relatively large Thevenin resistance and replicates the voltage at the output port, which has a low output reisistance
- Input signal is applied to the base/gate, output is taken from the emitter/source
- Voltage gain is about unity
- Input resistance is high
- Output resistance is low



B. Biasing

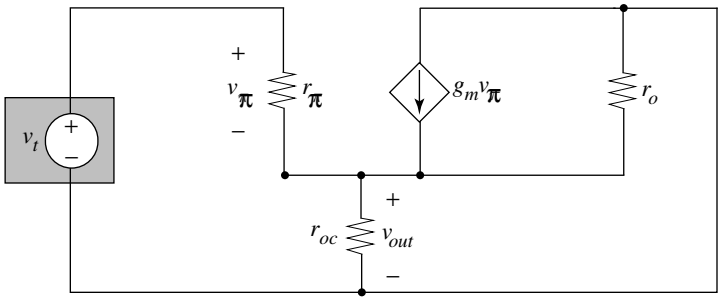
- Set V_{OUT} to "halfway" between power rails-->$V_{BIAS} - V_{BE} = V_{OUT}$

$$V_{BE} = \frac{kT}{q} \ln \frac{I_{SUP}}{I_S}$$

- Output voltage maximum $V_{CC}/2 - V_{CE(sat)} \approx V_{CC}/2 - 0.2$ V
- Output voltage minumum set by voltage requirement across I_{SUP}

V. Small-Signal Two Port Parameters

A. Common Colletor small-signal model and procedure for finding A_v



- Circuit analysis: current through $r_{oc} \parallel r_o$ is $v_\pi / r_\pi + g_m v_\pi$ -->

$$\frac{v_t - v_{out}}{r_\pi} + g_m (v_t - v_{out}) = \frac{v_{out}}{r_{oc} \parallel r_o}$$

- Multiplying by r_π and recognizing that $g_m r_\pi = \beta_o$,

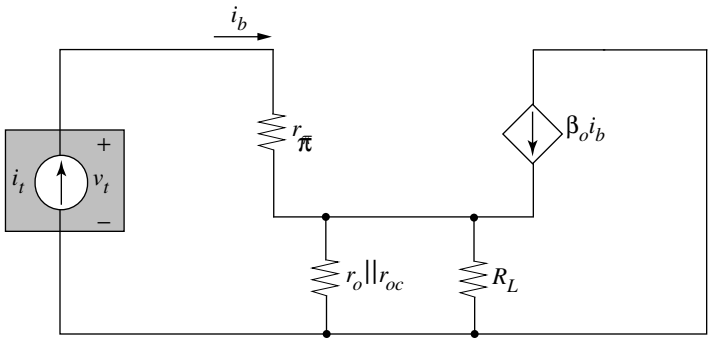
$$v_t - v_{out} + \beta_o (v_t - v_{out}) = (1 + \beta_o)(v_t - v_{out}) = \frac{v_{out}}{r_{oc} \parallel r_o} r_\pi$$

- Solving for the open-circuit voltage gain:

$$A_v = \frac{1}{1 + \dfrac{r_\pi}{r_{oc} \parallel r_o (\beta_o + 1)}} \approx 1$$

B. Common-Collector Input Resistance R_i

- Procedure: apply pure test source, leave load resistor R_L

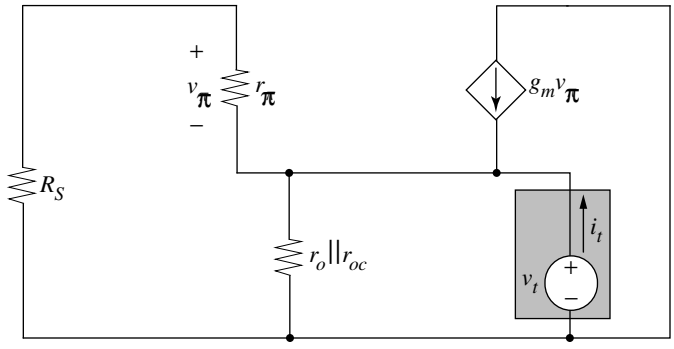


- Note that current through $r_{oc} \| r_o \| R_L$ is $i_t + \beta_o\, i_t$ -->

$$R_{in} = r_\pi + (\beta_o + 1)\left(r_{oc} \| r_o \| R_L \right)$$

C. Common Collector Output Resistance

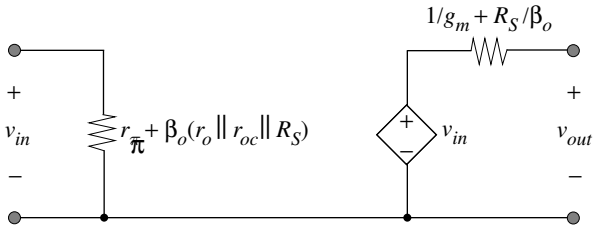
- Apply pure test current source at the output, leaving source resistance attached



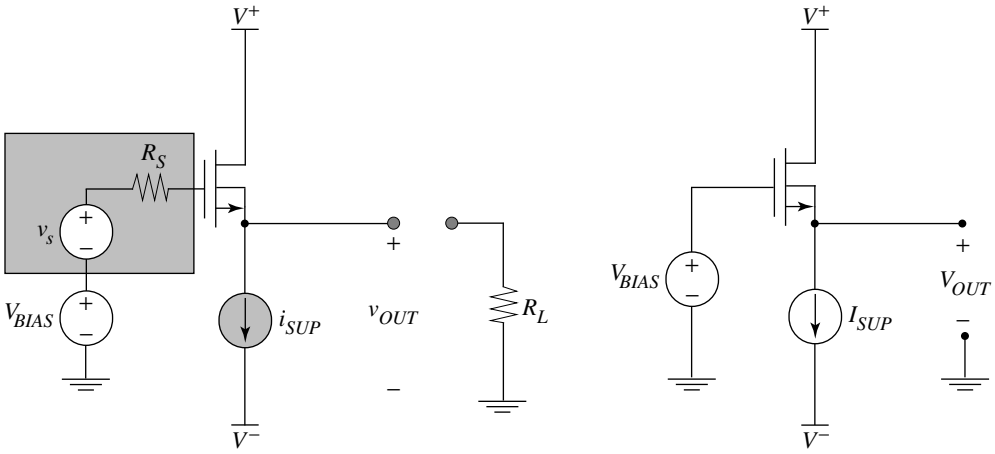
$$R_{out} \approx \frac{1}{g_m} + \frac{R_S}{\beta_o}$$

D. Common Collector Two-Port Model

- Good voltage buffer
- Non unilateral network

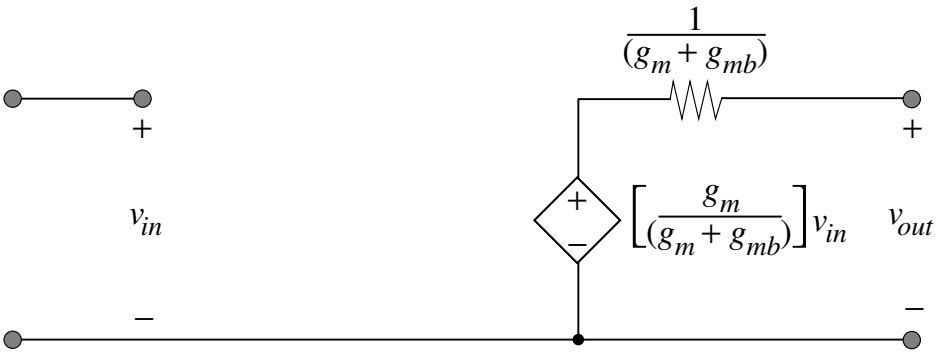


E. Common Drain Amplifier



- Analysis: much the same as for CC amplifier
- If V_{SB} isn't zero, then the voltage gain is degraded from about 1 to 0.8-0.9

F. Common Drain Amplifier Two-Port Model



- If $V_{SB} = 0$, then the voltage gain is $A_v \approx 1$ and $R_o \approx 1 / g_m$
- The CD amplifier is a reasonable voltage buffer
- Improve output resistance by increasing g_m
- Input loading is a non-issue, since the gate is open-circuited for MOSFETs.

VI. Summary

A. Single-Stage Building Blocks

Table 1: Simplified Two-Port Parameters

Amplifier Type	Controlled Source	Input Resistance R_i	Output Resistance R_o
Common Emitter	$G_m = g_m$	r_π	$r_o \parallel r_{oc}$
Common Source	$G_m = g_m$	infinity	$r_o \parallel r_{oc}$
Common Base	$A_i = -1$	$1 / g_m$	$r_{oc} \parallel r_o\,[1+g_m(r_\pi \parallel R_S)\,]$
Common Gate	$A_i = -1$	$1 / g_m$ if $v_{sb} = 0$, -otherwise- $1 / (g_m + g_{mb})$	$r_{oc} \parallel (r_o + g_m r_o R_S\,)$, if $v_{sb}=0$ -otherwise- $r_{oc} \parallel [r_o+(g_m+g_{mb})r_o R_S]$
Common Collector	$A_v = 1$	$r_\pi + \beta_o\,(r_o \parallel r_{oc} \parallel R_L)$	$(1 / g_m\,) + R_S / \beta_o$
Common Drain	$A_v = 1$ if $v_{sb} = 0$, -otherwise- $g_m / (g_m + g_{mb})$	infinity	$1 / g_m$ if $v_{sb} = 0$, -otherwise- $1 / (g_m + g_{mb})$

B. Ultra Simplified Two-Port Parameters

- $g_{mb} = 0$, common base used as a current buffer --> $R_S >> r_\pi$

Table 2: Ultra Simplified Two-Port Parameters

Amplifier Type	Controlled Source	Input Resistance R_i	Output Resistance R_o
Common Emitter	$G_m = g_m$	r_π	$r_o \parallel r_{oc}$
Common Source	$G_m = g_m$	infinity	$r_o \parallel r_{oc}$
Common Base	$A_i = -1$	$1 / g_m$	$r_{oc} \parallel (\beta_o r_o)$
Common Gate	$A_i = -1$	$1 / g_m$	$r_{oc} \parallel (g_m R_S r_o)$
Common Collector	$A_v = 1$	$r_\pi + \beta_o (r_o \parallel r_{oc} \parallel R_L)$	$(1 / g_m) + R_S / \beta_o$
Common Drain	$A_v = 1$	infinity	$1 / g_m$

- This table is adequate for first-cut hand design