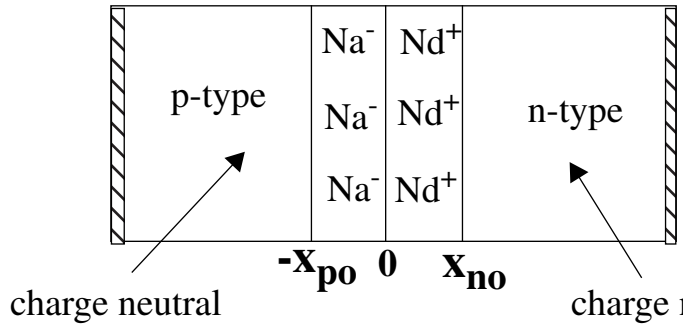
I. pn Junction - Quantitative Electrostatics - Thermal Eq.

A. The Depletion Approximation



- In the bulk regions far away from the junction, we can approximate

$$\rho = 0$$

- Near the junction, the charge density is maximum. From $0 < x < x_{no}$:

$$\rho = q\,(p_o + N_d - n_o - N_a) = q\,(N_d - n_o)$$

since there are no acceptors on this side and the hole concentration is negligible.

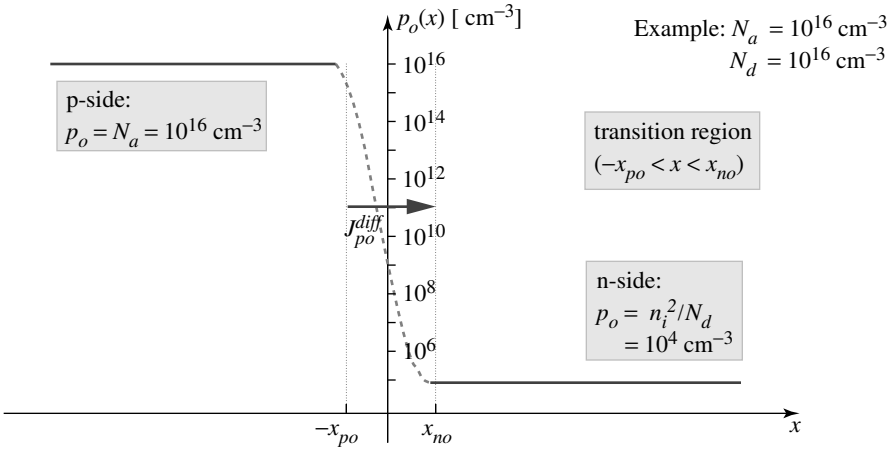
- Recall

$$\phi_o = V_{th} \ln\left(\frac{n_o}{n_i}\right)$$

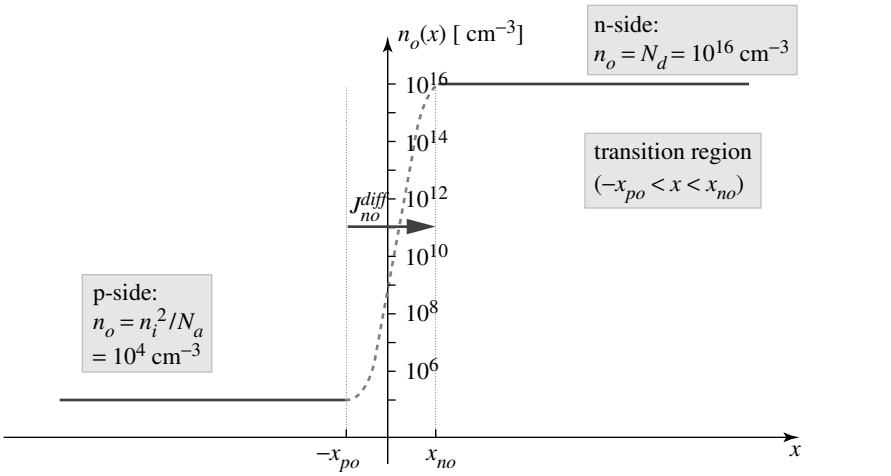
$$\rho(x) \cong q\left(N_d - n_i e^{\phi(x)/V_{th}}\right) \qquad \left(0 \le x \le x_{no}\right)$$

$$\frac{\partial^2 \phi}{\partial x^2} = -\frac{\rho(x)}{\varepsilon_s}$$

- Qualitative hole and electron concentration in Thermal Equilibrium



(a)



(b)

- For hand calculations, we will assume that

$$\rho = q N_d \quad (0 < x < x_n)$$

$$\rho = - q N_a \quad (-x_p < x < 0)$$

$$\rho = 0 \quad (x < -x_p), (x > x_n)$$

B. One more time ...

- Bulk silicon is *CHARGE NEUTRAL*, to a good approximation
- Region 1 is *bulk*

$$\rho = q\left(N_d + p_o - N_a - n_o\right) \cong 0 \qquad \text{-->} \qquad p_o \cong N_a$$

- Region 4 is *bulk*:

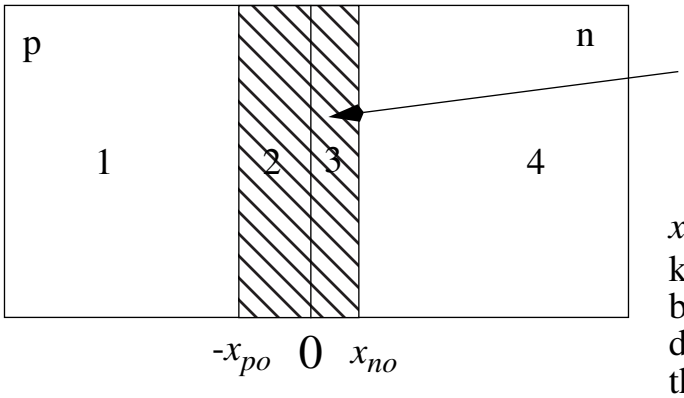
$$\rho = q\left(N_d + p_o - N_a - n_o\right) \cong 0 \qquad \text{-->} \qquad n_o \cong N_d$$

- Near the junction, the silicon is *DEPLETED* of mobile carriers:
- region 2 is *depleted*:

$$\rho = q\left(N_d + p_o - N_a - n_o\right) \cong -qN_a$$

- region 3 is *depleted*:

$$\rho = q\left(N_d + p_o - N_a - n_o\right) \cong qN_d$$

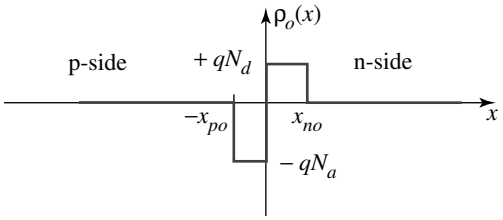


Depletion Region

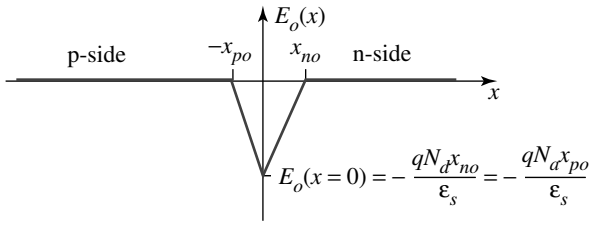
x_{no}, $-x_{po}$ are not known -- use boundary conditions to find them.

C. Quantitative pn Junction in Thermal Equlibrium:

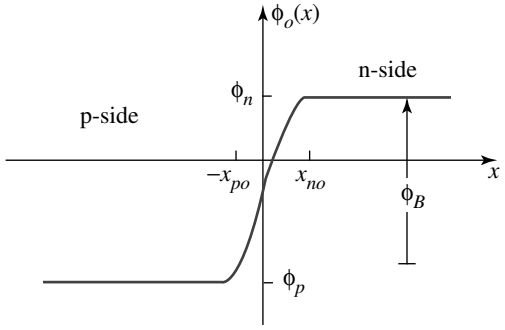
- Using the Depletion Approximation



(a)



(b)



(c)

- Charge in depletion region must sum to zero

$$qN_d x_{no} = qN_a x_{po}$$

- Electrostatic potential is continuous

$$\phi(0) = \phi_p + \frac{qN_a}{2\varepsilon_s}\left(x_{po}\right)^2 = \phi_n - \frac{qN_d}{2\varepsilon_s}\left(x_{no}\right)^2$$

D. Depletion Widths in Thermal Equilibrium

- See detailed calculations in Chapter 3

$$x_{po} = \sqrt{\left(\frac{2\varepsilon_s \phi_B}{qN_a}\right)\left(\frac{N_d}{N_d + N_a}\right)}$$

$$x_{no} = \sqrt{\left(\frac{2\varepsilon_s \phi_B}{qN_d}\right)\left(\frac{N_a}{N_d + N_a}\right)}$$

$$X_{do} = x_{no} + x_{po} = \sqrt{\left(\frac{2\varepsilon_s \phi_B}{q}\right)\left(\frac{1}{N_a} + \frac{1}{N_d}\right)}$$

- Asymmetric junctions: i.,e., $N_a >> N_d$ or $N_d >> N_a$.
- most of depletion width is on the side with the lower doping, since

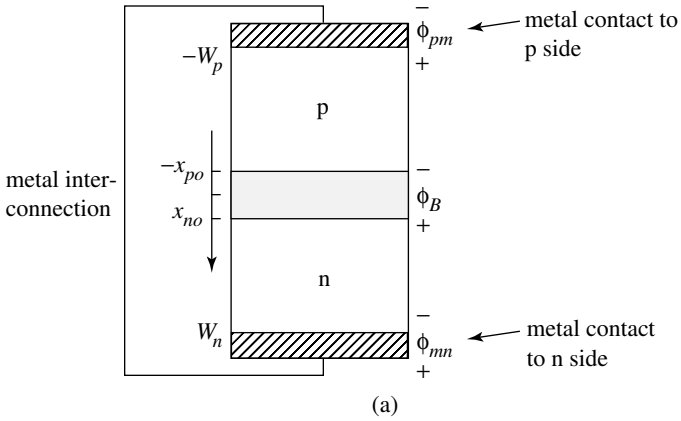
$$\frac{1}{N_a} + \frac{1}{N_d} \approx \frac{1}{N_d} \qquad (N_a \gg N_d)$$

$$\frac{1}{N_a} + \frac{1}{N_d} \approx \frac{1}{N_a} \qquad (N_d \gg N_a)$$

- many IC pn junctions are asymmetric

E. Contact Potentials

- The metal layers are also part of the device. What role do they play?
- Potential jumps at the contact -- same phenomenon as built-in barrier at pn junction.
- ϕ_{mp} = barrier from metal to p-type silicon= $-\phi_{pm}$
- ϕ_{nm} = barrier from n-type silicon to metal



- Kirchhoff's voltage law

$$0 = -\phi_{mp} + \phi_B - \phi_{nm} \quad \text{--->} \quad \phi_B = \phi_{mp} + \phi_{nm}$$

$$\phi_B = \phi_n - \phi_p$$

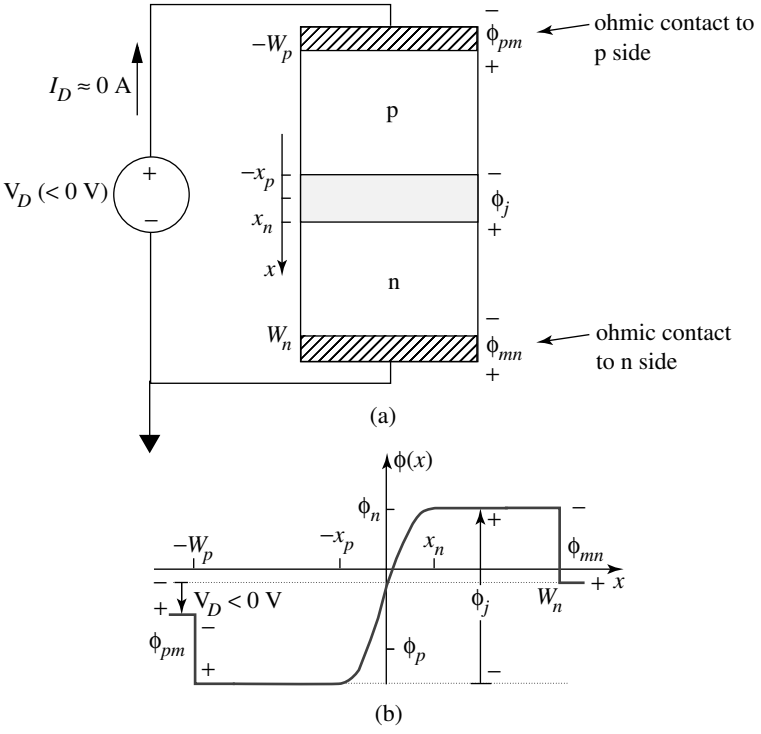
F. Reverse Bias

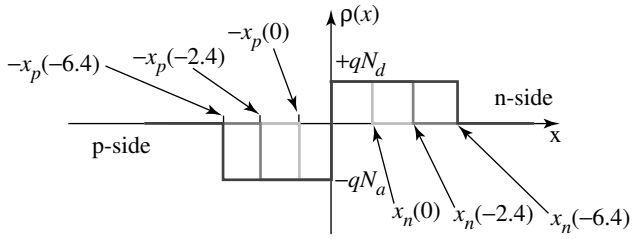
- Assume no current flows

$$x_p(V_D) = \sqrt{\left(\frac{2\varepsilon_s\left(\phi_B - V_D\right)}{qN_a}\right)\left(\frac{N_d}{N_d + N_a}\right)} = x_{po}\sqrt{1 - \left(V_D/\phi_B\right)}$$

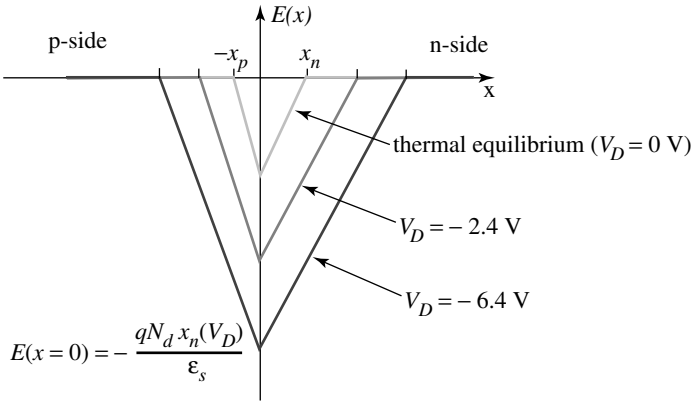
$$x_n(V_D) = \sqrt{\left(\frac{2\varepsilon_s\left(\phi_B - V_D\right)}{qN_d}\right)\left(\frac{N_a}{N_d + N_a}\right)} = x_{no}\sqrt{1 - \left(V_D/\phi_B\right)}$$

$$X_d(V_D) = \sqrt{\left(\frac{2\varepsilon_s\left(\phi_B - V_D\right)}{q}\right)\left(\frac{1}{N_a} + \frac{1}{N_d}\right)} = X_{do}\sqrt{1 - \left(V_D/\phi_B\right)}$$

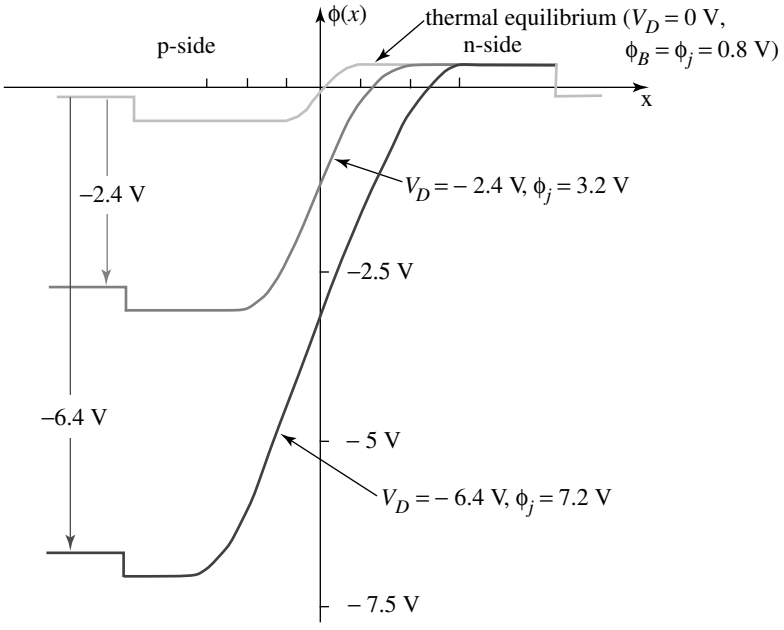



ρ(x)
$-x_p(0)$
$-x_p(-6.4)$
$-x_p(-2.4)$
$+qN_d$
n-side
x
p-side
$-qN_a$
$x_n(0)$
$x_n(-2.4)$
$x_n(-6.4)$

(a)


E(x)
p-side
$-x_p$
x_n
n-side
x
thermal equilibrium ($V_D = 0$ V)
$V_D = -2.4$ V
$V_D = -6.4$ V
$E(x=0) = -\frac{qN_d\, x_n(V_D)}{\varepsilon_s}$

(b)


ϕ(x)
thermal equilibrium ($V_D = 0$ V,
$\phi_B = \phi_j = 0.8$ V)
p-side
n-side
x
$V_D = -2.4$ V, $\phi_j = 3.2$ V
–2.4 V
–2.5 V
–6.4 V
– 5 V
$V_D = -6.4$ V, $\phi_j = 7.2$ V
– 7.5 V