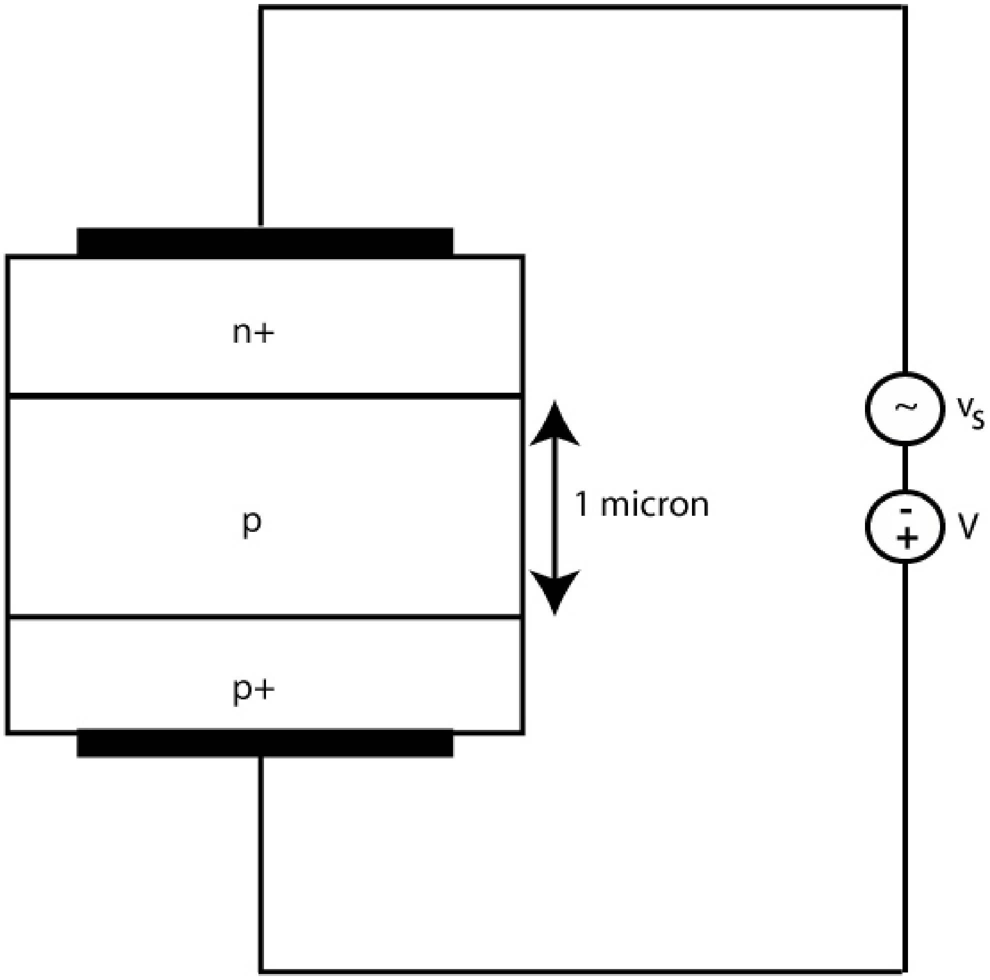
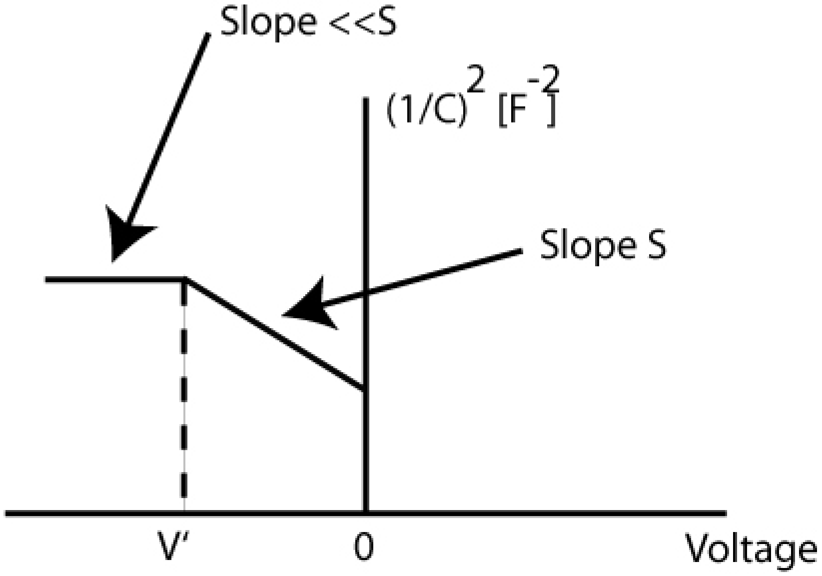
Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science
6.012
Microelectronic Devices and Circuits
Spring 2007
February 28, 2007 - Homework #3
Due - March 9, 2007

Problem 1

The device drawn below is biased as shown, and a capacitance-voltage (C-V) measurement is taken. The area of the device is 10^{-6} cm^2. Assume the electrostatic potential in the n+ silicon region, φ_{n+}=550mV.

A plot of $(1/C)^2$ as a function of the DC voltage, V, where C is the capacitance is shown below. The device is in reverse bias. The slope, S, is -4.8 * 10^{26} F^{-2} V^{-1}.
NOTE: The polarity of the DC source is now shown correctly.





a) Derive an expression for the doping, N$_a$, in the p-type region in terms of the slope S, shown in the plot, and other known parameters (e.g. constants like q ε_{Si}, the device area).

b) Assume now that N$_a$ is 10^{16} cm^{-3}. Estimate the DC voltage V' where the slope of the plot of $(1/C)^2$ vs. voltage changes, as seen in the graph.

a) $$C_j(V) = \frac{C_{jO}\times A}{\sqrt{1-V/\phi_B}} \longrightarrow \left(\frac{1}{C_j}\right)^2 = \frac{1-V/\phi_B}{C_{jO}^2\times A^2} = \frac{\phi_B - V}{\phi_B^2\times C_{jO}^2\times A^2}$$

$$Slope, S = \frac{-1}{\phi_B^2\times C_{jO}^2\times A^2} \qquad C_{jO} = \sqrt{\frac{q\times\varepsilon_{Si}\times N_a}{2\times\phi_B}}$$

$$N_a = \frac{-2}{A^2\times q\times\varepsilon_{Si}\times S}$$

Plugging in the numbers, we find N$_a$=2.5 x 10^{16} cm^{-3}. The numerical answer is not necessary.

b) The slope will change when the 1 micron wide p-type region is completely depleted, i.e., x$_d$=1 micron.

$$x_d(V) = x_{dO}\times\sqrt{1-V'/\phi_B}$$

$$\phi_B = \phi_{n+} - \phi_p = .55-(-.36) = 0.91V$$

$$x_{dO} = \sqrt{\frac{2 \times \varepsilon_{Si} \times \phi_B}{q \times N_a}} = 3.44 \times 10^{-5}\, cm$$

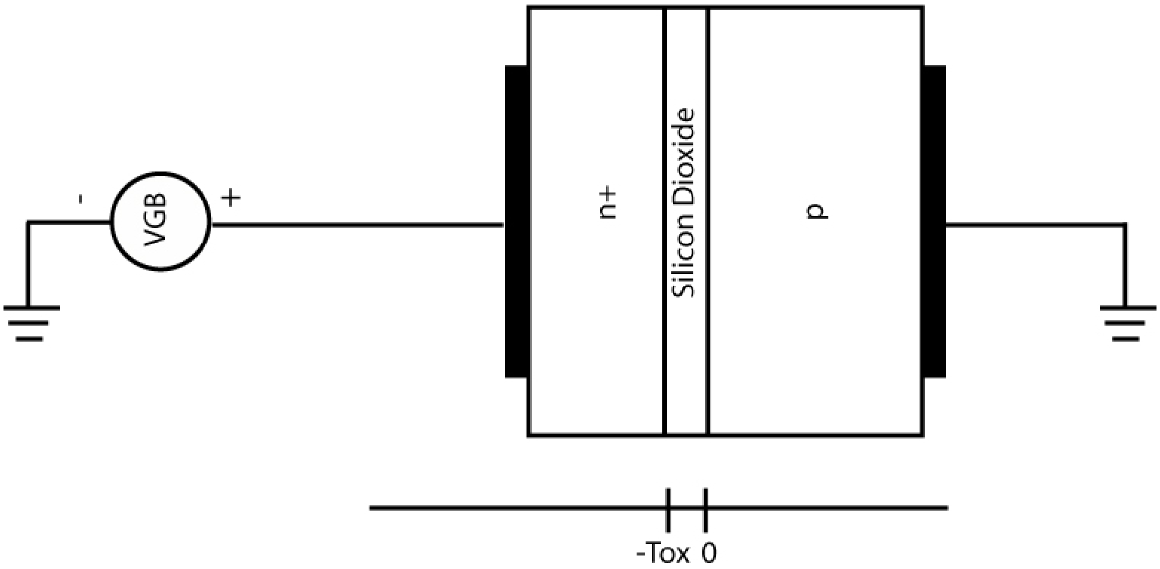
$$x_d \big/ x_{dO} = \sqrt{1 - V' \big/ \phi_B} = \frac{10^{-4}\, cm}{3.44 \times 10^{-5}\, cm} = 2.91$$

Solving for V`, we find

$$V' = -6.8V$$

Problem 2

A metal-oxide-semiconductor (MOS) device is pictured below. T_{ox} is 15nm. Assume φ_{n+}=0.55V, and that N_a in the p region is 10^{17} cm^{-3}.



a) Find the threshold voltage of this device.
b) What applied bias leads to a sheet charge density in the inversion layer, Q_N, of -10^{-6} C/cm^2?
c) What is the value of E_{ox}, the field in the oxide, when the charge on the gate, Q_G= 10^{-6} C/cm^2?

a) The threshold voltage is the V_{GB} applied to make the potential at x=0 equal to -$\varphi_{p.}$

First find the flatband voltage, V_{FB}.

$$V_{FB} = -(\phi_{gate} - \phi_{bulk}) = -(.55 + .42) = -0.97V$$

$$V_T = V_{FB} - 2\phi_p + 1 \big/ C_{ox} \times \sqrt{2 \times q \times \varepsilon_{Si} \times N_a \times (-2\phi_p)}$$

$$C_{ox} = \varepsilon_{SiO2} / t_{ox} = 2.3 \times 10^{-7}\, F/cm^2$$

Plugging these values into the threshold voltage equation:

$$V_T = 0.58V$$

b) Above threshold, we know how to relate the inversion charge, Q_N, to the applied gate to bulk voltage through the following equation.

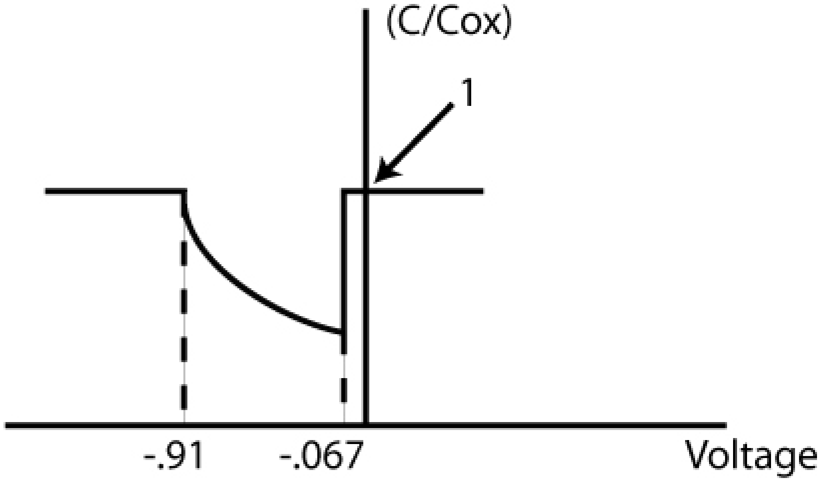
$$Q_N = -C_{ox}(V_{GB} - V_T) \longrightarrow V_{GB} = 0.58V - \frac{-10^{-6}\, C/cm^2}{2.3 \times 10^{-7}\, F/cm^2} = 4.9V$$

c) We can use Gauss's law to find the magnitude of the electric field in the oxide.

$$E_{ox} = Q_G / \varepsilon_{SiO2} = 2.9 \times 10^{6}\, V/cm$$

Problem 3

Shown below is a capacitance-voltage plot for an MOS capacitor. The gate is n+, therefore you can assume its potential is 550mV. The silicon dioxide thickness is 15nm, and the body is doped with some concentration of acceptors, N_a.



a) Determine the threshold voltage, V_T, and the flatband voltage, V_{FB}, on the C-V plot.
b) Specify the range of voltages where the MOS capacitor is in inversion, depletion, and accumulation.
c) Calculate the doping concentration in the body, N_a, from the given information
d) Now assume the gate is doped p+, so the potential of the gate is -550mV. Sketch the C-V, labeling V_T and V_{FB}.

a) By looking at the shape of the C-V, we know that -.91V is the flatband voltage, and -0.067V is the threshold voltage. Since our substrate is p-type, as we go to voltages more positive than V_T, we will be balancing the positive charge on the gate with free electrons in the inversion layer. As we go to voltages more negative than V_{FB}, we will be balancing negative charge on the gate with free holes in the accumulation layer.

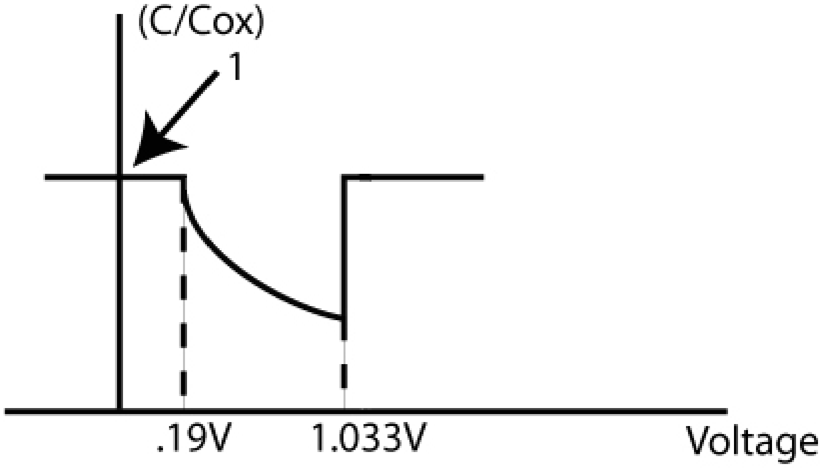
b) Accumulation: $V \le -0.91V$, Depletion: $-0.91V < V < -0.067V$
Inversion: $V \ge -0.067V$

c) We can most easily calculate the doping concentration from the flatband voltage.

$$V_{FB} = -(\phi_{gate} - \phi_{bulk}) = -\left(.55V - \left(-60mV \times \log\left(\frac{N_a}{n_i}\right)\right)\right) = -0.91V$$

$$N_a = 10^{16}\,cm^{-3}$$

d) By changing the gate from n+ to p+, we change the gate's potential from 550mV to -550mV. That results in a translation of the C-V 1100mV to the right.



Problem 4

It is sometimes useful in analog circuits to use a transistor biased in triode as a voltage controlled resistor. Use the following parameters to design a p-channel MOSFET with a resistance of 100KΩ.
$\mu_p Cox = 25\mu A/V^2$ $V_{Tp} = -1V$ $V_{GS} = -1.2V$ $V_{BS} = 0V$

a) If the device has a width of 10μm, what is the necessary length?
b) What is the necessary width to get a 10KΩ resistor, if the length is 5μm?

a) When the MOSFET is in the linear region, it behaves like a voltage controlled resistor. The resistance of a PMOSFET in the linear region can be written as:

$$R = \frac{1}{\mu_p \times C_{ox} \times \frac{W}{L} \times (V_{SG} + V_{Tp})}$$

Now, we can solve for the length to achieve a resistance of 100KΩ.

$$100K\Omega = \frac{1}{25 \,{}^{\mu A}\!/_{V^2} \times \frac{10}{L} \times (V_{SG} - 1)} \longrightarrow L = 5\mu m$$

b) We will use the same equation and solve for the width.

$$10K\Omega = \frac{1}{25 \,{}^{\mu A}\!/_{V^2} \times \frac{W}{5} \times (V_{SG} - 1)} \longrightarrow W = 100\mu m$$

Problem 5

Hafnium dioxide (HfO_2, ε= 25) is an attractive replacement for silicon dioxide as a gate dielectric due to its high dielectric constant.

Consider an n-channel MOSFET. The channel length, L = 2μm, the width, W = 30μm, the electron mobility is $\mu_n = 300\ cm^2V^{-1}s^{-1}$ and the substrate doping is $N_a = 10^{17}cm^{-3}$. Assume the gate is n+ silicon, so its potential is 550mV.

a) What thickness of HfO_2 is needed for $V_{Tn} = 0.5$ V?
b) Find the backgate effect parameter, γ_n for the hafnium dioxide gate insulator thickness from (a).
c) If I=5μA, what is V_{GS}? Assume saturation. What is the minimum drain voltage to ensure saturation?

a) First calculate the flatband voltage.

$$V_{FB} = -(\phi_{gate} - \phi_{bulk}) = -(.55V - (-.42V)) = -0.97V$$

$$V_T = 0.5V = V_{FB} - 2\phi_p + {}^{1}\!/_{C_{ox}} \times \sqrt{2 \times q \times \varepsilon_{Si} \times N_a \times (-2\phi_p)}$$

$$C_{ox} = {}^{\varepsilon_{HfO2}}\!/_{t_{ox}}$$

Plugging in the known quantities and solving for t_{ox}:

t_{ox}=85 nanometers

b)

$$\gamma_n = \frac{\sqrt{2 \times \varepsilon_{Si} \times q \times N_a}}{C_{ox}}$$

$$C_{ox} = \varepsilon_{HfO2} / t_{ox} = \frac{2.21 \times 10^{-12}\ F/cm}{85 \times 10^{-7}\ cm} = 2.6 \times 10^{-7}\ F/cm^2$$

$$\gamma_n = \frac{\sqrt{2 \times \varepsilon_{Si} \times q \times N_a}}{C_{ox}} = 0.687 V^{1/2}$$

c) The drain current equation for an NMOSFET in saturation is shown below.

$$I_d = \frac{1}{2} \times \frac{W}{L} \times \mu_n \times C_{ox} \times (V_{GS} - V_T)^2$$

If I_d is 5μA, we can solve for V_{GS}.

$$5\mu A = \frac{1}{2} \times \frac{30}{2} \times 300 \times 2.6 \times 10^{-7} (V_{GS} - 0.5)^2 \longrightarrow V_{GS} = 0.59V$$

To ensure saturation, the drain source voltage, V_{DS}, must be greater than or equal to $V_{DS,SAT}$=V_{GS}-V_T=.09V. Therefore, the minimum drain source voltage to ensure saturation is 0.09V.