

- Course Roadmap
- Rectification
- Bipolar Junction Transistor

Acnowledgements:
Neamen, Donald: Microelectronics Circuit Analysis and Design, 3rd Edition
The Art Of Electronics by Horowitz and Hill

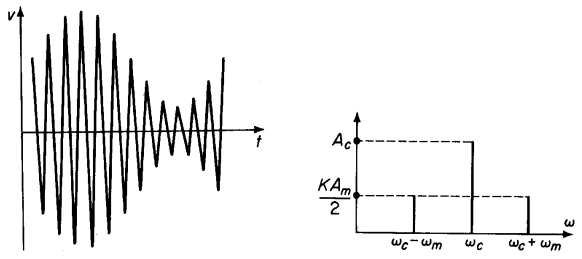
6.101 Course Roadmap

- Passive components: RLC – with RF
- Diodes
- Transistors: BJT, MOSFET
- Op-amps, 555 timer, ECG
- Switch Mode Power Supplies
- Fiber optics, PPG
- Applications

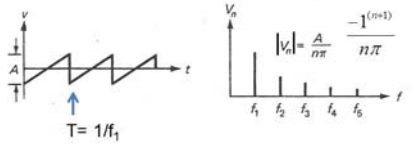
Time Domain Analysis

$$v = (A_c + KA_m \cos\omega_m t) * \cos\omega_c t$$

$$v = A_c \cos\omega_c t + \frac{KA_m}{2}[\cos(\omega_c - \omega_m)t + \cos(\omega_c + \omega_m)t]$$



Fourier Series - Ramp



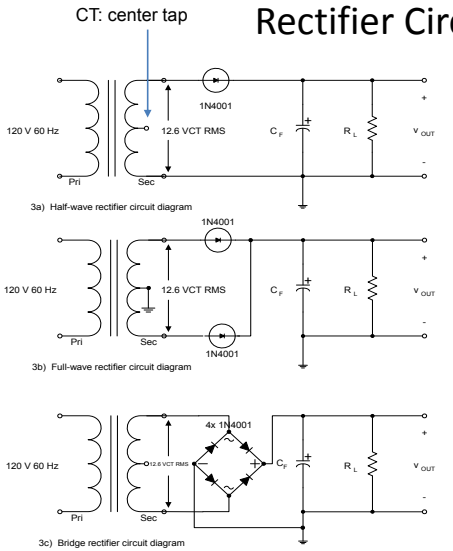

```
function [ t, sum ] = ramp(number)
%generate a ramp based on fixed number of terms
%
t = 0:.1:pi*4; % display two full cycles with 0.1 spacing

sum = 0
for n=1:number
      sum = sum + sin(n*t)*(-1)^(n+1)/(n*pi);
      end

plot(t, sum)
shg

end
```

Rectifier Circuits



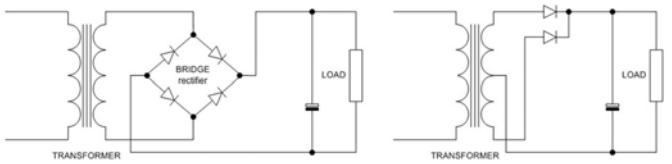
V_{out} =

V_{out} =

V_{out} =

RC >> 16.6ms why?

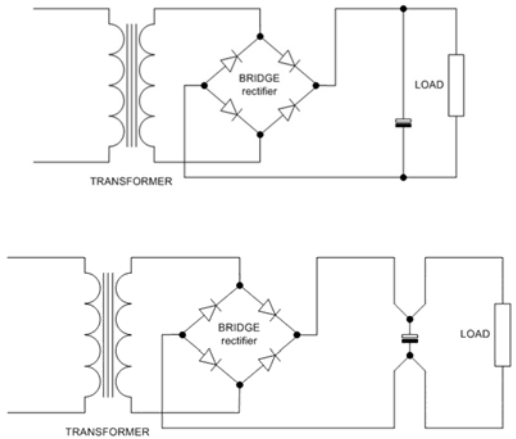
Full Wave Bridge vs Center Tapped



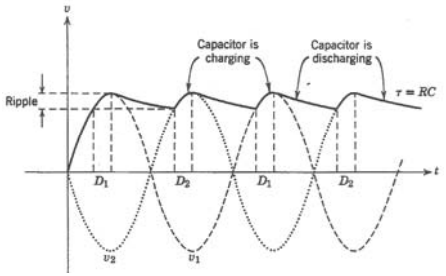
Center tapped advantages:

- Lower diode voltage drop (high efficiency)
- Secondary windings carries ½ average current (thinner windings, easier to wind)
- Used in computer power supplies

Physical Wiring Matters



Power Supply Ripple Voltage Calculation



D_2 conduction angle in degrees

Load Current I_L = 100 mA; RL ~ 160 Ω; C = 1000 μF; Vrms = 12 v

$\tau = RC = 160 \times 1000 \times 10^{-6} = 160\text{ms} >> 8.3\text{ms}$

60 Hz = 16.6 ms 120 Hz = 8.3 ms

$i_C = C\frac{dV}{dt}$ or, for this approximation: $i_C = C\frac{\Delta V}{\Delta t}$.

Solve for $\Delta V = \frac{i\Delta t}{C}$, where ΔV = ripple voltage, v_r.

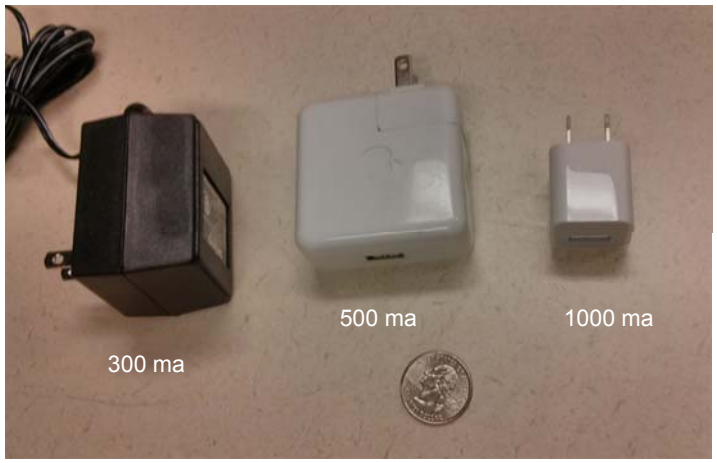
$$v_r = \frac{0.1A \times 8.3ms}{1000\mu F} = \frac{0.1 \times 8.3 \times 10^{-3}}{10^{-3}}; v_r = 0.83volt$$

V_{DCMAX} = 1.4 x 12v = 16.8v

V_{DCMIN} = 16.8v - 0.83v = 16.0v

V_{DCAVE} = [16.8 - 16.0]/2 = 16.4v

5 V Adapters



Diode AC Resistance

i_D = DC + AC signal; I_D = DC signal; i_d = AC signal; V_{TH} = 25mV at 25° C

$$i_D \cong I_S\left[e^{\left(\frac{v_D}{V_{TH}}\right)}\right] = I_S\left[e^{\left(\frac{V_{DQ}+v_d}{V_{TH}}\right)}\right] \quad 1.1$$

$$i_D = I_S\left[e^{\left(\frac{V_{DQ}}{V_{TH}}\right)}\right] \bullet \left[e^{\left(\frac{v_d}{V_{TH}}\right)}\right] = \text{DC term} \bullet \text{AC term} \quad 1.2$$

If the AC signal is small, that is $v_d << V_{TH}$, then we can use a Taylor series

$$e^{\left(\frac{v_d}{V_{TH}}\right)} \cong 1 + \frac{v_d}{V_{TH}} \text{ (AC term becomes linear)} \quad 1.3$$

$$i_D = I_{DQ} \bullet \left[1 + \frac{v_d}{V_{TH}}\right] = I_{DQ} + \frac{I_{DQ}}{V_{TH}} \bullet v_d \quad 1.4$$

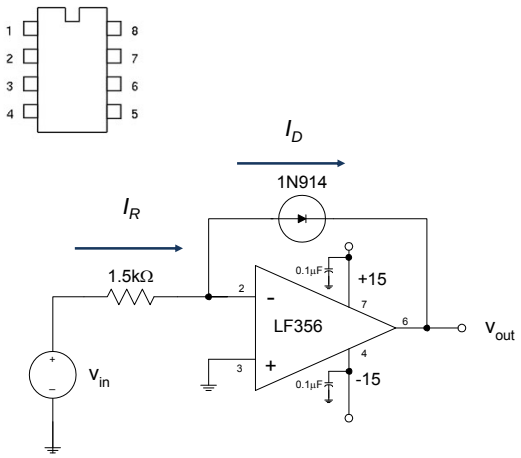
$$i_D = I_{DQ} + \frac{I_{DQ}}{V_{TH}} \bullet v_d, \quad 1.5$$

$\frac{I_{DQ}}{V_{TH}}$ has the dimensions of conductance, [mhos, or inverted ohms];

and is a constant [g_d]

AC conductance is a linear function of the DC BIAS CURRENT!

Log Amplifier



bypass caps
0.1uf caps (2)

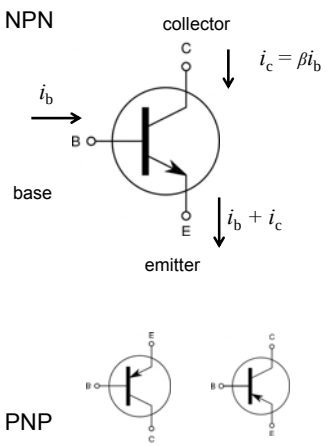
$I_R = -I_D$

$V_{out} = -V_D$

$$I_D = I_S\left(e^{\left[\frac{qV_D}{kT}\right]} - 1\right) \approx I_S e^{\left[\frac{qV_D}{kT}\right]}$$

$$V_{out} = -\frac{kT}{q} ln\left(\frac{V_{in}}{1.5k * I_S}\right)$$

Bipolar Junction Transistors



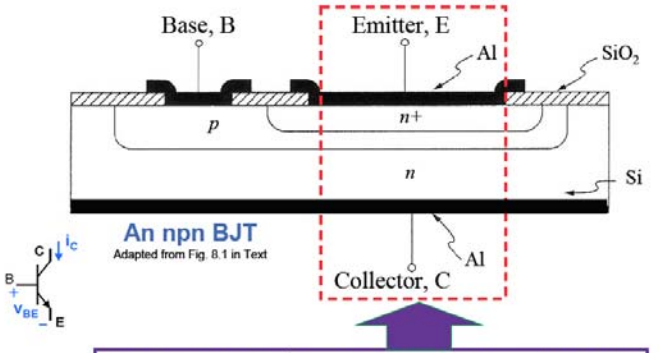
- BJT can operate in a linear mode (amplifier) or can operate as a digital switch.
- Current controlled device
- Two families: npn and pnp.
- BJT's are current controlled devices
- NPN – 2N2222
- PNP – 2N2907
- V_{CE} ~30V, 500 mw power

Why BJT's ?

- Preferred device for demanding analog application, both integrated and discrete (lower noise)
- Great for high frequency applications; characteristics well understood.
- High reliability makes it a key device in automotive applications.
- Lower output resistance at emitter vs source
- Larger g_m compared to FET

How do we make a BJT?

Basic Bipolar Junction Transistor (BJT) - *cross-section*

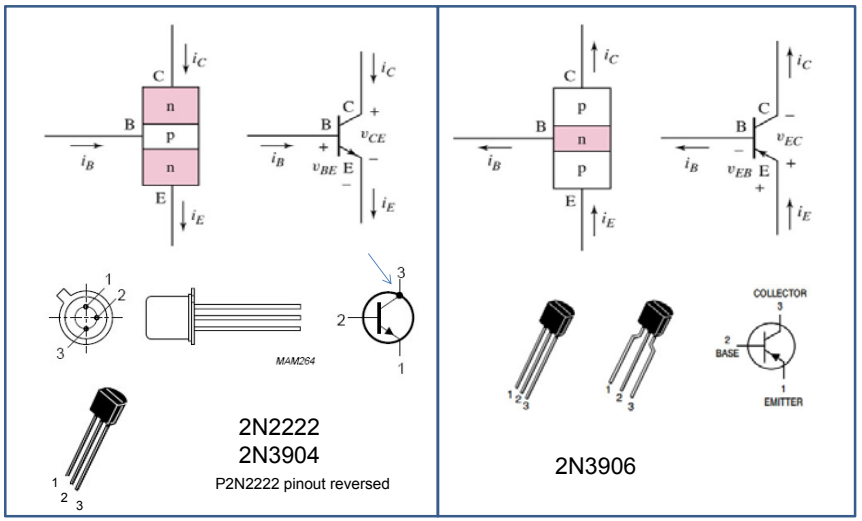


The heart of the device, and what we will model

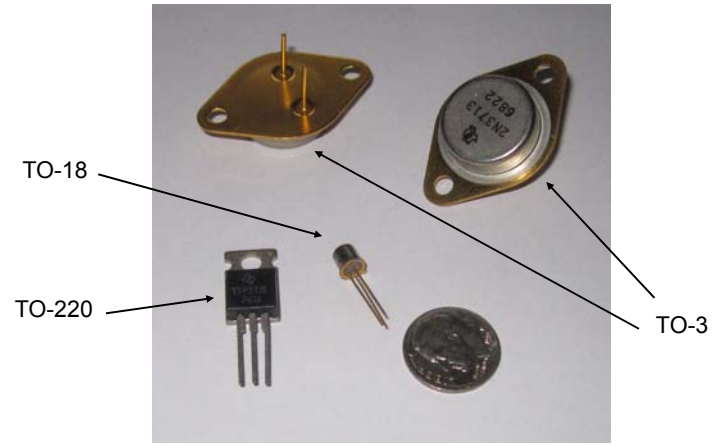
How does it work?

Clif Fonstad, 10/1/09 Lecture 7 - Slide 10

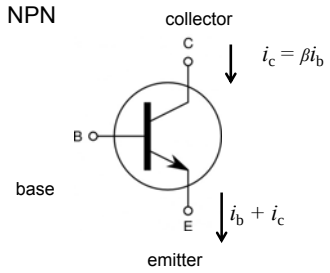
BJT Symbols



Packaging



BJT Current Relationship



$$i_E = i_C + i_B$$

$$i_C = \beta i_B$$

$$i_E = (\beta + 1) i_B$$

$$i_C = \alpha i_E$$

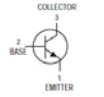
$$\beta = \frac{\alpha}{1 - \alpha}$$

h_{FE} = β = large signal (DC) gain at fixed current

$h_{FE} < h_{fe}$

General Purpose Transistors
NPN Silicon

2N3903
2N3904*
*Motorola Preferred Device





CASE 29–04, STYLE 1
TO–92 (TO–226AA)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	40	Vdc
Collector–Base Voltage	V_{CBO}	60	Vdc
Emitter–Base Voltage	V_{EBO}	6.0	Vdc
Collector Current — Continuous	I_C	200	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0	mW mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 12	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS(1)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Breakdown Voltage (2) (I_C = 1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	40	—	Vdc
Collector–Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	$V_{(BR)CBO}$	60	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	$V_{(BR)EBO}$	6.0	—	Vdc
Base Cutoff Current (V_{CE} = 30 Vdc, V_{EB} = 3.0 Vdc)	I_{BL}	—	50	nAdc
Collector Cutoff Current (V_{CE} = 30 Vdc, V_{EB} = 3.0 Vdc)	I_{CEX}	—	50	nAdc

1. Indicates Data in addition to JEDEC Requirements.
2. Pulse Test: Pulse Width ≤ 300 μs; Duty Cycle ≤ 2.0%.

max voltage

max continuous current

max power at 25° C

2N3903 2N3904

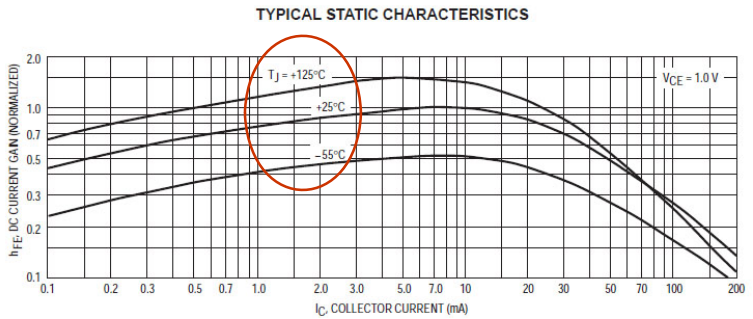
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Continued)

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS					
DC Current Gain(1) (I_C = 0.1 mAdc, V_{CE} = 1.0 Vdc)	2N3903 2N3904	h_{FE}	20 40	— —	—
(I_C = 1.0 mAdc, V_{CE} = 1.0 Vdc)	2N3903 2N3904	β	35 70	— —	
(I_C = 10 mAdc, V_{CE} = 1.0 Vdc)	2N3903 2N3904		50 100	150 300	
(I_C = 50 mAdc, V_{CE} = 1.0 Vdc)	2N3903 2N3904		30 60	— —	
(I_C = 100 mAdc, V_{CE} = 1.0 Vdc)	2N3903 2N3904		15 30	— —	
Collector–Emitter Saturation Voltage(1) (I_C = 10 mAdc, I_B = 1.0 mAdc) (I_C = 50 mAdc, I_B = 5.0 mAdc)		$V_{CE(sat)}$	— —	0.2 0.3	Vdc
Base–Emitter Saturation Voltage(1) (I_C = 10 mAdc, I_B = 1.0 mAdc) (I_C = 50 mAdc, I_B = 5.0 mAdc)		$V_{BE(sat)}$	0.65 —	0.85 0.95	Vdc
SMALL–SIGNAL CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	2N3903 2N3904	f_T	250 300	— —	MHz
Output Capacitance (V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz)		C_{obo}	—	4.0	pF
Input Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)		C_{ibo}	—	8.0	pF
Input Impedance (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N3903 2N3904	h_{ie}	1.0 1.0	8.0 10	kΩ
Voltage Feedback Ratio (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N3903 2N3904	h_{re}	0.1 0.5	5.0 8.0	$\times 10^{-4}$
Small–Signal Current Gain (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N3903 2N3904	h_{fe}	50 100	200 400	—
Output Admittance (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{oe}	1.0	40	μmhos
Noise Figure (I_C = 100 μAdc, V_{CE} = 5.0 Vdc, R_S = 1.0 kΩ, f = 1.0 kHz)	2N3903 2N3904	NF	— —	6.0 5.0	dB

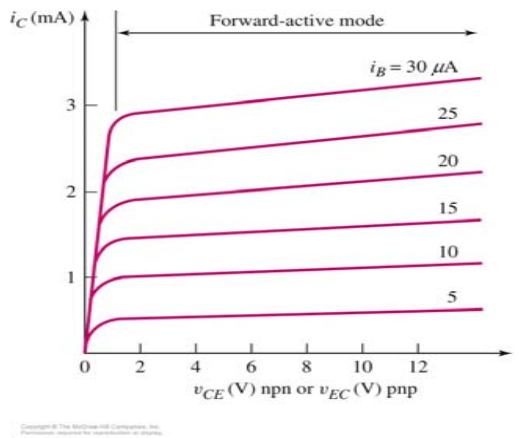
h_{FE} = f(I_c) peaks at ~ 0.5-10ma

h_{FE} @1.0ma < h_{fe} @1.0ma

hFE & Current & Temperature Characteristics



NPN Common Emitter V-I Relationship



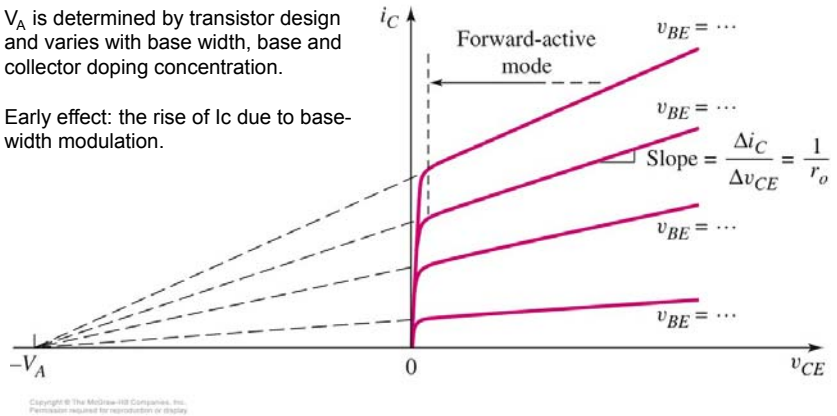
β = ?

(James) Early Voltage

A large V_A is desirable for high voltage gains ~ 30-50v.

V_A is determined by transistor design and varies with base width, base and collector doping concentration.

Early effect: the rise of Ic due to base-width modulation.



Tek 575 Curve Tracer



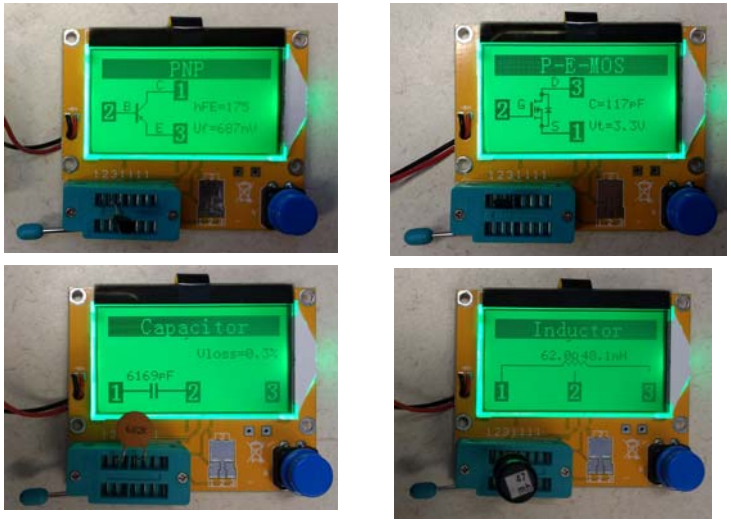
- Vertical axis: current
- Horizontal axis: voltage
- Voltage sweep: positive and negative with resistor current limit 0-20v; 0-200v!
- Input: fixed current steps (0.001-200ma); 240 steps
- Tests: diodes, BJT, MOSFETs
- Calibrate zero current step

Mcube

- Tests:
  - Diodes (forward drop)
  - BJT (type, beta)
  - MOSFET (type, V_{TH} and more)
- Auto terminal identification



RLC – BJT MOSFET Testor



BJT Configurations

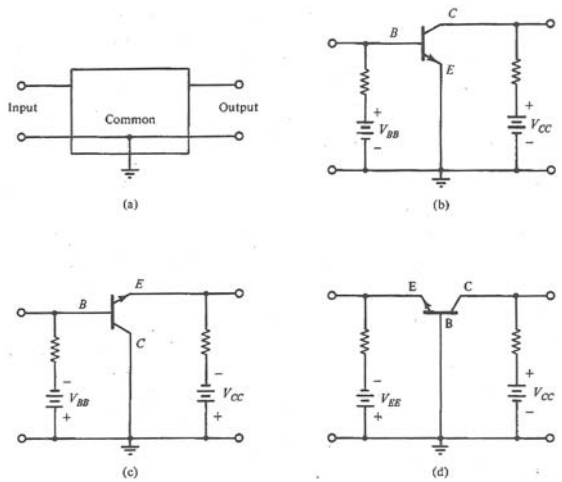
	Voltage Gain	Current Gain	Power Gain
Common Emitter	X	X	X
Common Collector		X	X
Common Base	X		X

Common emitter: hgh input impedance, for general amplification of voltage, current and power from low power, high impedance sources.

Common collector: aka "emitter follower" for high input impedance and current gain without voltage gain, as in an amplifier output stage.

Common base: low input impedance for low impedance sources, for high frequency response. Grounding the base short circuits the Miller capacitance from collector to base and makes possible much higher frequency response.

General Configuration

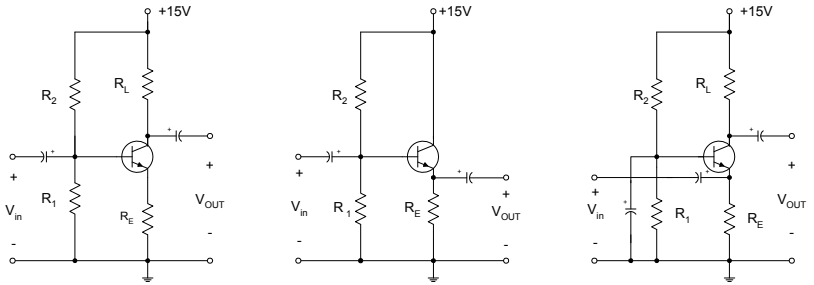


Common Emitter

Common Collector

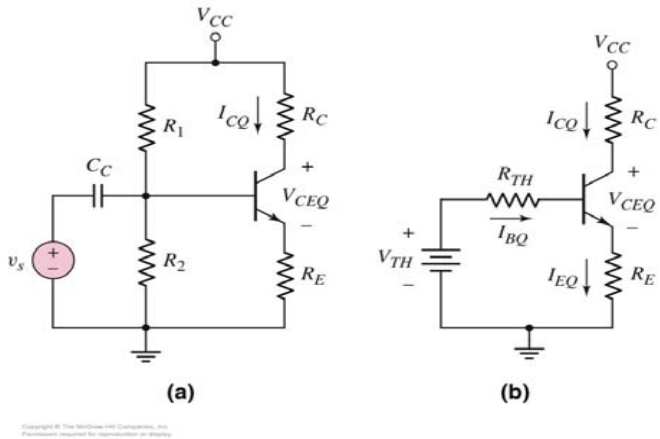
Common Base

Transistor Configurations



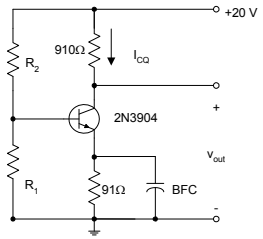
[a] Common Emitter Amplifier [b] Common Collector [Emitter Follower] Amplifier [c] Common Base Amplifier

Common Emitter Operation – Quiescent Point

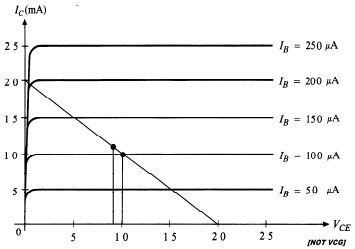


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Load Line – Operating Point

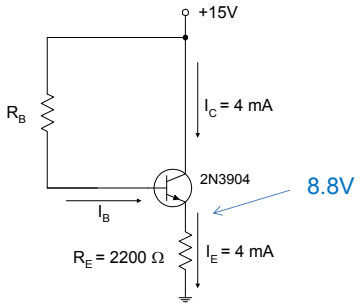


- Find V_{out} open circuit voltage: 20V
- Find I_{CQ} max = 20/(910 +91) = ~20ma
- Draw load line.



- For $R_E = 0$, just choose Q at ½ V_{CC} for maximum swing.
- For $R_E > 0$, set Q at ½ [$V_{CC} - V_{RE}$].
- For I_{CQ} = 10 mA, V_{RL} = 9.1V, V_{RE} = 0.91V, V_{CE} = 10V. For I_{CQ} = 10.5mA, V_{RL} = 9.6V, V_{RE} = 0.96V, V_{CE} = 9.5V

Transistor Bias Instability



$$\beta_F = 100, \qquad I_C = \beta_F I_B$$
$$I_E = (\beta_F + 1) I_B, \qquad I_E \approx I_C$$

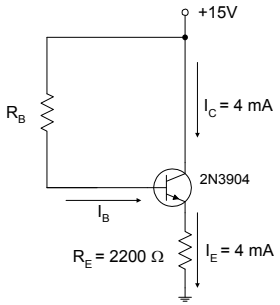
$$I_B R_B + 0.7V + I_C R_E = V_{CC}$$
$$I_B R_B + 0.7V + \beta_F I_B R_E = V_{CC}$$
$$I_B (R_B + \beta_F R_E) = V_{CC} - 0.7V$$

$$I_B = \frac{(V_{CC} - 0.7V)}{R_B + \beta_F R_E} \qquad (1)$$

$$I_C = \frac{\beta_F (V_{CC} - 0.7V)}{R_B + \beta_F R_E} \qquad (2)$$

$$R_B + \beta_F R_E = \frac{\beta_F (V_{CC} - 0.7V)}{I_C}$$
$$R_B + 100 \times 2200\Omega = \frac{100(15V - 0.7V)}{4mA}$$
$$R_B + 220k\Omega = \frac{1430}{4} \times 10^3 \Omega$$
$$R_B + 220k\Omega = 358k\Omega$$
$$R_B = 138k\Omega$$

Variation of Collector Current with β
One Resistor

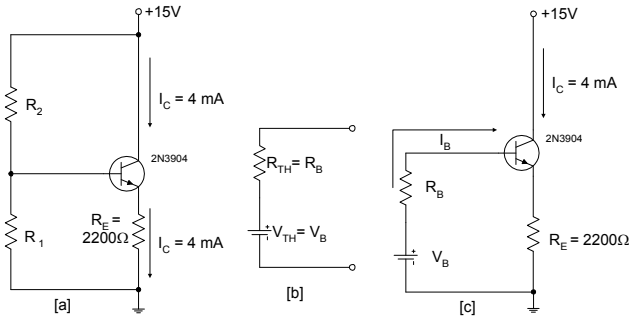


$$I_C = \frac{\beta_F (V_{CC} - 0.7V)}{R_B + \beta_F R_E} \qquad (2)$$

Variation of Collector Current with Beta

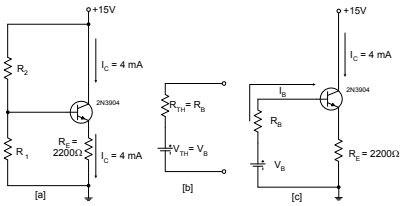
I_C	β_F
2.9 mA	50
4.0 mA	100
5.0 mA	200
5.4 mA	300
ΔI_C=2.5 mA	

Two Resistor Biasing



$$V_B = \frac{R_1}{R_1 + R_2} \times V_{cc} \quad (3) \qquad R_B = R_1 // R_2 = \frac{R_1 R_2}{R_1 + R_2} \quad (4)$$

Two Resistor Biasing



$$V_B - I_B R_B - 0.7V - I_C R_E = 0$$
$$V_B = I_B R_B + 0.7V + \beta_F I_B R_E$$
$$V_B - 0.7V = I_B R_B + \beta_F I_B R_E = I_B\left(R_B + \beta_F R_E\right)$$

$$I_B = \frac{\left(V_B - 0.7V\right)}{R_B + \beta_F R_E} \quad (5)$$

$$I_C = \frac{\beta_F\left(V_B - 0.7V\right)}{R_B + \beta_F R_E} \quad (6)$$

Assume R_B = 22kΩ,

βR$_E$ = 220kΩ and ignore R_B

$$4mA \times \left(22k\Omega + 220k\Omega\right) = 100\left(V_B - 0.7V\right)$$
$$4mA \times 242k\Omega = 100V_B - 70$$
$$968 + 70 = 100V_B$$
$$V_B = 10.4V$$

Two Resistor Biasing

Given V_B= 10.4 V and R_B= 22kΩ, we can now solve equations (3) and (4) for R_1 and R_2.

$$\frac{R_1 R_2}{R_1 + R_2} = R_B = 22k\Omega$$
$$\frac{R_1 \times 0.45R_1}{R_1 + 0.45R_1} = 22k\Omega$$
$$\frac{0.45R_1^2}{1.45R_1} = 22k\Omega$$
$$0.310R_1 = 22k\Omega$$
$$R_1 = 70.9k\Omega \quad use \quad 68k\Omega$$
$$R_2 = 0.45R_1 = 0.45 \times 70.9k\Omega = 31.9k\Omega \quad use \quad 33k\Omega$$

$$V_B = \frac{R_1}{R_1 + R_2} \times V_{CC}$$
$$R_1 + R_2 = R_1\left(\frac{V_{CC}}{V_B}\right) = R_1\left(\frac{15V}{10.4V}\right) = 1.45R_1$$
$$R_1 + R_2 = 1.45R_1$$
$$0.45R_1 = R_2$$

Variation of Collector Current with β
Two Resistor Biasing

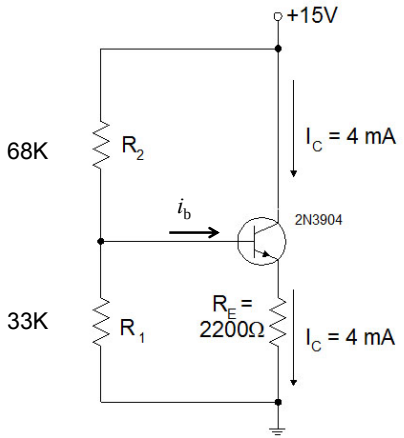
$$I_C = \frac{\beta_F\left(V_B - 0.7V\right)}{R_B + \beta_F R_E} \quad (6)$$

$$I_C = \frac{\beta_F\left(10.4 - 0.7V\right)}{22k\Omega + \beta_F 2200\Omega}$$

Variation of Collector Current with Beta

Two Resistor	One Resistor	
I_C	I_C	β_F
3.7 mA	2.9 mA	50
4.0 mA	4.0 mA	100
4.2 mA	5.0 mA	200
4.3 mA	5.4 mA	300
ΔI_C=0.6 mA	ΔI_C=2.5 mA	

Base Current – Resistor Divider

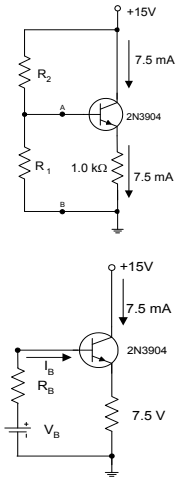


I_C	β_F
3.7 mA	50
4.0 mA	100
4.2 mA	200
4.3 mA	300
ΔI_C=0.6 mA	

Make i_b small compared to the current through R_2

See handout: Transistor bias stability

Common Collector – Emitter Follower Biasing



- B = 100, i_B = 7.5ma/100 =- 75µa
- Using Thevenin equivalent,

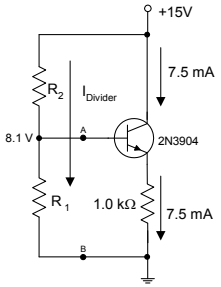
$R_B = R_1 \| R_2$, $V_B = 15\left(\frac{R_1}{R_1 + R_2}\right)$

$V_B = I_B R_B + 0.6V + 7.5V$
$V_B = [75\ \mu A \times 10k] + 0.6V + 7.5V$
$V_B = 750\ mV + 0.6V + 7.5V$
$V_B = 8.9V$

$[15\ R_1] \div [R_1 + R_2] = 8.9V$
$15\ R_1 = 8.9 \times [R_1 + R_2]$
$[15-8.9]\ R_1 = 8.9\ R_2$
$R_1 = 1.44\ R_2$
$[R_1 \times R_2] \div [R_1 + R_2] = 10\ k\Omega$

$[1.44R_2 \times R_2] \div [1.44\ R_2 + R_2] = 10k\Omega$
$R_2 = 16.9\ k\Omega$ (use 16 kΩ)
$R_1 = 1.44\ R_2 = 24.4\ k\Omega$ (use 24 kΩ)

Common Collector – Emitter Follower Biasing



- With R1 = 24kΩ, R2 = 16 kΩ, the current through the voltage divider is 15 ÷ [40 kΩ] = 375 µA.
- The 75 µA base current is 20% of 375 µA.

- With R1 = 2 kΩ, will need a divider current that is ~ 4.1 mA. (75 µA is only ~2% of 4.1 mA, which is negligible)
- The voltage drop across R2 will be [15 V – 8.1 V] = 6.9 V; R2 = 1.7 kΩ
- But input impedance will be low = ~890Ω
- Use bootstrapping configuration

= 24.4 kΩ (use 24 kΩ)

Bootstrapping – Higher Input Impedance

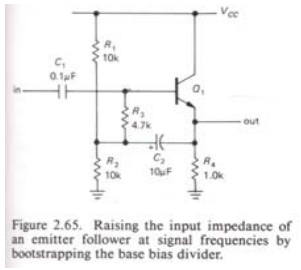


Figure 2.65. Raising the input impedance of an emitter follower at signal frequencies by bootstrapping the base bias divider.

Horowitz and Hill Figure 2.65

The base is connected to the emitter through with R_3 and C_2. At signal frequency, C_2 is a short so both ends of R_3 are at the same voltage – so no current flows. Therefore R_1 and R_2 cannot load the input. So R_3 appears to be very high.

In real life, there is a small AC voltage across R_3. The AC current through R_3 is 0.006 ÷ 4.7kΩ = 1.1 µA.

Result: "stiff" biasing with high input resistance at signal frequency.

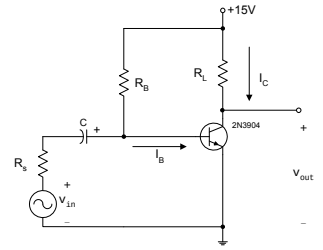
"Our treatment of bipolar transistors is going to be quite different from that of many other books. It is a common practice to use the h-parameter (hybrid pi) model and equivalent circuit. In our opinion that is unnecessarily complicated and unintuitive. . . . you also have the tendency to lose sight of which parameters of transistors behavior you can count on and more important, which ones can vary over large ranges."

The Art of Electronics, Horowitz & Hill 3rd edition page 71

Commom Emitter – Hybrid π

TRANSISTOR AMPLIFIER CONFIGURATIONS WITH HYBRID-π EQUIVALENT CIRCUITS

COMMON EMITTER AMPLIFER

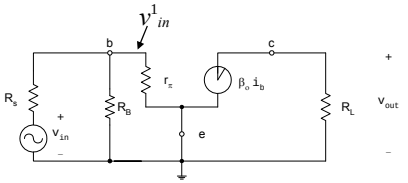


$$\beta_0 = g_m r_\pi$$

$$g_m = \frac{I_{CQ}}{V_{TH}}$$

$$r_0 = \frac{V_A}{I_{CQ}}$$

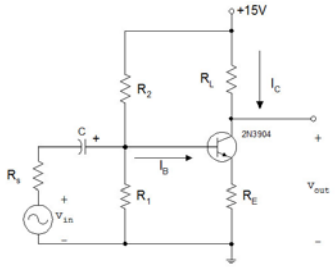
Early Voltage



$$A_v = \frac{v^1_{out}}{v^1_{in}} = \frac{-\beta_o i_b R_L}{i_b[r_\pi]} = \frac{-\beta_o R_L}{r_\pi}$$

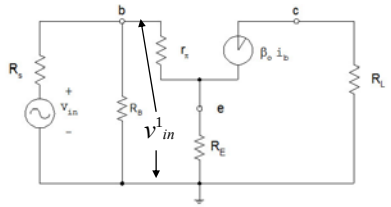
$$then\ A_v = \frac{-\beta_o R_L}{\frac{\beta_o}{g_m}} = -g_m R_L$$

Common Emitter with Emitter Degeneration



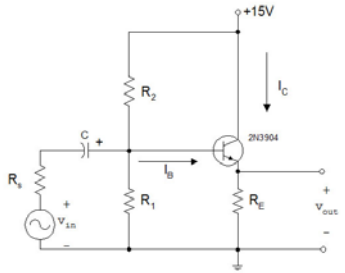
$$A_v = \frac{v^1_{out}}{v^1_{in}} = \frac{-\beta_o i_b R_L}{i_b[r_\pi + (\beta_o + 1)R_E]} = \frac{-\beta_o R_L}{r_\pi + (\beta_o + 1)R_E};$$

$$if\ \ r_\pi << (\beta_o + 1)R_E; \qquad then\ A_v \approx -R_L / R_E$$



- Input resistance $(\beta+1)R_E$
- Voltage gain reduced by $(1+g_m R_E)$
- Voltage gain less dependent on β (linearity)

Common Collector (Emitter Follower)

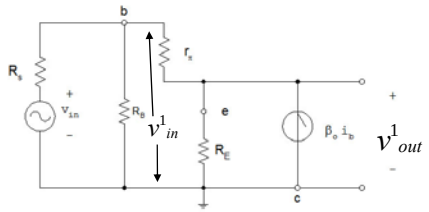


$$\beta_0 = g_m r_\pi$$

$$g_m = \frac{I_{CQ}}{V_{TH}} \qquad V_{TH} = 26mv$$

$$A_v = \frac{v^1_{out}}{v^1_{in}} = \frac{(\beta_o + 1)i_b R_E}{i_b[R'_s + r_\pi + (\beta_o + 1)R_E]} = \frac{(\beta_o + 1)\ R_E}{R'_s + r_\pi + (\beta_o + 1)R_E};$$

$$if\ \ r_\pi << (\beta_o + 1)R_E; \qquad then\ A_v \approx 1$$



- Buffer with unity gain
- High input resistance driving low output resistance (current gain).

Low Frequency Hybrid-π Equation Chart

Characteristic	Common Emitter	CE with R_E	CC [E. Follower]	Common Base
Voltage Gain [if $r_o >> R_L$]	$A_v = -g_m R_L$	$A_v \approx -\frac{R_L}{R_E}$	$A_v \approx 1$	$A_v = \frac{\beta_o R_L}{r_\pi // R_E + (\beta_o + 1)R_s}$
Current Gain	β_o	β_o	β_o+1	$\frac{\beta_o}{\beta_o + 1}$
Input Impedance	$r_\pi // R_B$	$[r_\pi + (\beta_o + 1)R_E] // R_B$	$[r_\pi + (\beta_o + 1)R_E] // R_B$	$\frac{r_\pi}{\beta_o + 1}$
Output Impedance	R_L [if $r_o >> R_L$]	R_L [if $r_o >> R_L$]	$\left[\frac{(r_\pi + R_s // R_B)}{\beta_o + 1}\right] // R_E$	R_L [if $r_o >> R_L$]
Phase Reversal?	Yes	Yes	No	No
	High gain applications Moderate input resistance High output resistance		Unity gain, low output resistance High input resist.	High gain, better high frequency response Low input resistance

Hybrid-π Parameters

$$g_m = \left(\frac{q}{kT}\right)|I_C|$$

$$\beta_0 = h_{fe} \ \ (datasheet)$$

$$C_\mu = C_{ob} \ \ (datasheet)$$

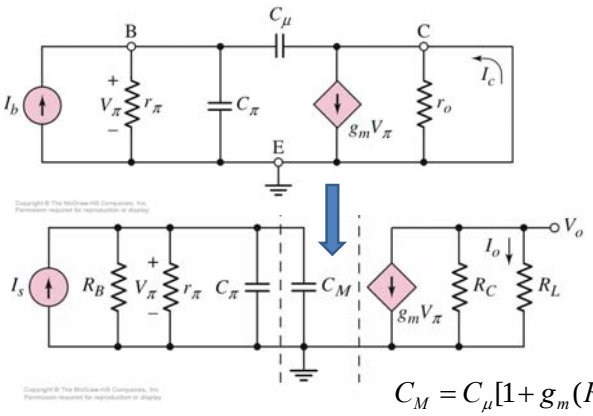
$$\frac{g_m}{2\pi(C_\pi + C_\mu)} = f_T \ \ (transit \ \ frequency \ \ datasheet)$$

$$C_\pi = \frac{g_m}{2\pi f_T r\pi} - C\mu$$

$$r_x \ (low \ frequency) : datasheet \ or \ estimate \ 50 - 100\Omega$$

$$(high \ \ frequency) : estimate \approx 25\Omega$$

Miller Effect* – Common Emitter



$$C_M = C_\mu[1 + g_m(R_C \| R_L)]$$

* Agarwal & Lang Foundations of Analog & Digital Electronics Circuits p 861

h_{fe} and High Frequency Limits

Small signal current gain versus frequency, h_{fe}, of a BJT biased in a common emitter configuration:

$$i_b = \frac{v_{be}}{r_\pi} + v_{be} j\omega C \qquad h_{fe} = \frac{g_m v_{be}}{i_b} = \frac{g_m r_\pi}{1 + j\omega r_\pi C} = \frac{\beta}{1 + j\omega r_\pi C}$$

For h_{fe} = 1 = f_T, (transit frequency) $h_T = \frac{g_m}{2\pi f_t C}$ *where* $C = (c_\pi + c_\mu)$

For 2N3904*, I_C =1ma, V_{CE}=10V , c_π=25pF, c_μ=2pF

$$f_T = \frac{0.04mho}{2\pi 27\,pF} = 240MHz$$

$$for\ a\ gain\ of\ g_m R_L = 100 \quad f_h = \frac{1}{2\pi\, r_\pi g_m R_L c_\mu} = \frac{1}{2\pi\ 2.5K\Omega(100)2\,pF} = 320kHz$$

Miller effect reduces high frequency limit!

*Lundberg, Kent: Become One with the Transistor p29