

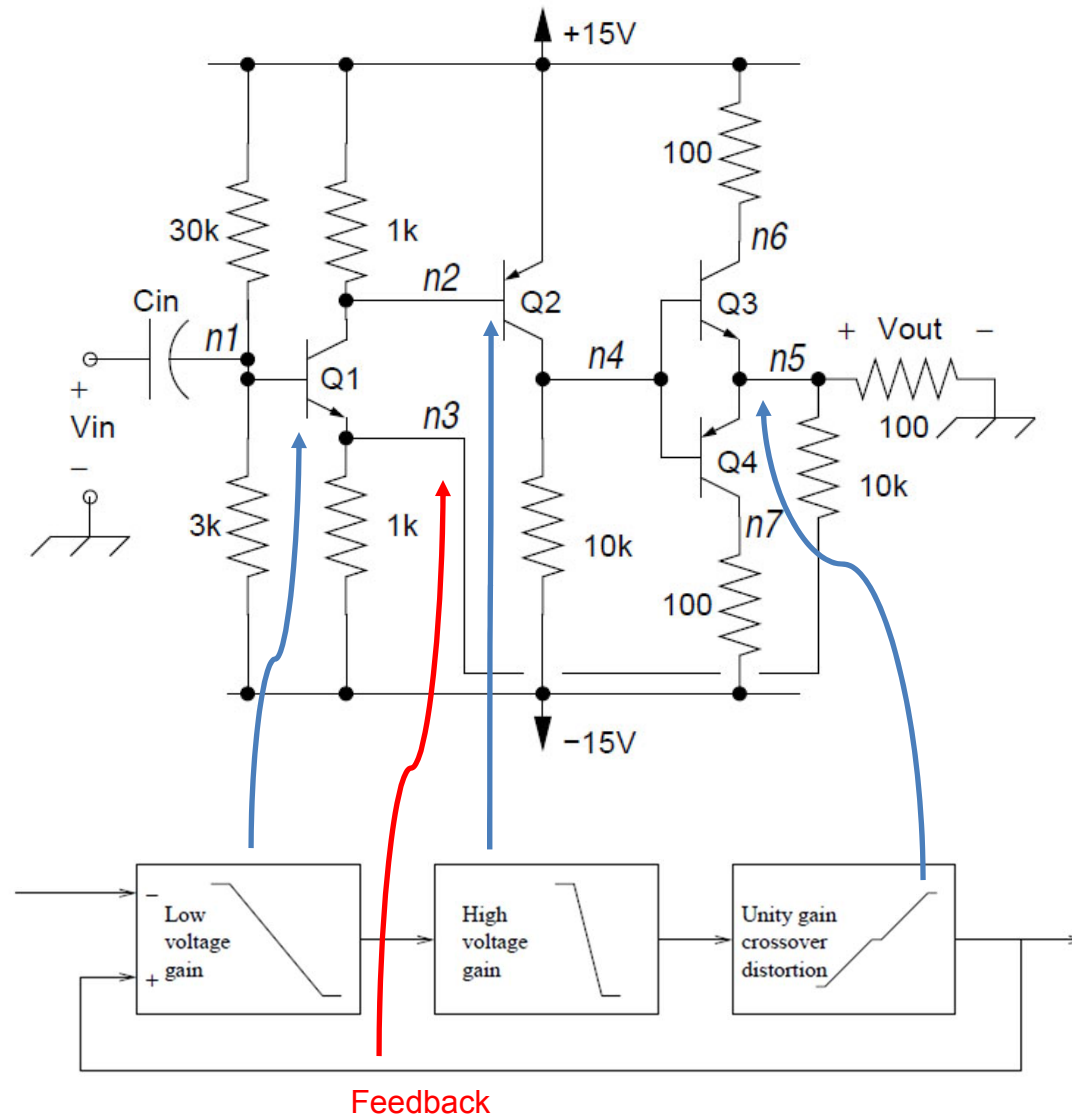


- Crossover Distortion
- FETS
- Spec sheets
- Configurations
- Applications

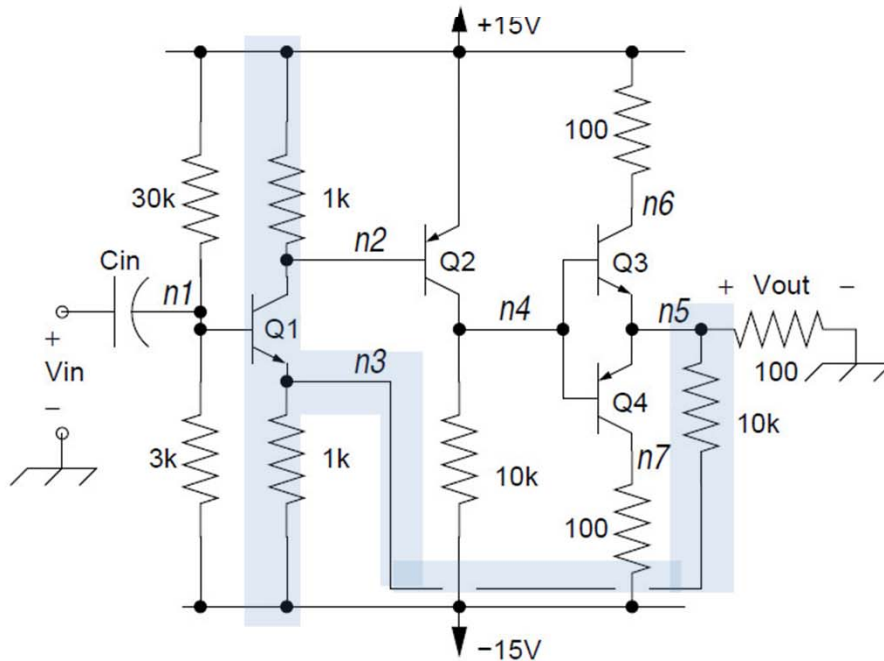
Acknowledgements:

Neamen, Donald: Microelectronics Circuit Analysis and Design, 3rd Edition

Three Stage Amplifier – Crossover Distortion Hole



Crossover Distortion Analysis



The emitter follows the base by 0.6v,
 v_e incrementally follows v_b

The emitter current
$$i_E = \frac{v_E - (-15)}{1000} + \frac{v_E - v_{OUT}}{10000}$$

The collector voltage, assuming large β ($i_E = i_C$)
 is $v_C = 15 - 1000i_C$

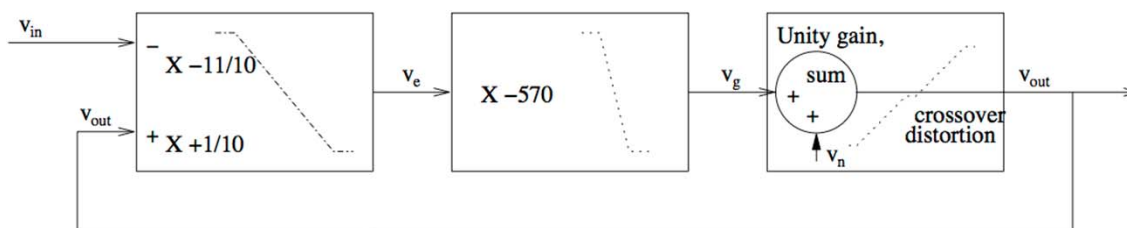
Then
$$\Delta v_C = -\frac{11}{10} \Delta v_B + \frac{1}{10} v_{OUT}$$

Now we have enough information, i.e. equations
 to put everything together.

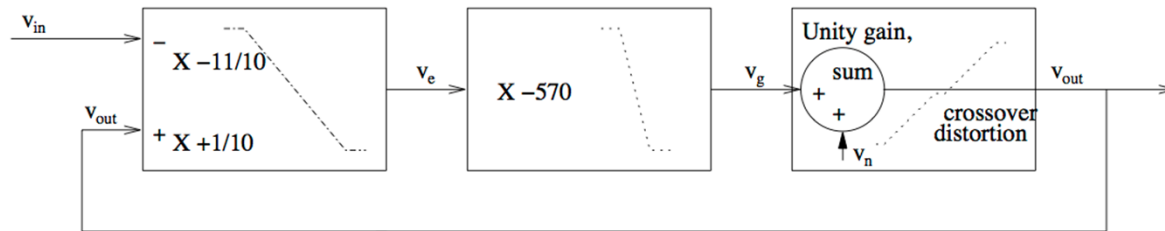
$$v_{OUT} = -570 \left(-\frac{11}{10} v_{IN} + \frac{1}{10} v_{OUT} \right)$$

$$v_{OUT} \left(1 + \frac{570}{10} \right) = 570 \left(\frac{11}{10} \right) v_{IN}$$

$$\frac{v_{OUT}}{v_{IN}} = \frac{570 \left(\frac{11}{10} \right)}{1 + \frac{570}{10}} \approx 10.8$$



Crossover Distortion Analysis



$$v_e = -\frac{11}{10}v_{in} + \frac{1}{10}v_{out}$$

$$v_g = -570v_e$$

$$v_{out} = -570\left(-\frac{11}{10}v_{in} + \frac{1}{10}v_{out}\right) + v_n$$

$$v_{out} = \frac{-570 \frac{-11}{10}}{1 + 570 \frac{1}{10}}v_{in} + \frac{1}{1 + 570 \frac{1}{10}}v_n \approx 10.81v_{in} + 0.0172v_n$$

- The distortion 0.6v in each direction or 1.2v total resulting in a hole that is:

$$0.0172 * 1.2 \sim 0.02v$$

- Increasing open loop gain will reduce the crossover distortion.

BJT - FET

Bipolar Junction Transistor

- Three terminal device
- Collector current controlled by base current $i_b = f(V_{be})$
- Think as current amplifier
- NPN and PNP

Field Effect Transistor

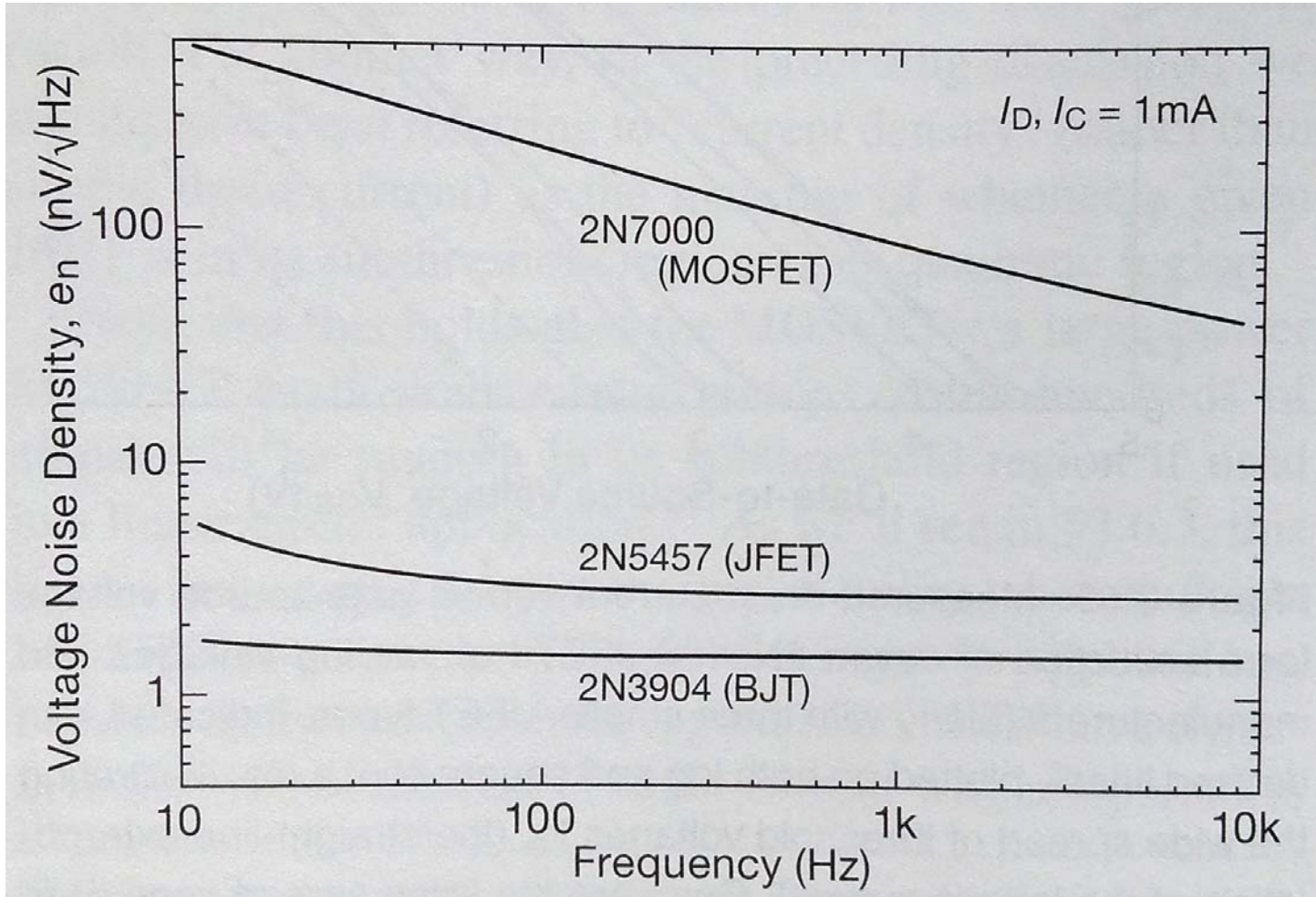
- Three terminal device
- Channel conduction controlled by electric field
- No forward biased junction i.e. no current
- JFETs, MOSFETs
- Depletion mode, enhancement mode

BJT - JFETS - MOSFETS

	BJT	JFET	MOSFET
Circa	1960	1970	1980
Gm/I (signal gain)	Best	Better	Good
Isolation		PN Junction	Metal Oxide*
ESD	Low	Moderate	Very sensitive
Control	Current	Voltage	Voltage
Power	YES	No	Yes

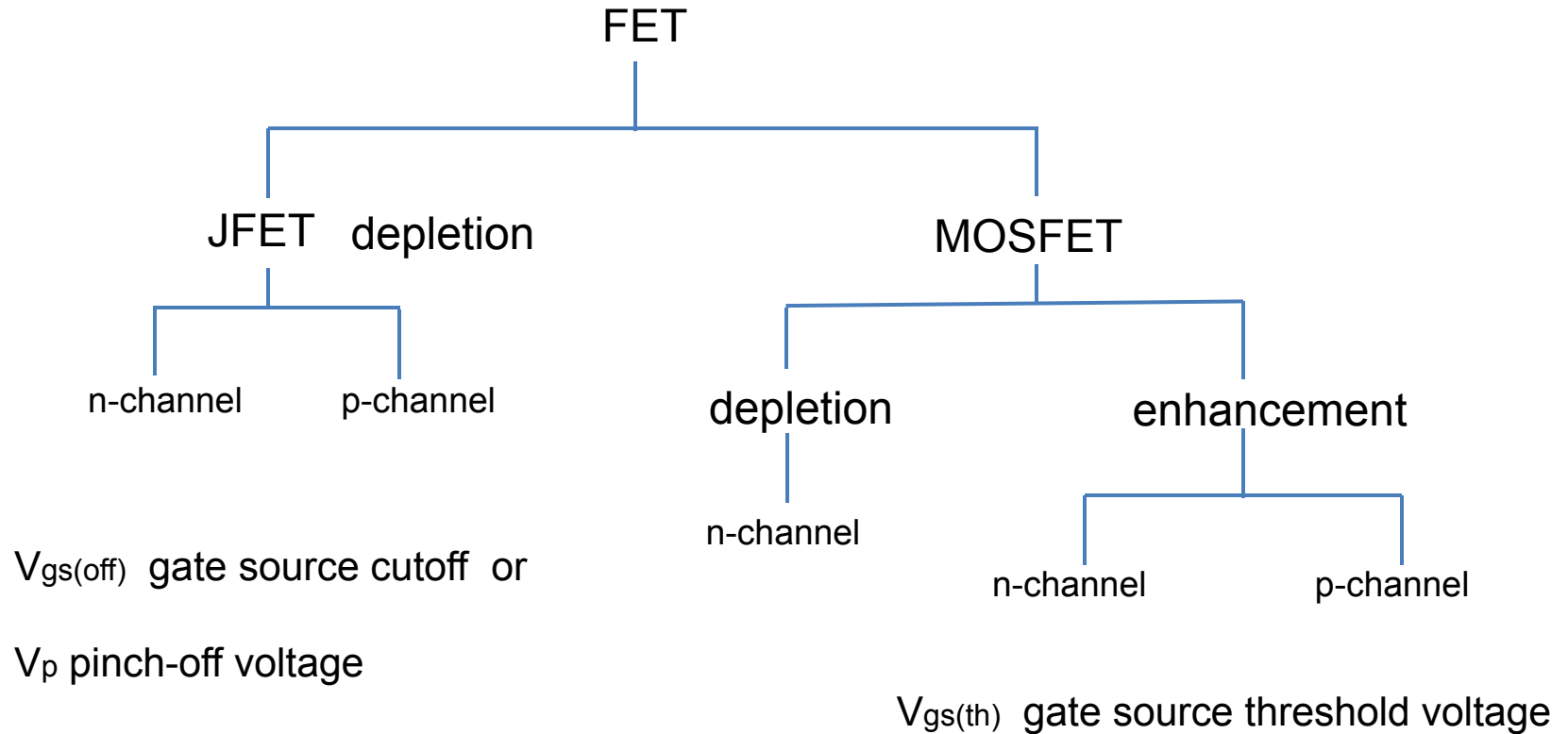
*silicon dioxide

Voltage Noise *

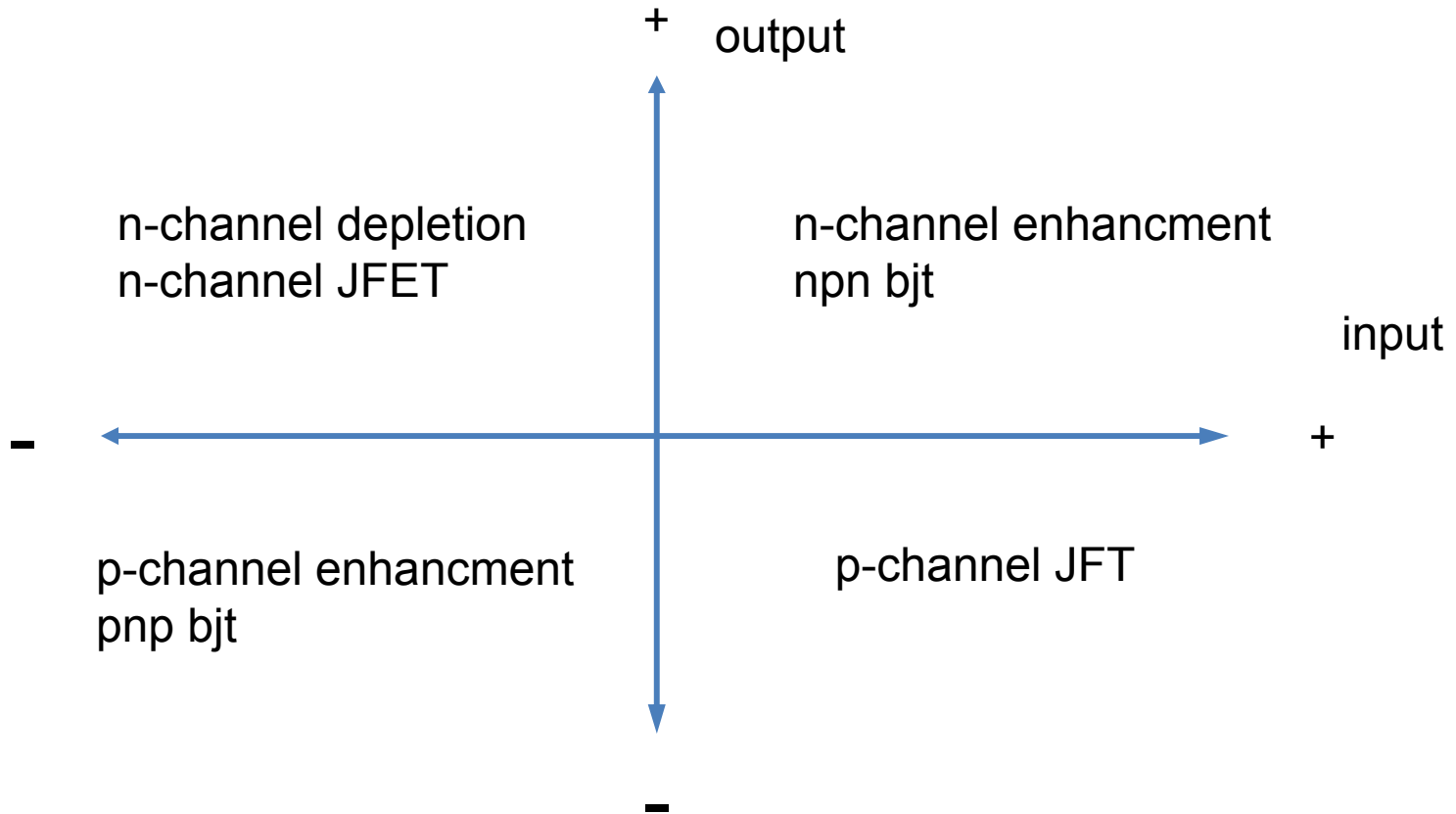


* Horowitz & Hill, Art of Electronics 3rd Edition p 170

FET Family Tree



Transistor Polarity Mapping*



* Horwitz & Hill, the Art of Electronics, 3rd Edition

MOSFET & JFETS

- **MOSFETS**

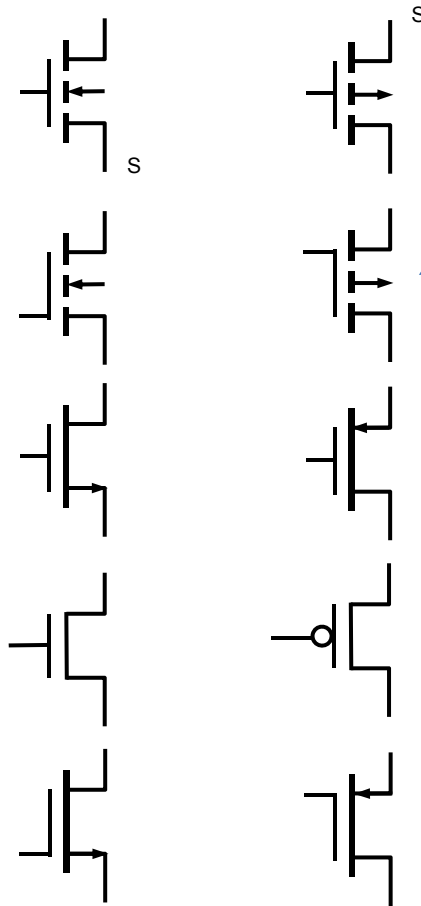
- Much more finicky difficult process (to make) than JFET's.
- Good news: Extremely high input impedance. Zero input current.
- Bad news: Easily blown up by ESD on the gate. Add protection circuit and input bias current becomes at best comparable to JFET's.
- Good news: Essentially infinitely fast. If you change the gate voltage, the device will respond instantaneously! Essentially always in static equilibrium.
- Bad news: It can be *really* hard to change the gate voltage quickly! (especially power devices – BIG BIG capacitor)
- Much better power devices than JFET's. (There were briefly power JFET's as output devices in audio amps. Too many blew up.)
- And you can't make digital VLSI out of JFET's.

MOSFET vs JFETS

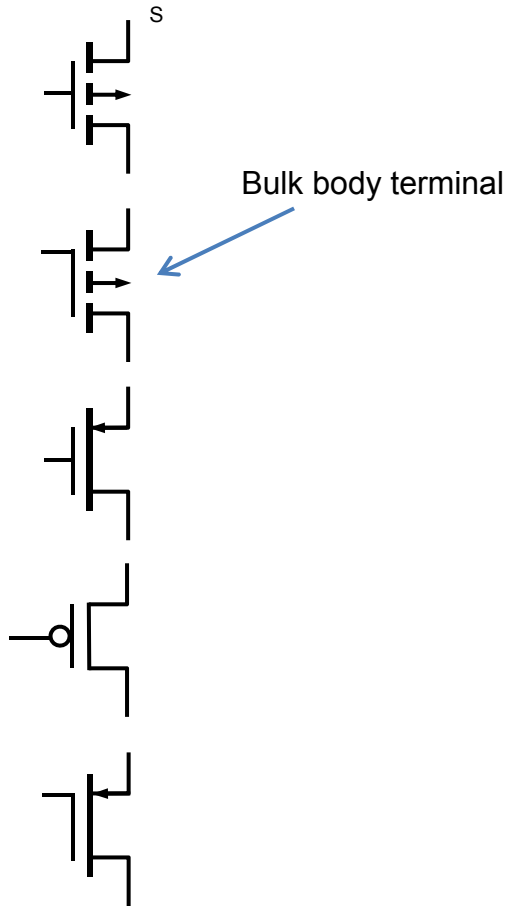
- JFET's

- Very simple manufacturing process like BJT's. Much cheaper than (discrete) MOSFET's. Quieter than MOSFET's.
- Low input bias current – like back biased diode. As low as 10pA.
- But note this doubles every 6 deg C! At high temps a JFET op amp can have more input current than some bipolar op amps!
- Used in microphones, hearing aids and other high impedance sources (electret microphones have very high output impedance) because of low noise and ruggedness compared to MOSFET's.
- Fast. Used on many high speed scope probes. Was major advance in bias current and speed over bipolar-input op amps. See data sheets of (JFET input) LF356 series and compare to then bipolars.
- Downside is input capacitance can't be as low as some BJT's.
- Wide spread in threshold voltage and zero- V_{gs} current. Sometimes requires sorting and selecting for a given circuit.

MOSFET Symbols

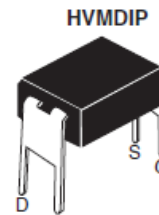


N-channel

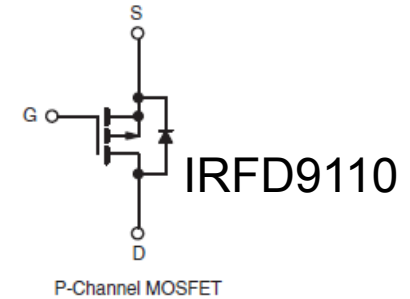


P-channel

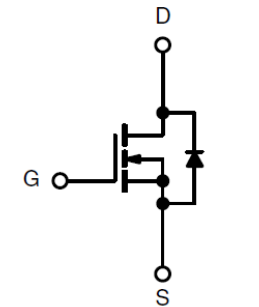
PRODUCT SUMMARY		
V_{DS} (V)	- 100	
$R_{DS(on)}$ (Ω)	$V_{GS} = - 10$ V	1.2
Q_g (Max.) (nC)	8.7	
Q_{gs} (nC)	2.2	
Q_{gd} (nC)	4.1	
Configuration	Single	



2N7000

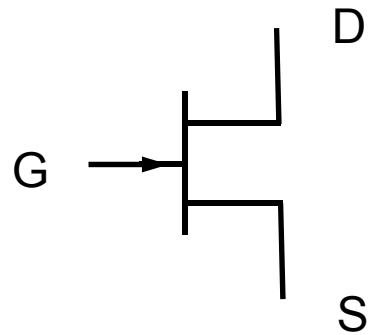


P-Channel MOSFET

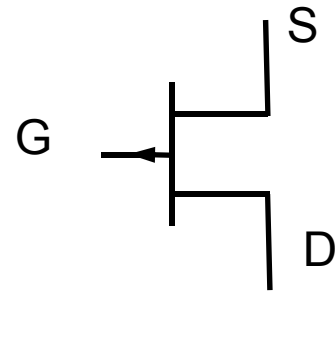


N-Channel MOSFET

JFET: Junction FET Symbol

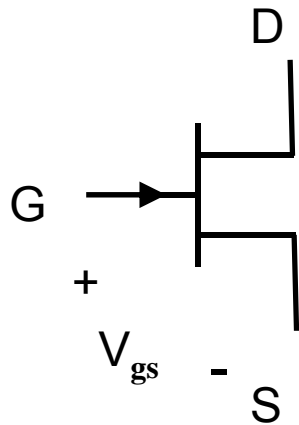


N channel JFET



P channel JFET

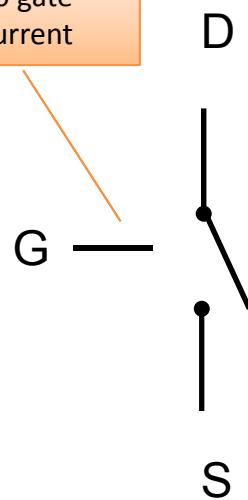
Simple Model of MOSFET



MOSFET made VSLI
(microprocessors and
memories) possible.

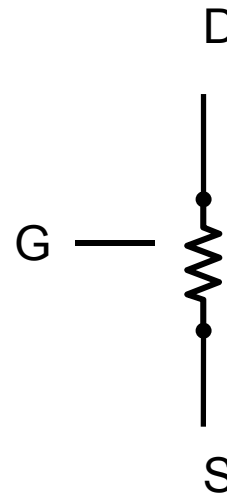
Very high input resistance
Voltage controlled device
~25 V max operating

~0 gate
current



off state

$$V_{gs} < V_t$$



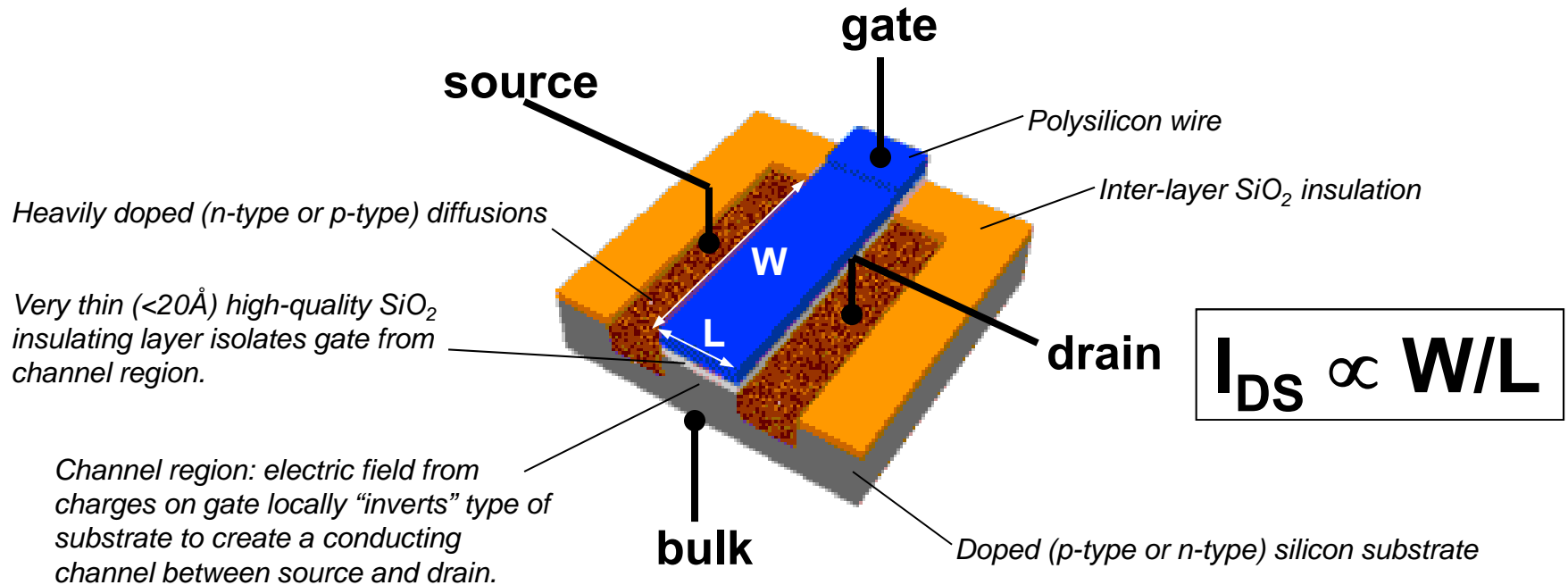
on state

$$V_{gs} \geq V_t$$

2N7000
 $R_{on} 7.5 \Omega$
@50ma

IRFD9110
 $R_{on} 1.2 \Omega$
@0.42A

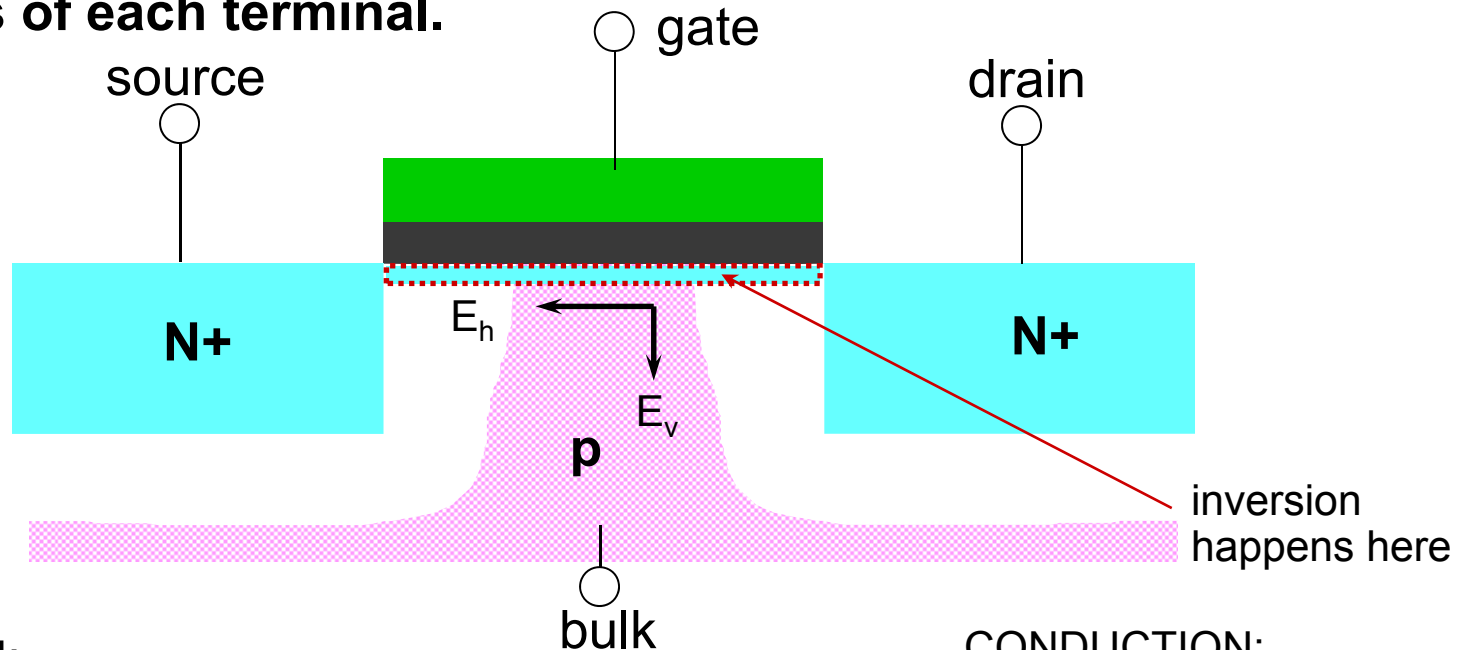
MOSFETS: Gain & non-linearity



MOSFETs (metal-oxide-semiconductor field-effect transistors) are four-terminal voltage-controlled switches. Current flows between the diffusion terminals if the voltage on the gate terminal is large enough to create a conducting “channel”, otherwise the mosfet is off and the diffusion terminals are not connected.

FETs as switches

The four terminals of a Field Effect Transistor (gate, source, drain and bulk) connect to conductors that generate a complicated set of electric fields in the channel region which depend on the relative voltages of each terminal.



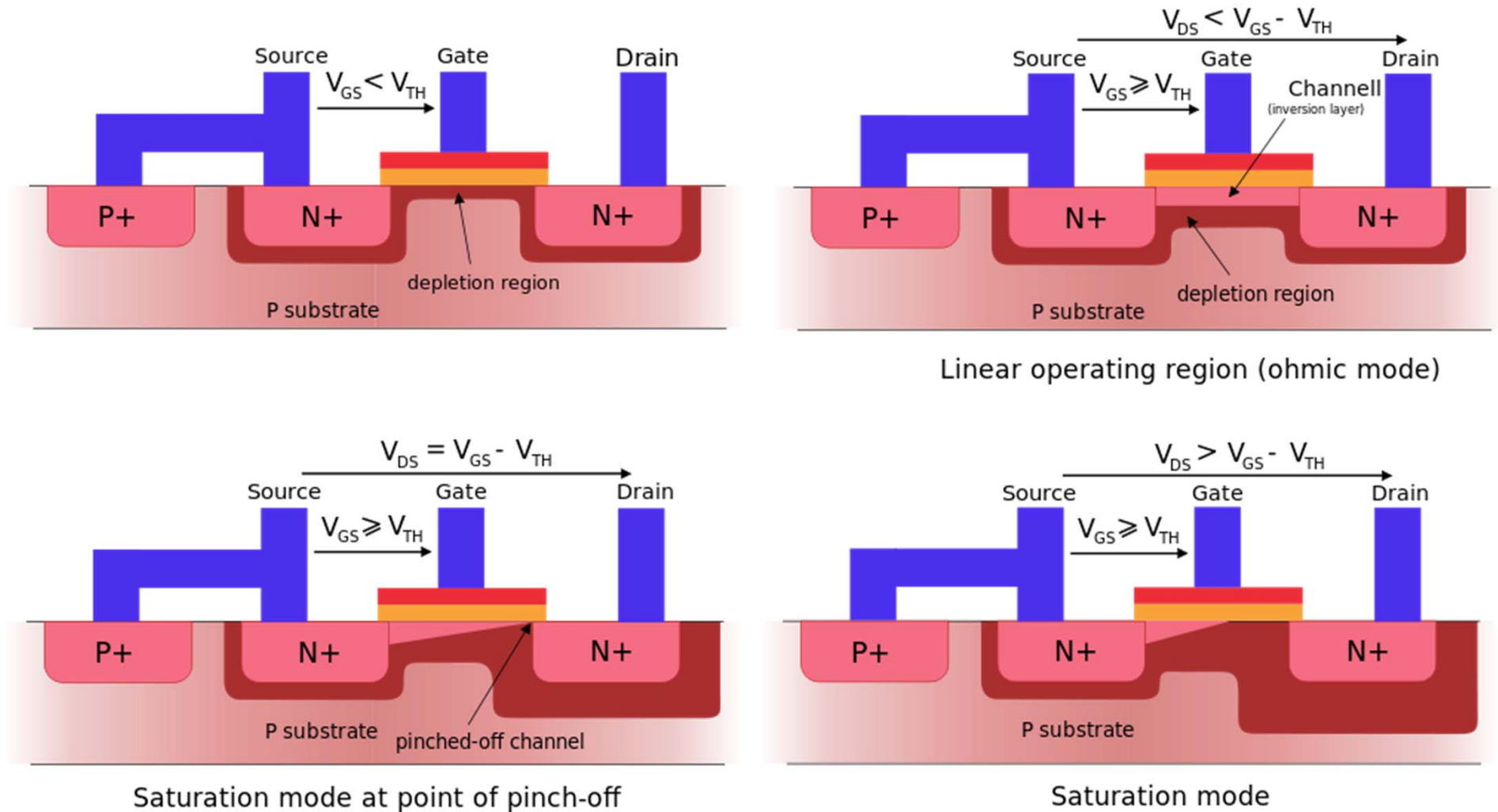
INVERSION:

A sufficiently strong vertical field will attract enough electrons to the surface to create a conducting n-type channel between the source and drain. The gate voltage when the channel first forms is called the *threshold voltage* -- the mosfet switch goes from "off" to "on".

CONDUCTION:

If a channel exists, a horizontal field will cause a drift current from the drain to the source.

Four states of MOSFET for different V_{GS} and V_{DS}



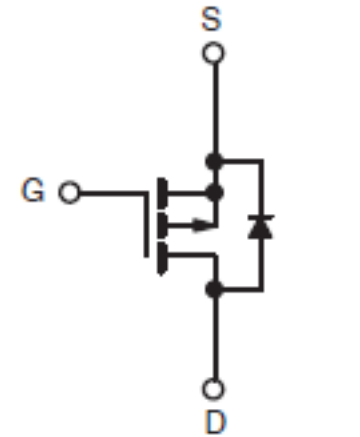
Olivier Deleage and Peter Scott (CC BY-SA 3.0)

What's the difference between the drain and the source?

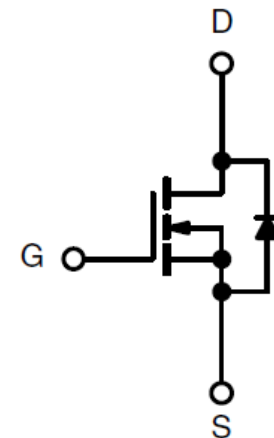
MOSFET's can be symmetrical and drain and source interchangeable. Especially inside IC's.

But discrete devices (with few exceptions) have input protection networks on the gate to protect against ESD. Also, the substrate must connect somewhere.

Once the input protection clamping and the substrate are connected to a terminal, that must be the source.



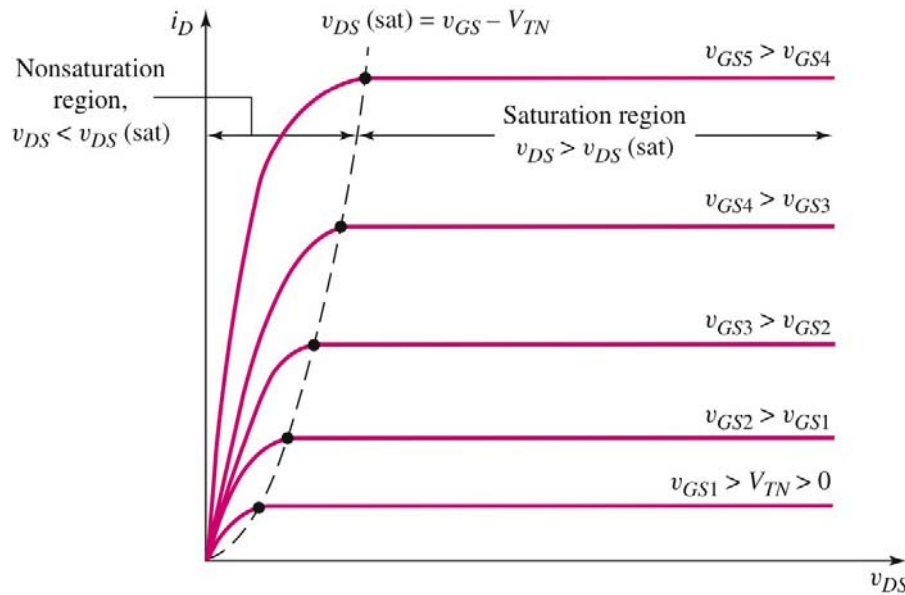
P-Channel MOSFET



N-Channel MOSFET

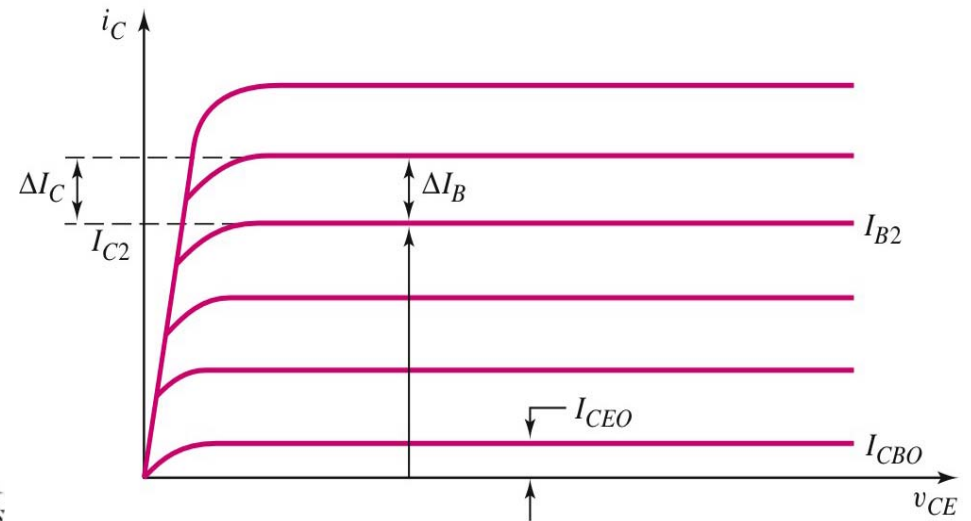
Classic “ideal” MOSFET characteristics –

Flat curves in saturation region assume “long” channel



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MOSFET



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BJT

“ideal” MOSFET curves continued

Triode mode, or “linear” mode, or ohmic region.

$$I_D = \mu_n C_{ox} \frac{W}{L} \left((V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

Saturation or active mode.

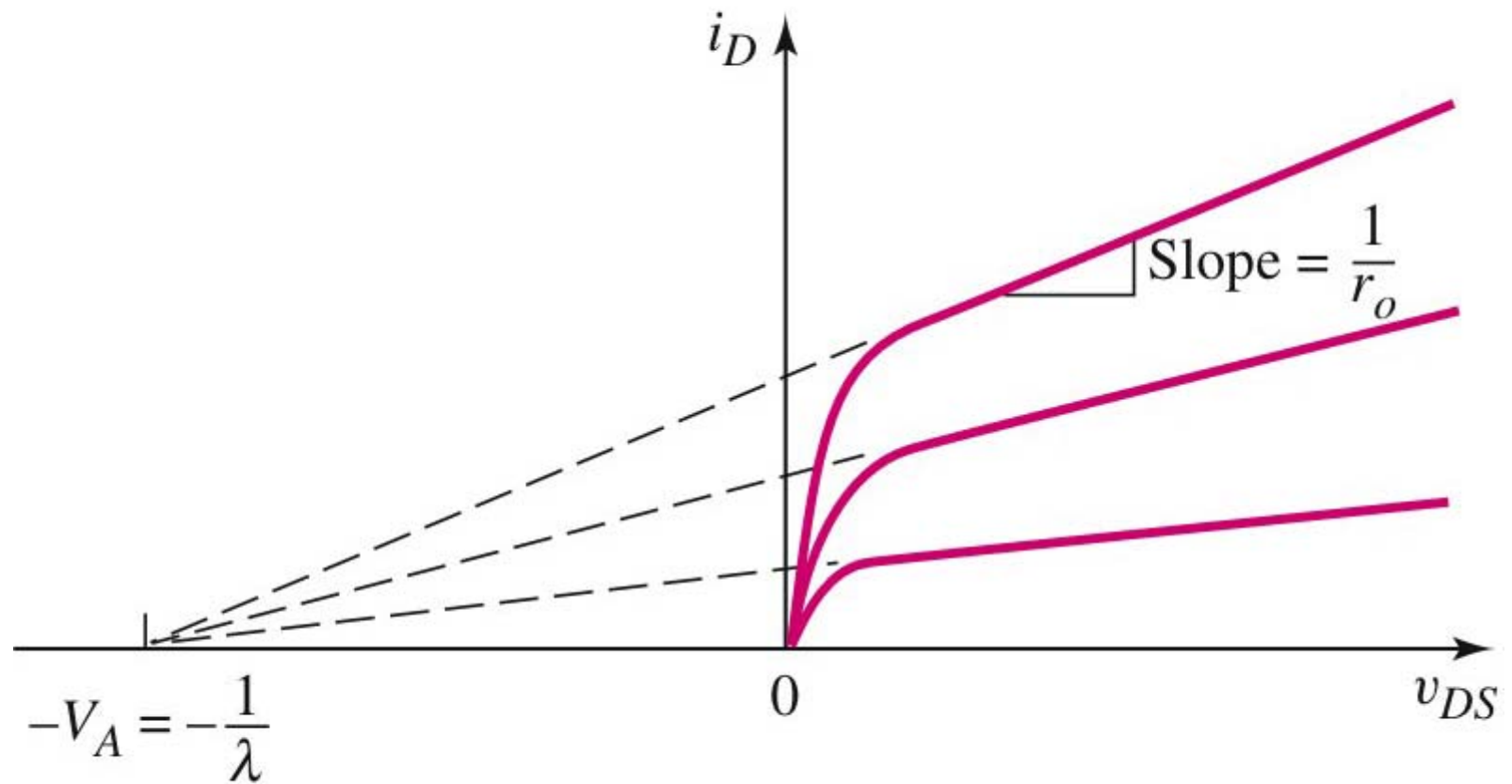
K_n = transconductance parameter

$$I_D = \frac{\mu_n C_{ox} W}{2 L} (V_{GS} - V_{th})^2 (1 + \lambda(V_{DS} - V_{DSsat}))$$

As the channel length becomes short, these equations become inaccurate. At the channel ends, source and drain regions causing “fringing” effects and distort the electric fields from the “ideal” case used to derive above eq’s.

For analog design, long-channel MOSFET’s can offer extremely high output Impedance, making excellent “stiff” current sources. Minimum geometry transistors used in digital VLSI do not have such flat curves.

Channel Length Modulation: Early Voltage

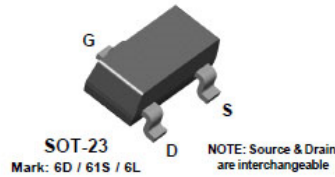
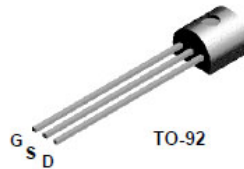


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2N5457
2N5458
2N5459

MMBF5457
MMBF5458
MMBF5459



N-Channel General Purpose Amplifier

This device is a low level audio amplifier and switching transistors, and can be used for analog switching applications. Sourced from Process 55.

Absolute Maximum Ratings* TA = 25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_{DG}	Drain-Gate Voltage	25	V
V_{GS}	Gate-Source Voltage	- 25	V
I_{GF}	Forward Gate Current	10	mA
T_J, T_{stg}	Operating and Storage Junction Temperature Range	-55 to +150	°C

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

NOTES:

- 1) These ratings are based on a maximum junction temperature of 150 degrees C.
- 2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

Thermal Characteristics TA = 25°C unless otherwise noted

Symbol	Characteristic	Max		Units
		2N5457-5459	*MMBF5457-5459	
P_D	Total Device Dissipation	625	350	mW
	Derate above 25°C	5.0	2.8	mW/°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	125		°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	357	556	°C/W

*

2N5457 / 5458 / 5459 / MMBF5457 / 5458 / 5459

JFET p-channel

N-Channel General Purpose Amplifier (continued)

Electrical Characteristics

TA = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
$V_{(BR)GSS}$	Gate-Source Breakdown Voltage	$I_G = 10 \mu A, V_{DS} = 0$	-25			V
I_{GSS}	Gate Reverse Current	$V_{GS} = -15 V, V_{DS} = 0$ $V_{GS} = -15 V, V_{DS} = 0, T_A = 100^\circ C$			-1.0 -200	nA nA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 15 V, I_D = 10 nA$	5457 5458 5459	-0.5 -1.0 -2.0	-6.0 -7.0 -8.0	V V V
V_{GS}	Gate-Source Voltage	$V_{DS} = 15 V, I_D = 100 \mu A$ $V_{DS} = 15 V, I_D = 200 \mu A$ $V_{DS} = 15 V, I_D = 400 \mu A$	5457 5458 5459	-2.5 -3.5 -4.5		V V V

ON CHARACTERISTICS

I_{DSS}	Zero-Gate Voltage Drain Current*	$V_{DS} = 15 V, V_{GS} = 0$	5457 5458 5459	1.0 2.0 4.0	3.0 6.0 9.0	5.0 9.0 16	mA mA mA
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SMALL SIGNAL CHARACTERISTICS

g_{fs}	Forward Transfer Conductance*	$V_{DS} = 15 V, V_{GS} = 0, f = 1.0 kHz$	5457 5458 5459	1000 1500 2000		5000 5500 6000	$\mu mhos$ $\mu mhos$ $\mu mhos$
g_{os}	Output Conductance*	$V_{DS} = 15 V, V_{GS} = 0, f = 1.0 kHz$			10	50	$\mu mhos$
C_{iss}	Input Capacitance	$V_{DS} = 15 V, V_{GS} = 0, f = 1.0 MHz$			4.5	7.0	pF
C_{rss}	Reverse Transfer Capacitance	$V_{DS} = 15 V, V_{GS} = 0, f = 1.0 MHz$			1.5	3.0	pF
NF	Noise Figure	$V_{DS} = 15 V, V_{GS} = 0, f = 1.0 kHz,$ $R_G = 1.0 megohm, BW = 1.0 Hz$				3.0	dB

* Pulse Test: Pulse Width $\leq 300 ms$, Duty Cycle $\leq 2\%$

2N5457 / 5458 / 5459 / MMBF5457 / 5458 / 5459

Need gate-source cutoff voltage

2N7000 n-channel

2N7000 / 2N7002 / NDS7002A N-Channel Enhancement Mode Field Effect Transistor

General Description

These N-Channel enhancement mode field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. These products have been designed to minimize on-state resistance while provide rugged, reliable, and fast switching performance. They can be used in most applications requiring up to 400mA DC and can deliver pulsed currents up to 2A. These products are particularly suited for low voltage, low current applications such as small servo motor control, power MOSFET gate drivers, and other switching applications.

Features

- High density cell design for low $R_{DS(ON)}$
- Voltage controlled small signal switch.
- Rugged and reliable.
- High saturation current capability.



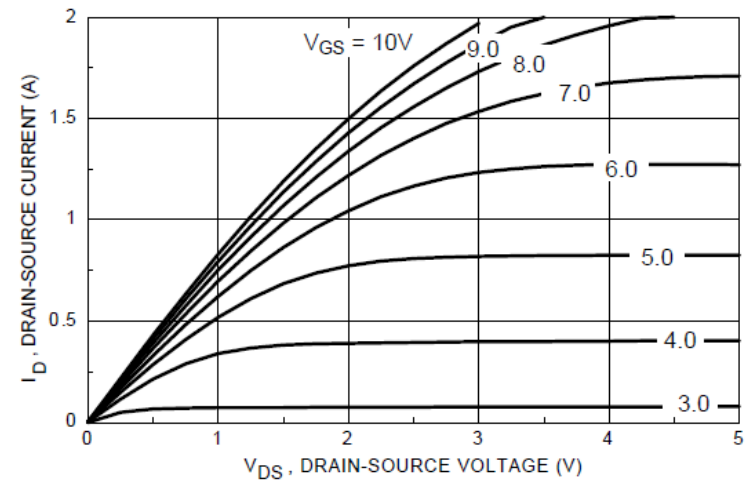
Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	2N7000	2N7002	NDS7002A	Units
V_{DS}	Drain-Source Voltage	60			V
V_{DGR}	Drain-Gate Voltage ($R_{GD} \leq 1 \text{ M}\Omega$)	60			V
V_{GS}	Gate-Source Voltage - Continuous	± 20			V
	- Non Repetitive ($t_p < 50\mu\text{s}$)	± 40			
I_D	Maximum Drain Current - Continuous	200	115	280	mA
	- Pulsed	500	800	1500	
P_D	Maximum Power Dissipation	400	200	300	mW
	Derated above 25°C	3.2	1.6	2.4	
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150			$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering Purposes, 1/16" from Case for 10 Seconds	300			$^\circ\text{C}$

2N7000

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted							
Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 10\ \mu\text{A}$	All	60			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 48\text{ V}, V_{GS} = 0\text{ V}$	2N7000			1	μA
		$T_J = 125^\circ\text{C}$			1	mA	
		$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$	2N7002 NDS7002A			1	μA
		$T_J = 125^\circ\text{C}$				0.5	mA
I_{GSSF}	Gate - Body Leakage, Forward	$V_{GS} = 15\text{ V}, V_{DS} = 0\text{ V}$	2N7000			10	nA
		$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	2N7002 NDS7002A			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	$V_{GS} = -15\text{ V}, V_{DS} = 0\text{ V}$	2N7000			-10	nA
		$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$	2N7002 NDS7002A			-100	nA
ON CHARACTERISTICS (Note 1)							
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 1\text{ mA}$	2N7000	0.8	2.1	3	V
		$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2N7002 NDS7002A	1	2.1	2.5	
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 500\text{ mA}$	2N7000		1.2	5	Ω
		$T_J = 125^\circ\text{C}$			1.9	9	
		$V_{GS} = 4.5\text{ V}, I_D = 75\text{ mA}$	2N7002		1.8	5.3	
		$V_{GS} = 10\text{ V}, I_D = 500\text{ mA}$			1.2	7.5	
		$T_J = 100^\circ\text{C}$		1.7	13.5		
		$V_{GS} = 5.0\text{ V}, I_D = 50\text{ mA}$	NDS7002A		1.7	7.5	
		$T_J = 100^\circ\text{C}$			2.4	13.5	
		$V_{GS} = 10\text{ V}, I_D = 500\text{ mA}$	NDS7002A		1.2	2	
$T_J = 125^\circ\text{C}$		2		3.5			
$V_{GS} = 5.0\text{ V}, I_D = 50\text{ mA}$		1.7	3				
		$T_J = 125^\circ\text{C}$		2.8	5		
$V_{DS(on)}$	Drain-Source On-Voltage	$V_{GS} = 10\text{ V}, I_D = 500\text{ mA}$	2N7000		0.6	2.5	V
		$V_{GS} = 4.5\text{ V}, I_D = 75\text{ mA}$			0.14	0.4	
		$V_{GS} = 10\text{ V}, I_D = 500\text{ mA}$	2N7002		0.6	3.75	
		$V_{GS} = 5.0\text{ V}, I_D = 50\text{ mA}$			0.09	1.5	
		$V_{GS} = 10\text{ V}, I_D = 500\text{ mA}$	NDS7002A		0.6	1	
		$V_{GS} = 5.0\text{ V}, I_D = 50\text{ mA}$			0.09	0.15	

Wide process spread
 $V_{GS(th)} : 0.8\text{-}3\text{V}$



2N7000

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted							
Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
ON CHARACTERISTICS Continued (Note 1)							
$I_{D(ON)}$	On-State Drain Current	$V_{GS} = 4.5\text{ V}, V_{DS} = 10\text{ V}$	2N7000	75	600		mA
		$V_{GS} = 10\text{ V}, V_{DS} \geq 2 V_{DS(on)}$	2N7002	500	2700		
		$V_{GS} = 10\text{ V}, V_{DS} \geq 2 V_{DS(on)}$	NDS7002A	500	2700		
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 200\text{ mA}$	2N7000	100	320		mS
		$V_{DS} \geq 2 V_{DS(on)}, I_D = 200\text{ mA}$	2N7002	80	320		
		$V_{DS} \geq 2 V_{DS(on)}, I_D = 200\text{ mA}$	NDS7002A	80	320		
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	All		20	50	pF
C_{oss}	Output Capacitance		All		11	25	pF
C_{rss}	Reverse Transfer Capacitance		All		4	5	pF
t_{on}	Turn-On Time	$V_{DD} = 15\text{ V}, R_L = 25\ \Omega,$ $I_D = 500\text{ mA}, V_{GS} = 10\text{ V},$ $R_{GEN} = 25\ \Omega$	2N7000			10	ns
		$V_{DD} = 30\text{ V}, R_L = 150\ \Omega,$ $I_D = 200\text{ mA}, V_{GS} = 10\text{ V},$ $R_{GEN} = 25\ \Omega$	2N7002 NDS7002A			20	
t_{off}	Turn-Off Time	$V_{DD} = 15\text{ V}, R_L = 25\ \Omega,$ $I_D = 500\text{ mA}, V_{GS} = 10\text{ V},$ $R_{GEN} = 25\ \Omega$	2N7000			10	ns
		$V_{DD} = 30\text{ V}, R_L = 150\ \Omega,$ $I_D = 200\text{ mA}, V_{GS} = 10\text{ V},$ $R_{GEN} = 25\ \Omega$	2N7002 NDS7002A			20	
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I_S	Maximum Continuous Drain-Source Diode Forward Current		2N7002			115	mA
			NDS7002A			280	
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		2N7002			0.8	A
			NDS7002A			1.5	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 115\text{ mA}$ (Note 1)	2N7002		0.88	1.5	V
		$V_{GS} = 0\text{ V}, I_S = 400\text{ mA}$ (Note 1)	NDS7002A		0.88	1.2	

Note:
1. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

RC time constant for V_{GS} ?

$$C_{iss} \propto C_{GS}$$

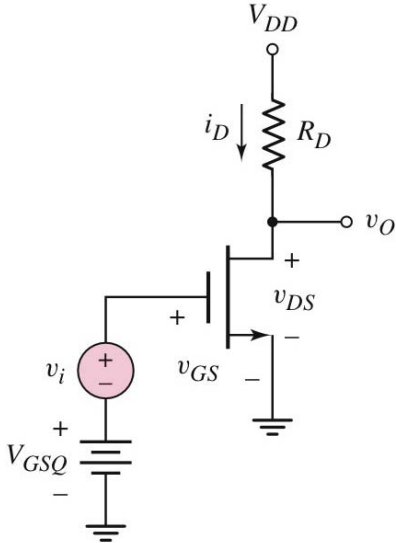
$$C_{oss} \propto C_{DS}$$

$$C_{irs} \propto C_{GD}$$

Estimating MOSFET Parameters
from the Data Sheet

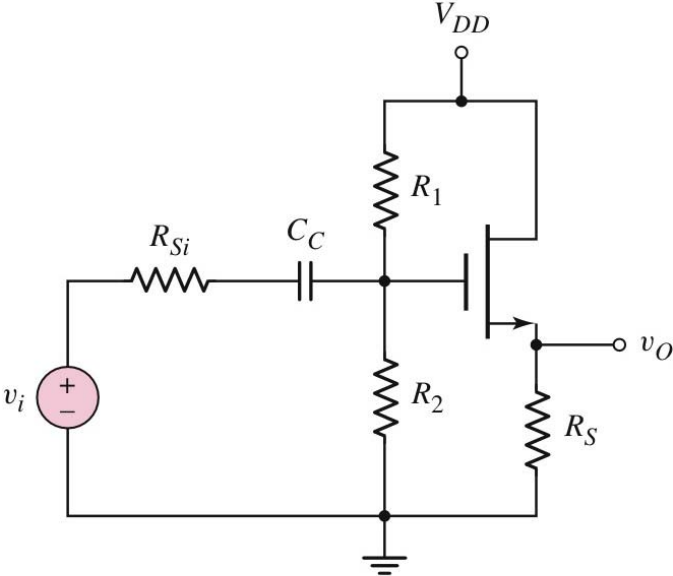
<http://www.ti.com/lit/ml/slup170/slup170.pdf>

MOSFET Configurations



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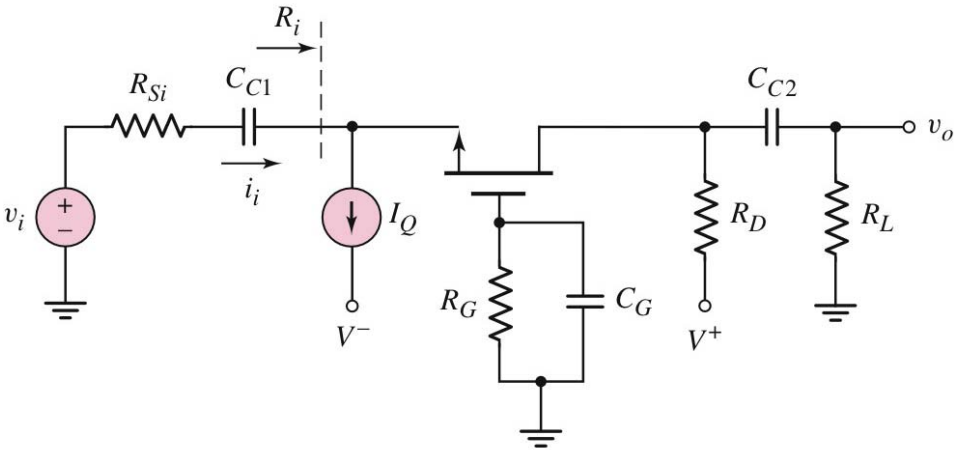
Common source



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Common drain

Common gate

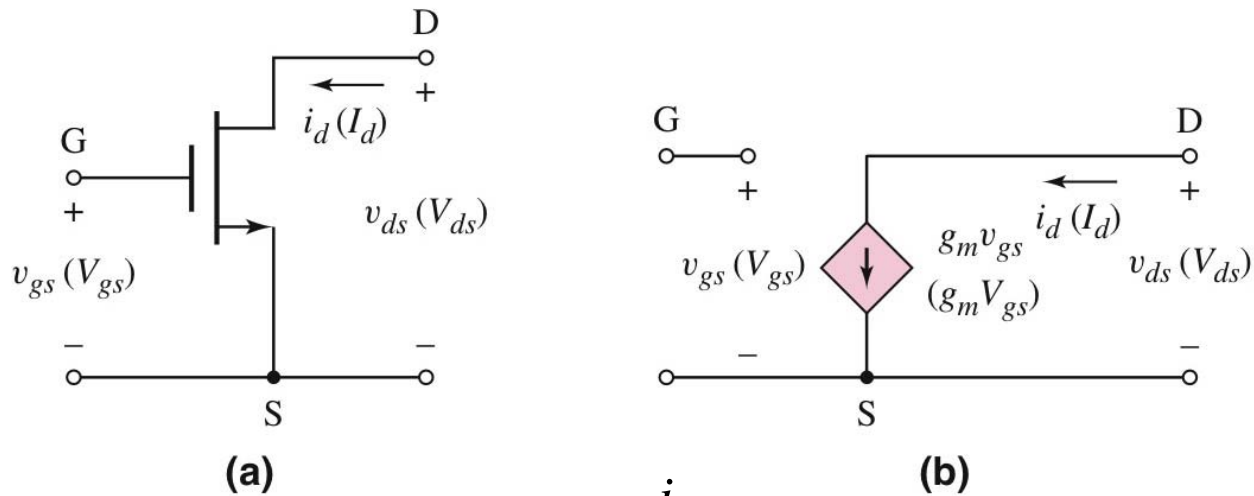


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Basic FET Circuits

- Analog switch - voltage controlled
- Digital logic – microprocessor, VLSI, ASIC
- Power switching – preferred over BJT
- Variable resistors – use linear region of drain curve
- Current sources
- General replacement for bjt (in some cases)

Simple NMOS Small-Signal Equivalent Circuit



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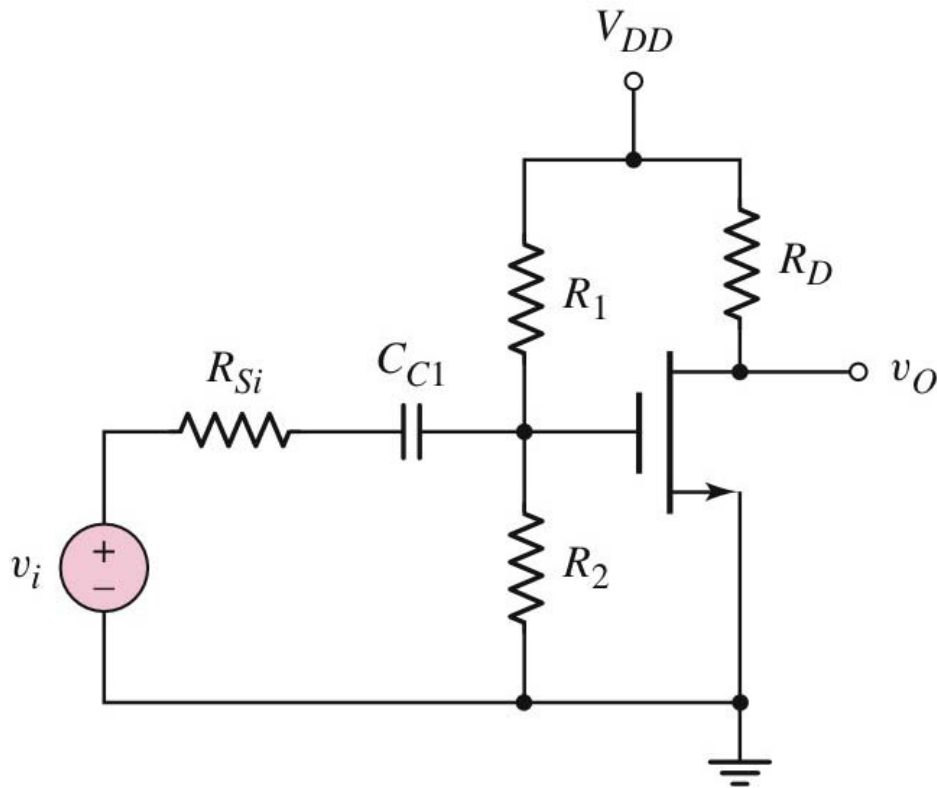
$$g_m = \frac{\partial i_D}{\partial v_{GS}} = \frac{i_d}{v_{gs}}$$

$$g_m = 2K_n (V_{GSQ} - V_{TN}) = 2\sqrt{K_n I_{DQ}}$$

$$r_o = \left(\frac{\partial i_D}{\partial v_{DS}}\right)^{-1}$$

$$r_o = [\lambda K_n (V_{GSQ} - V_{TN})^2]^{-1} \cong [\lambda I_{DQ}]^{-1}$$

Common-Source Configuration



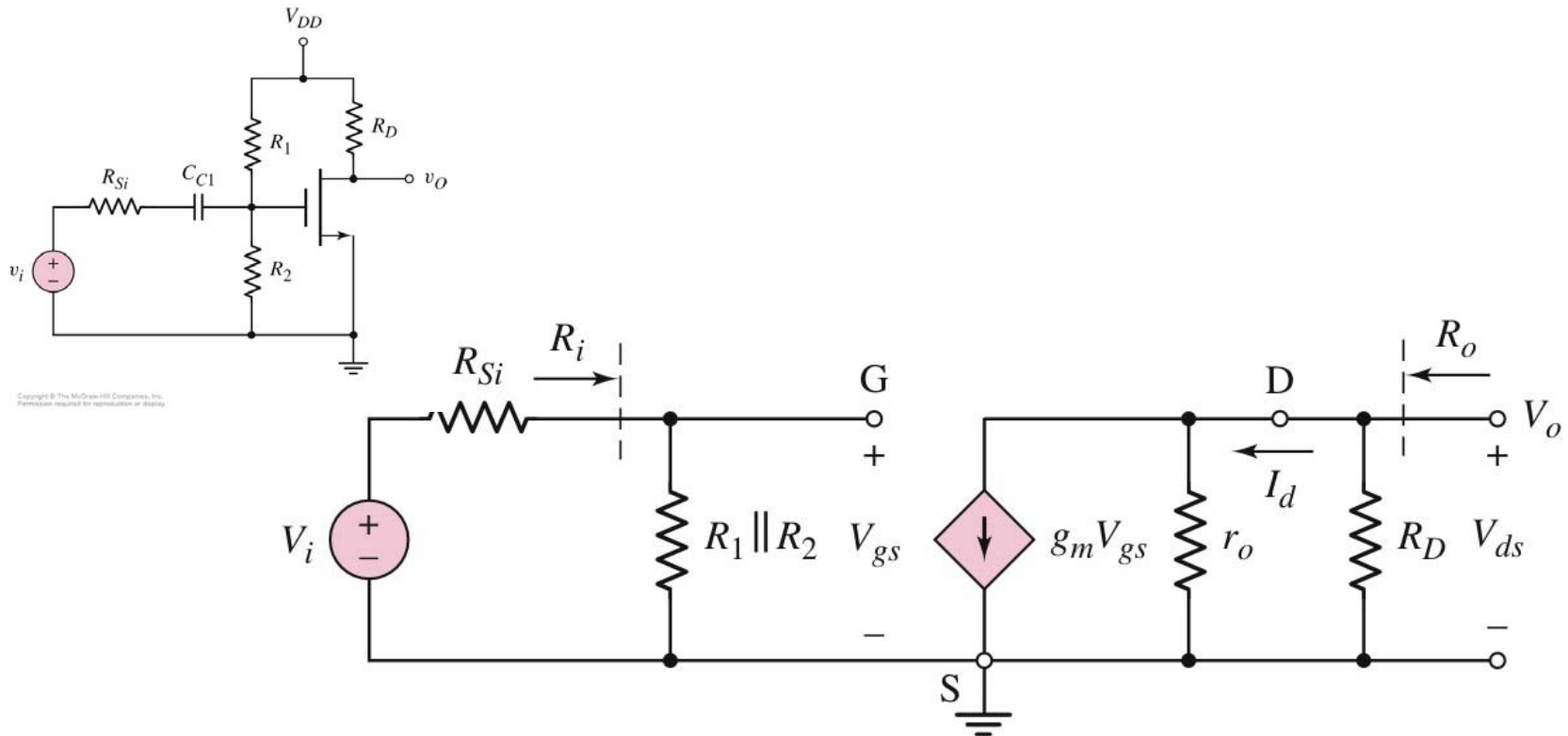
DC analysis:

Coupling capacitor is assumed to be open.

AC analysis:

Coupling capacitor is assumed to be a short. DC voltage supply is set to zero volts.

Small-Signal Equivalent Circuit



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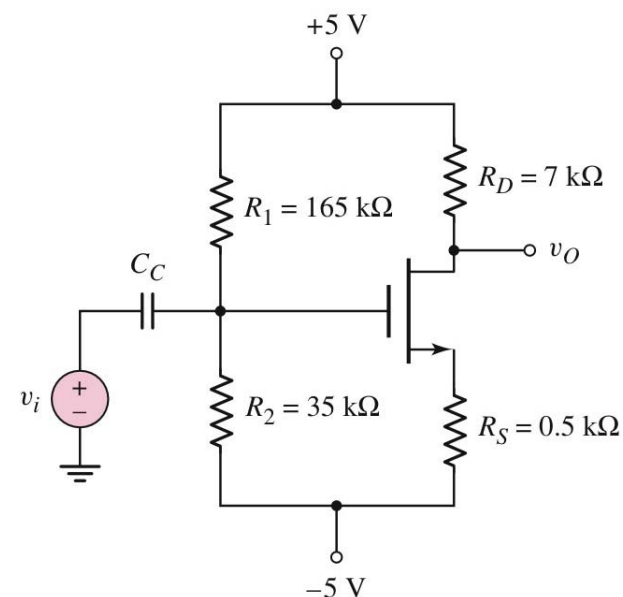
$$A_v = V_o / V_i = -g_m (r_o \parallel R_D) \left(\frac{R_i}{R_i + R_{Si}} \right)$$

Common Source

Neamen Ch 4.3

- More generalized common source with “source degeneration” and equations:

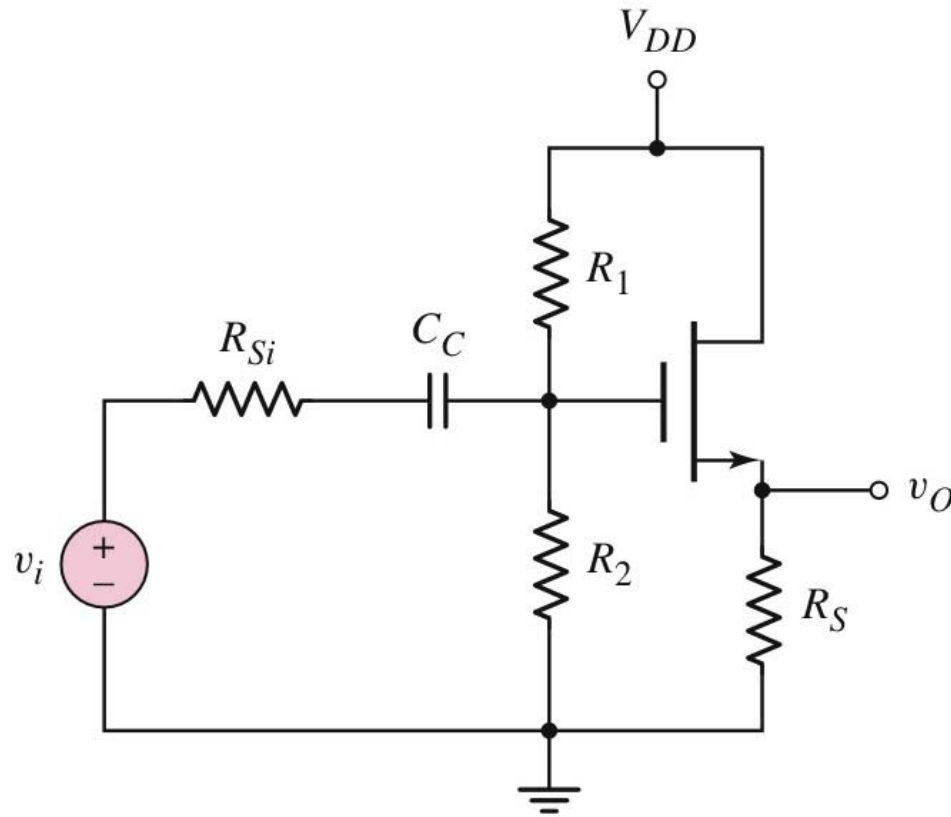
Current gain	$A_i = \frac{I_o}{I_i}$	NA
Voltage gain	$A_v = \frac{V_o}{V_i}$	$\frac{-g_m R_D}{1 + g_m R_S}$
Input resistance	$\frac{V_i}{I_i}$	Determined by biasing
Output resistance	$\frac{V_o}{I_o}$	R_D



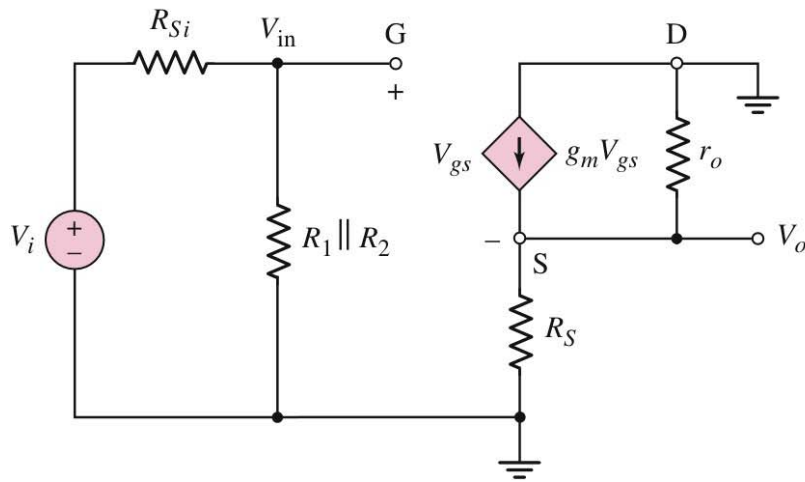
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Usage: voltage amplifier, transconductance amplifier

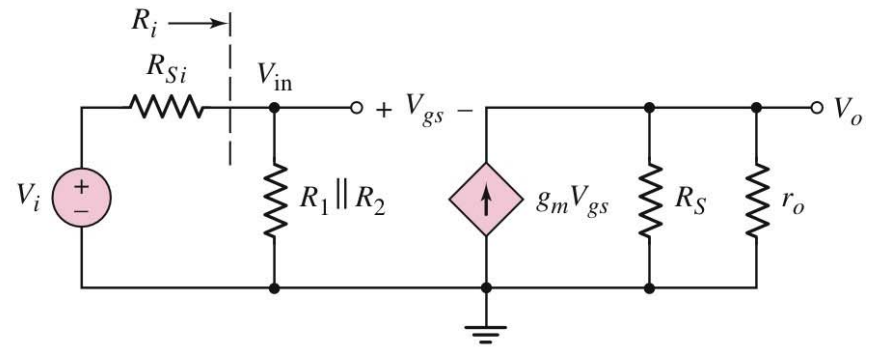
NMOS Source-Follower or Common Drain Amplifier



Small-Signal Equivalent Circuit for Source Follower



(a)



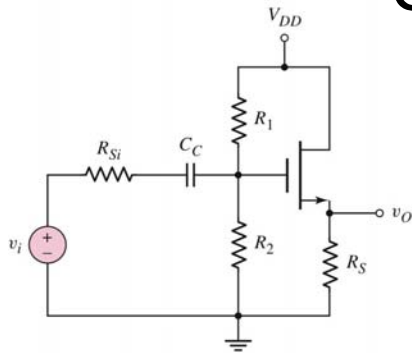
(b)

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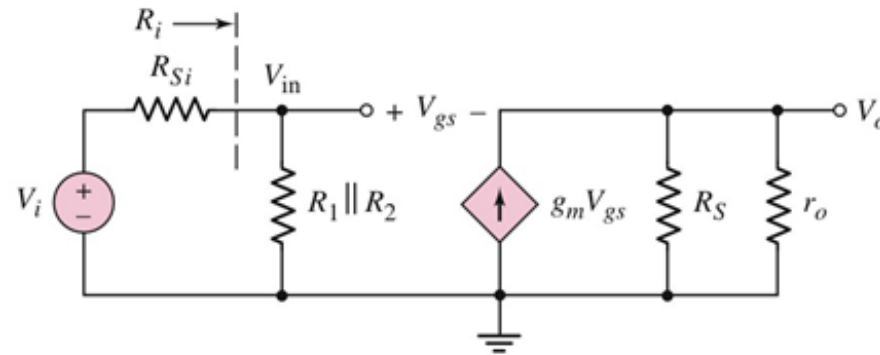
$$A_v = \frac{R_S \parallel r_o}{\frac{1}{g_m} + R_S \parallel r_o} \left(\frac{R_i}{R_i + R_{Si}} \right)$$

Common Drain – Source Follower

Neamen Ch 4.4



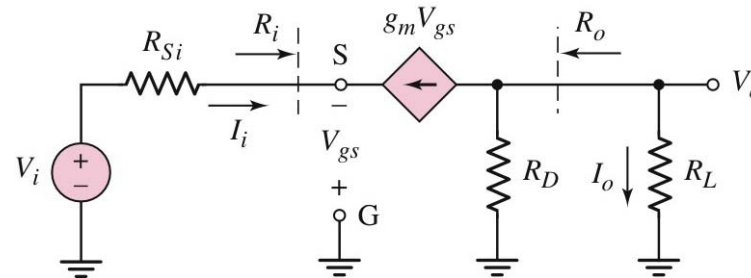
Usage: voltage buffer



Current gain	$A_i = \frac{I_o}{I_i}$	NA
Voltage gain	$A_v = \frac{V_o}{V_i}$	$\frac{g_m R_S r_o}{1 + g_m R_S r_o} \left(\frac{R_i}{R_i + R_{Si}} \right) \approx 1$
Input resistance	$\frac{V_i}{I_i}$	Determined by biasing
Output resistance	$\frac{V_o}{I_o}$	$R_S r_o \frac{1}{g_m}$

Common Gate

Neamen Ch 4.5



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Current gain	$A_i = \frac{I_o}{I_i}$	$\left(\frac{R_D}{R_D + R_L}\right) \left(\frac{g_m R_{Si}}{1 + g_m R_{Si}}\right) \approx 1$ $R_D \gg R_L$ and $g_m R_{Si} \gg 1$
Voltage gain	$A_v = \frac{V_o}{V_i}$	$\frac{g_m (R_D R_L)}{1 + g_m R_{Si}}$
Input resistance	$\frac{V_i}{I_i}$	$\frac{1}{g_m}$
Output resistance	$\frac{V_o}{I_o}$	R_D

Usage: High frequency amplifier

Comparison of 3 Basic Amplifiers

Configuration	Voltage Gain	Current Gain	Input Resistance	Output Resistance
Common Source	$A_v > 1$	—	$*R_{TH}$	Moderate to high
Source Follower	$A_v \approx 1$	—	$*R_{TH}$	Low
Common Gate	$A_v > 1$	$A_i \approx 1$	Low	Moderate to high

* Determined by biasing resistors

Cascode Configurations

All have the same purpose – to decouple the input terminal (of the bottom device) from capacitive feedback from the output by taking the output from a second device.

Bottom device: Current gain (no appreciable voltage gain)

Top device: Voltage gain (no current gain)

Combines common-emitter/source/cathode with common-base/gate/grid.

Result is like a single common-emitter/source/cathode device with drastically reduced “Miller capacitance” from the output to the input

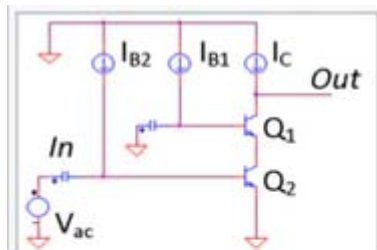


Figure 2: BJT Cascode using ideal current sources for DC bias and large coupling capacitors to ground and to the AC signal source; capacitors are short circuits for AC

BJT

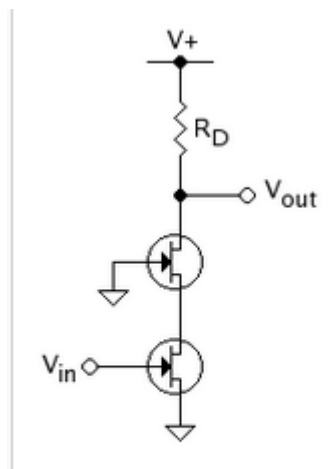


Figure 1: N-channel cascode amplifier with resistive load (neglecting biasing details)

JFET

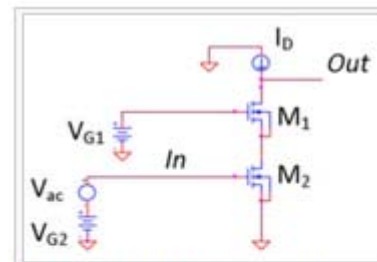
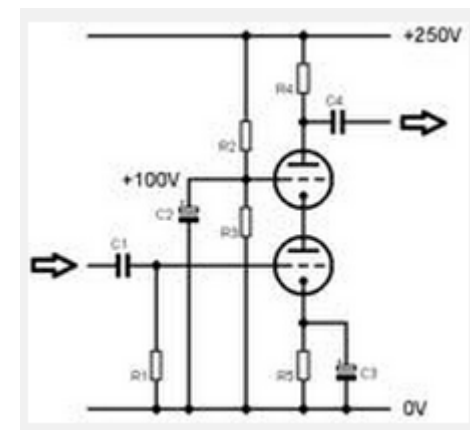


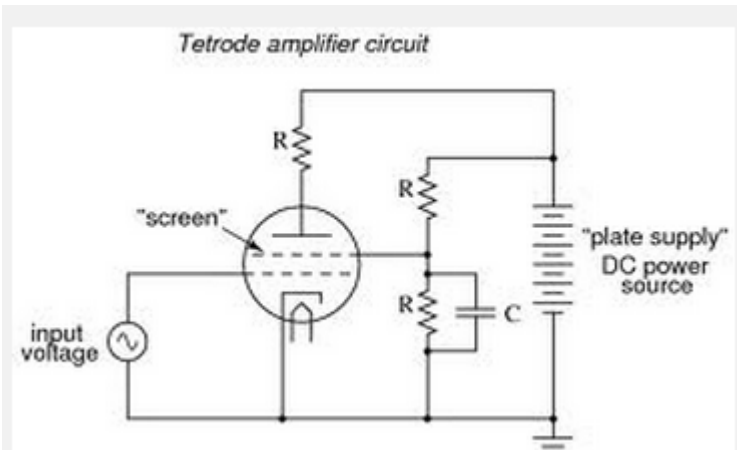
Figure 3: MOSFET Cascode using ideal voltage sources for DC gate bias and a DC current source as active load. Since each MOSFET transistor has gate and source connected, this configuration is valid only for discrete 3-terminal components.

MOSFET

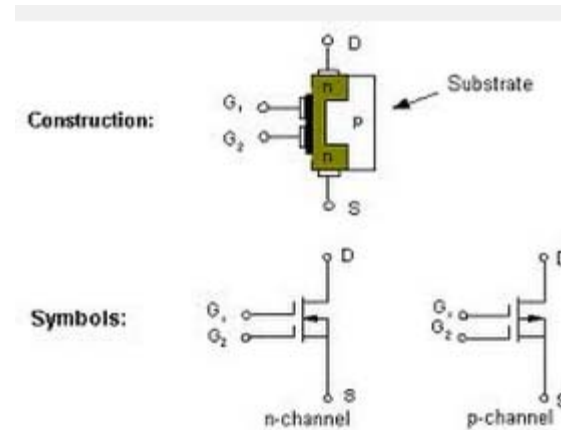


Vacuum
tube triode

Single devices with cascode like construction

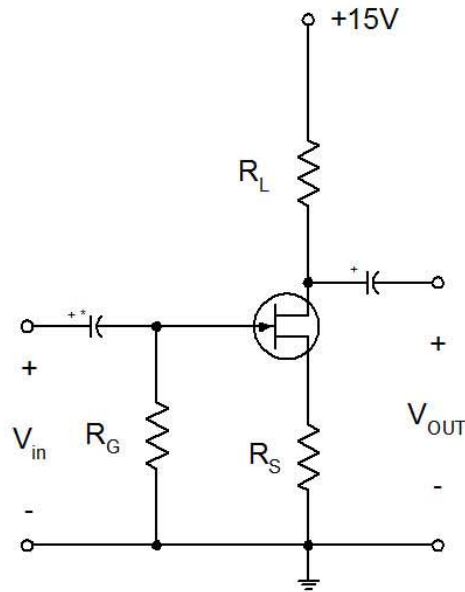


Tetrode (tet for "4" terminal) vacuum tube adds a fourth grid called a "screen" to shield the grid and cathode from the anode

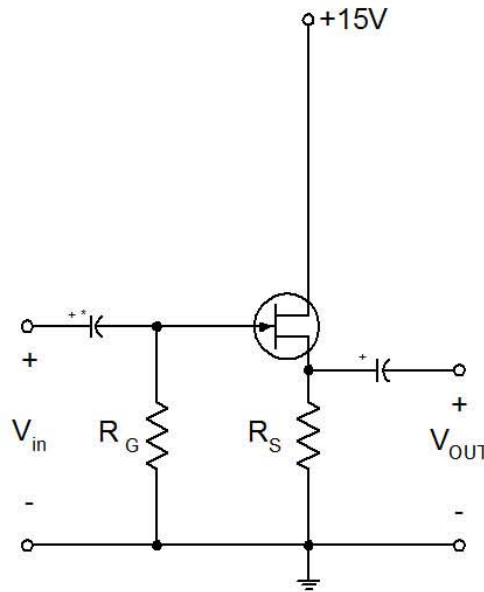


Similar MOSFET device incorporates a second gate. Useful for RF circuits.

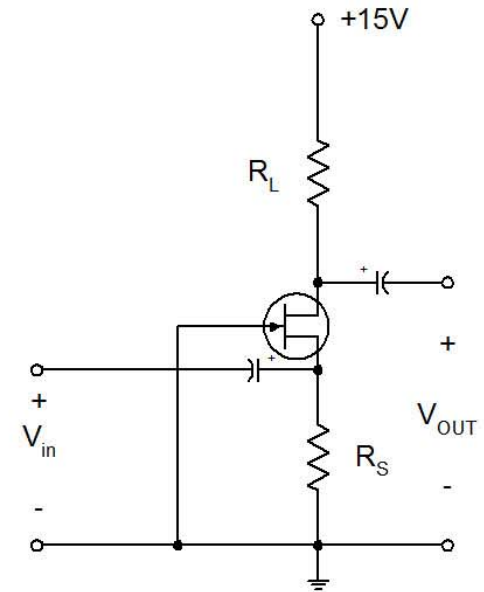
JFET Amplifier Configurations



Common Source Amplifier



Common Drain Amplifier
[Source Follower]

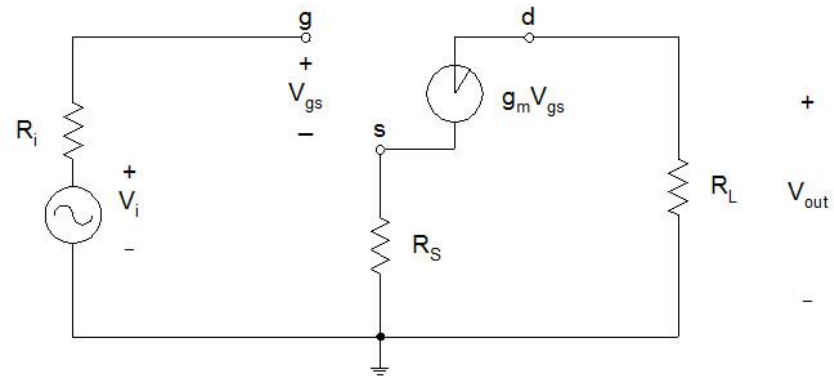
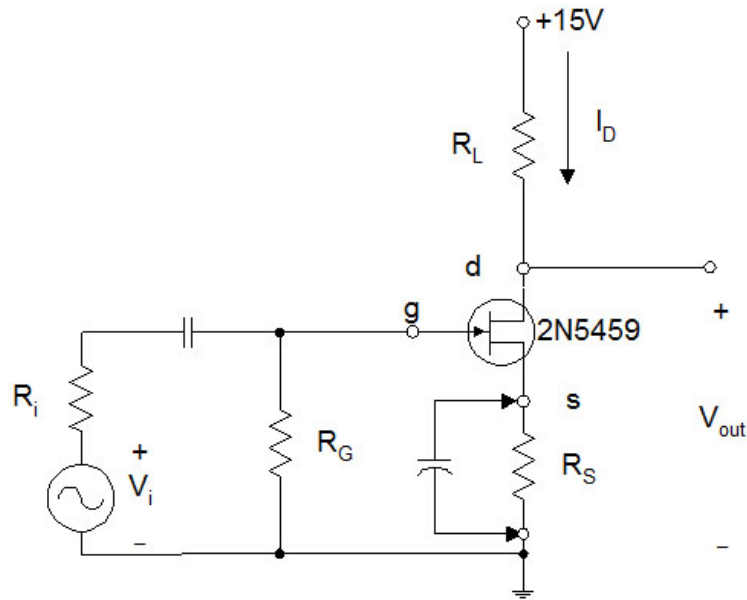


Common Gate Amplifier

* For polarized [electrolytic] input coupling capacitor, the "+" should be oriented towards the most positive DC voltage. For example, if there is -2V on the gate, and -8V associated with V_{in} , then the capacitor orientation should be reversed as shown.

The input coupling cap for the common gate configuration will most often be a polarized electrolytic, since the impedance at the Source of the JFET is only $1/g_m$ in parallel with R_S .

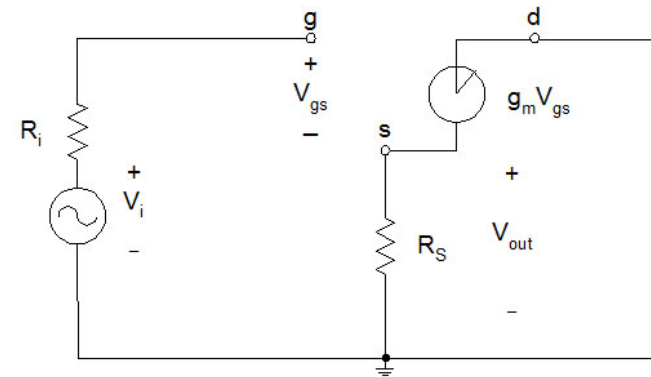
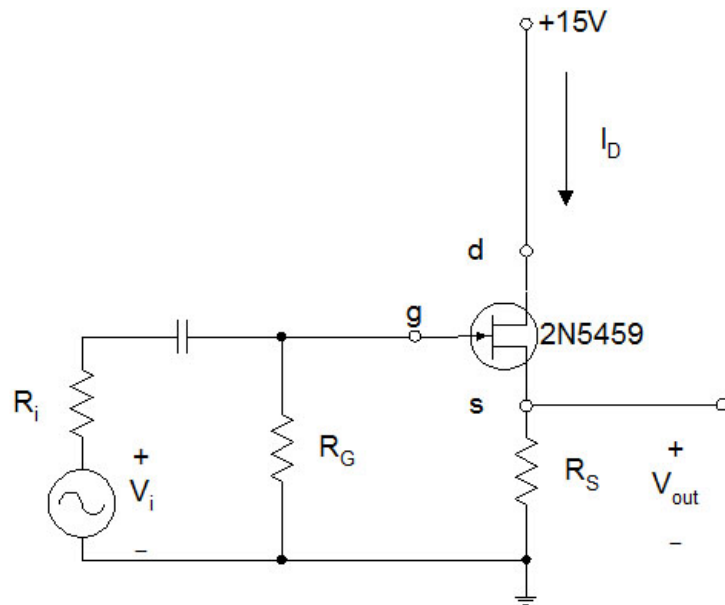
Common Source JFET (bypassed source resistor)



$$A_v = \frac{v_{out}}{v_{in}} = \frac{-g_m v_{gs} R_L}{v_{gs} + g_m v_{gs} R_S} = \frac{-g_m v_{gs} R_L}{v_{gs} [1 + g_m R_S]}$$

$$A_v = \frac{-g_m R_L}{1 + g_m R_S} \quad \text{or} \quad A_v = -g_m R_L$$

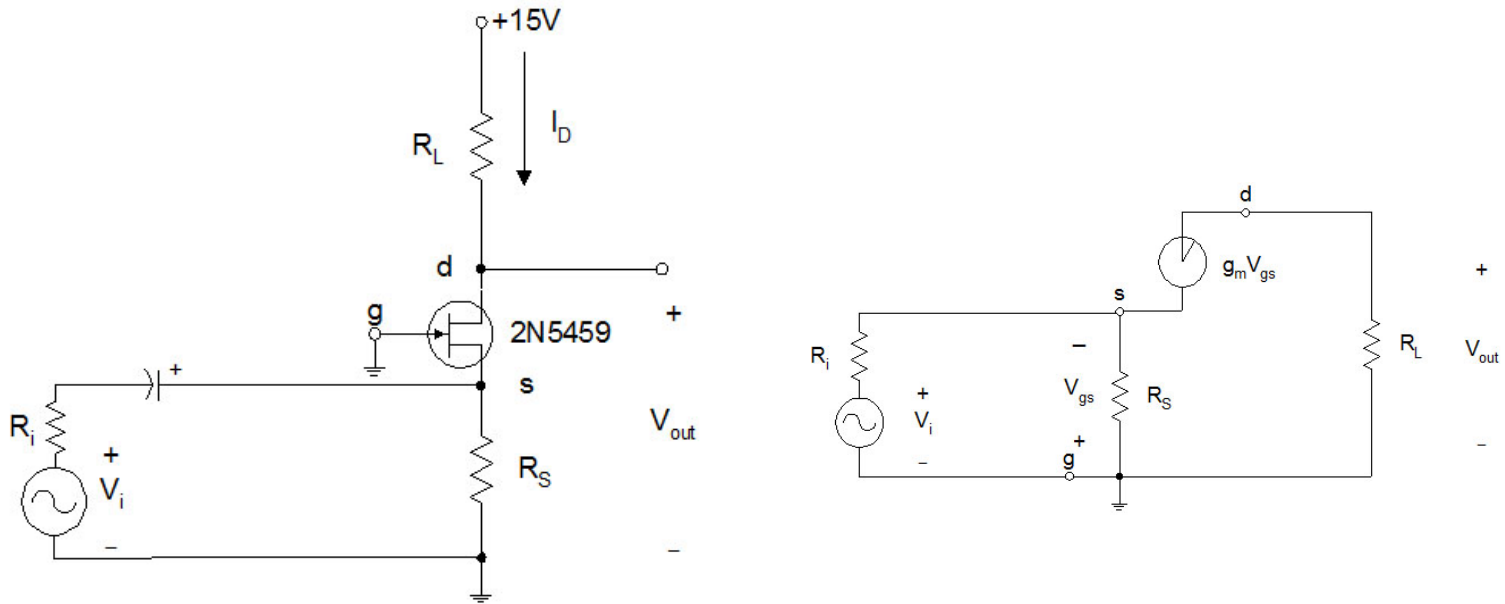
Common Drain Amplifier (Source Follower)



$$A_v = \frac{v_{out}}{v_{in}} = \frac{g_m v_{gs} R_S}{v_{gs} + g_m v_{gs} R_S} = \frac{g_m v_{gs} R_S}{v_{gs} [1 + g_m R_S]}$$

$$A_v = \frac{g_m R_S}{1 + g_m R_S}$$

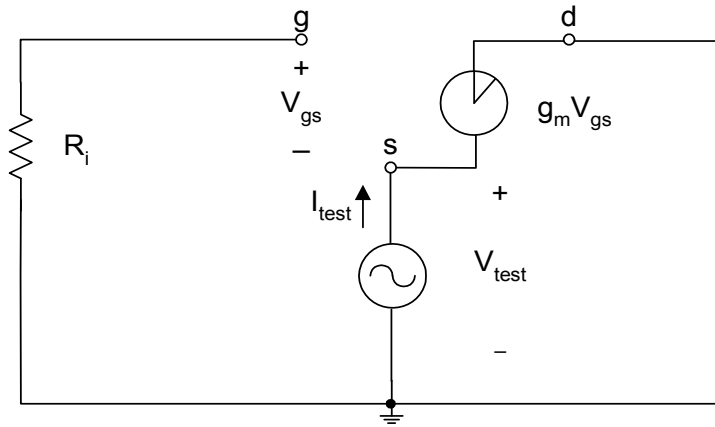
Common Gate Amplifier



$$A_v = \frac{v_{out}}{v_{in}} = \frac{-g_m v_{gs} R_L}{-v_{gs} \left[g_m R_i + \frac{R_i}{R_S} + 1 \right]} = \frac{g_m R_L}{1 + g_m R_i + \frac{R_i}{R_S}}; \quad \text{if } R_i = 0,$$

$$\text{then } A_v = g_m R_L$$

Output Resistance – Source Follower



Remove R_S and replace it with a test AC voltage generator

Short the input signal V_i and replace it with its source resistance R_i .

Solve for I_{test} , which is a consequence of applying the test generator V_{test} , and for V_{test} in terms of the hybrid- π parameters.

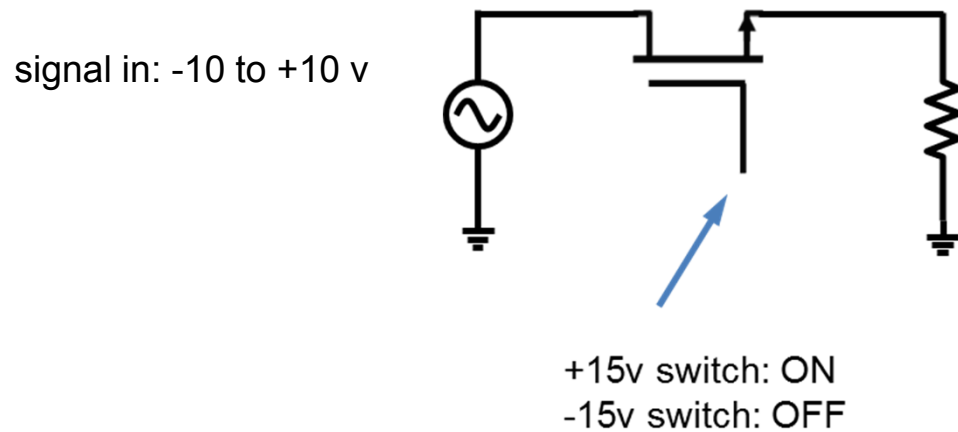
To correctly calculate the value of a bypass capacitor for R_S , use the parallel combination of r_o and R_S .

$$r_o = \frac{V_{test}}{I_{test}} = \frac{-V_{gs}}{-g_m V_{gs}} = \frac{1}{g_m}$$

Low Frequency Hybrid π Model

Characteristic	Common Source	C Source with R_S	Common Drain [Source Follower]	Common Gate
Voltage Gain [if $r_{ds} \gg R_L$]	$A_v = -g_m R_L$	$A_v = \frac{-g_m R_L}{1 + g_m R_S}$	$A_v = \frac{g_m R_S}{1 + g_m R_S}$	$A_v = \frac{g_m R_L}{1 + g_m R_i + \frac{R_i}{R_S}}$ <small>R_i = generator resistance</small>
Current Gain	$\frac{I_D}{I_S}$ Very large!	$\frac{I_D}{I_S}$ Very large!	$\frac{I_D}{I_S}$ Very large!	$A_i = \frac{g_m R_S}{g_m R_S + 1}$
Input Impedance	R_G	R_G	R_G	$\frac{R_S}{g_m R_S + 1} = \frac{1}{g_m} // R_S$
Output Impedance	R_L [if $r_{ds} \gg R_L$]	R_L [if $r_{ds} \gg R_L$]	$\frac{R_S}{g_m R_S + 1} = \frac{1}{g_m} // R_S$	R_L [if $r_{ds} \gg R_L$]
Phase Reversal?	Yes	Yes	No	No

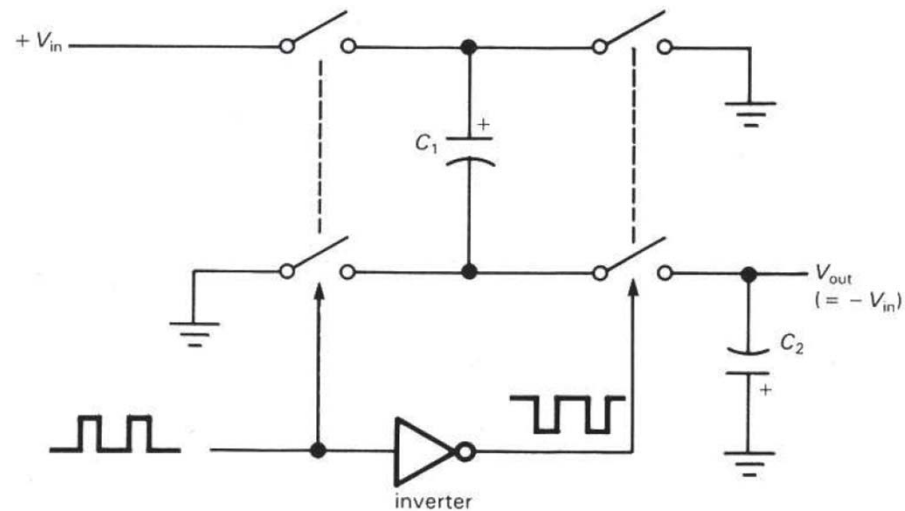
OK, now what can we do with these things?



MOSFET analog switch

OK, now what can we do with these things?

This schematic from the now obsolete Intersil 7662 datasheet shows how a “flying capacitor” generates a negative voltage from a positive voltage. Slightly different connections can double a voltage instead of inverting it.



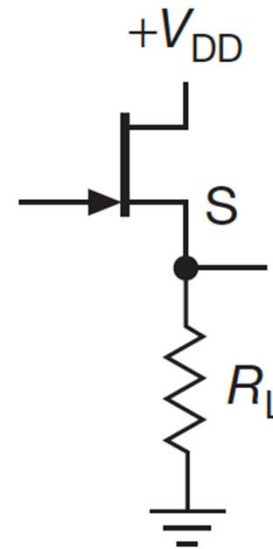
Art of Electronics: Figure 3.86

Source Follower

$$v_s = R_L i_d$$

$$i_d = g_m v_s = g_m (v_g - v_s)$$

$$v_s = \left[\frac{R_L g_m}{1 + R_L g_m} \right] v_g$$

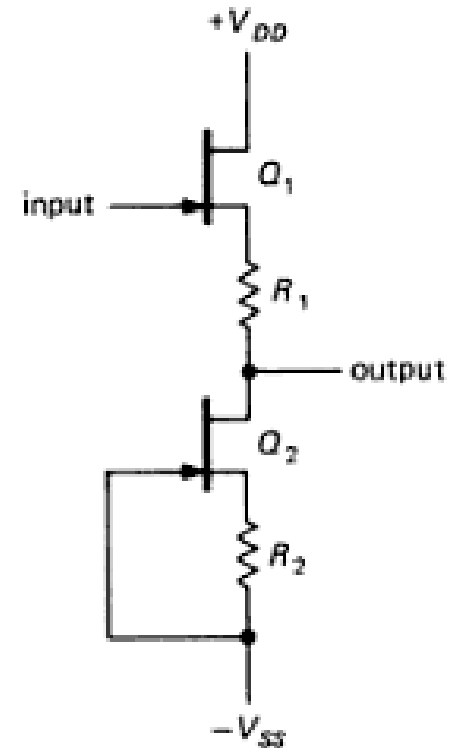


JFET follower

A JFET follower using matched (dual) JFET's. The bottom JFET automatically generates just the right amount of current to bias the top one so V_{in} is approximately equal to V_{out} .

$R_1 = R_2$ guarantees $V_{out} = V_{in}$ if Q_1 and Q_2 are matched.

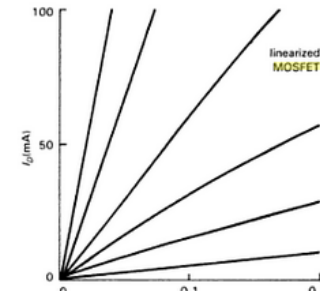
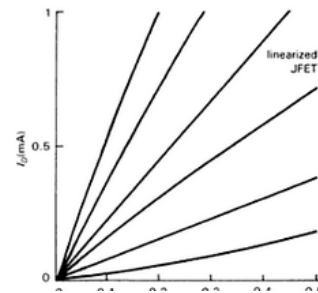
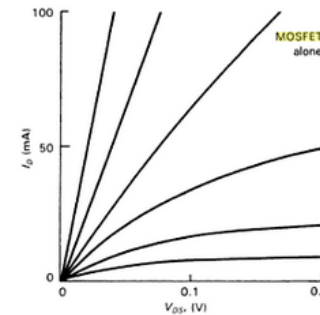
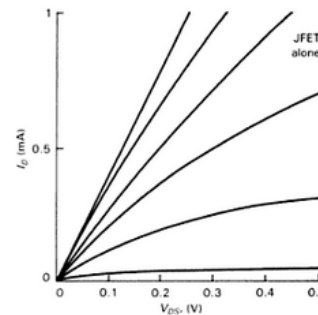
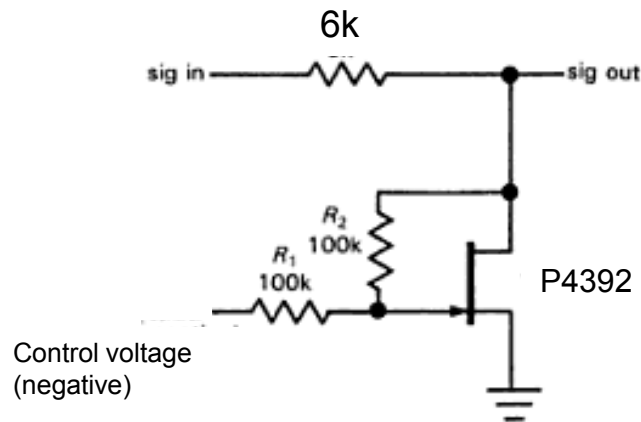
Horowitz Hill, 3rd Edition p160



JFET variable attenuator

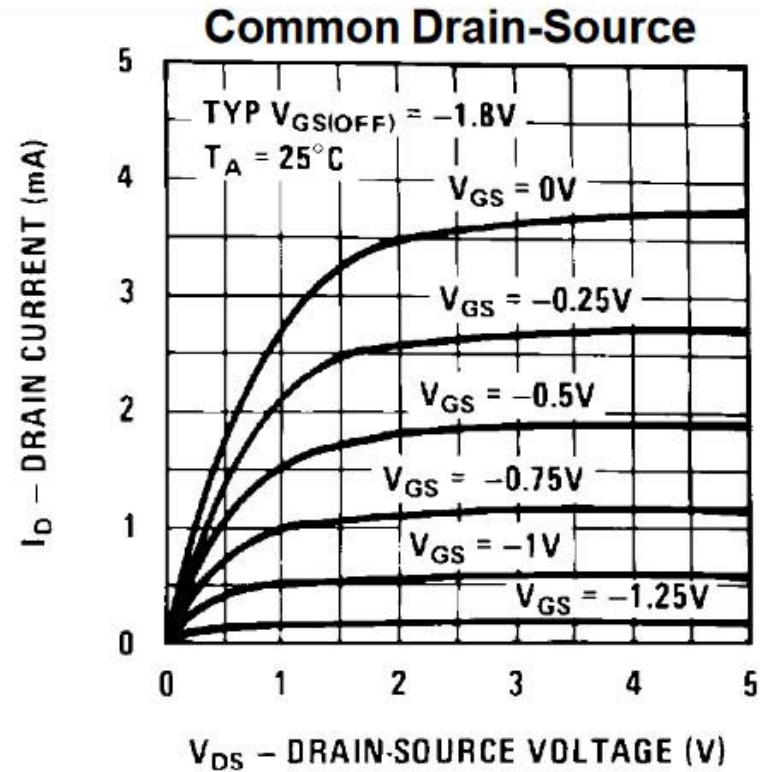
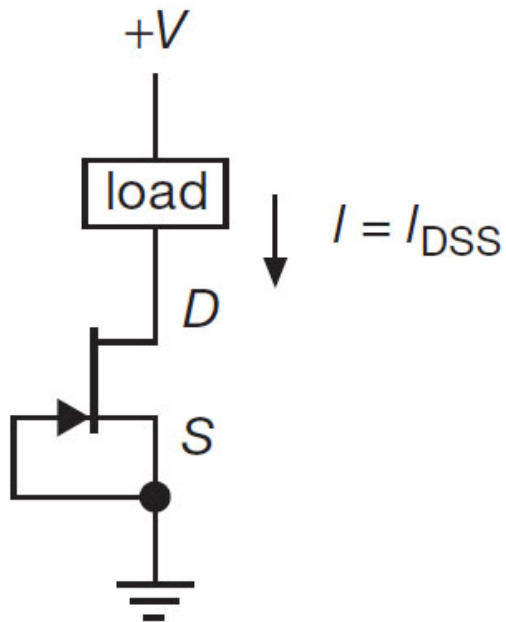
The Dolby B noise reduction circuit used this circuit as a Variable attenuator. By adding $\frac{1}{2}$ the drain voltage back to the gate voltage linearizes the JFET resistance.

$$\frac{1}{r_{DS}} = 2K \left[(V_{GS} - V_{th}) - \frac{V_{DS}}{2} \right]$$

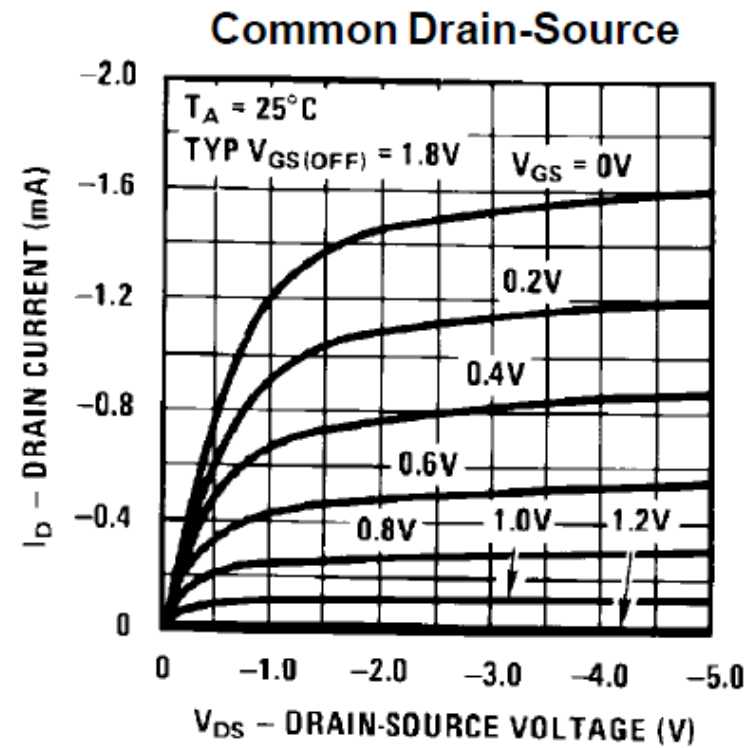
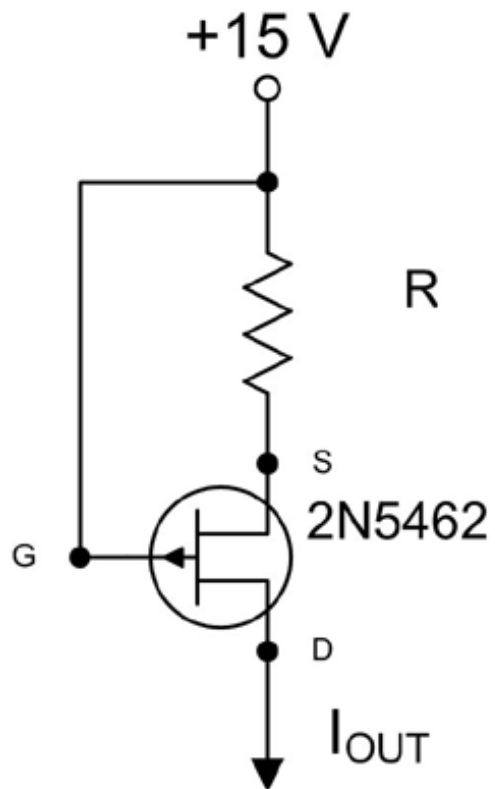


From An introduction to electronics, Cambridge Univ Press

n-Channel JFET Current Source 2N5459



P-Channel JFET Current Source



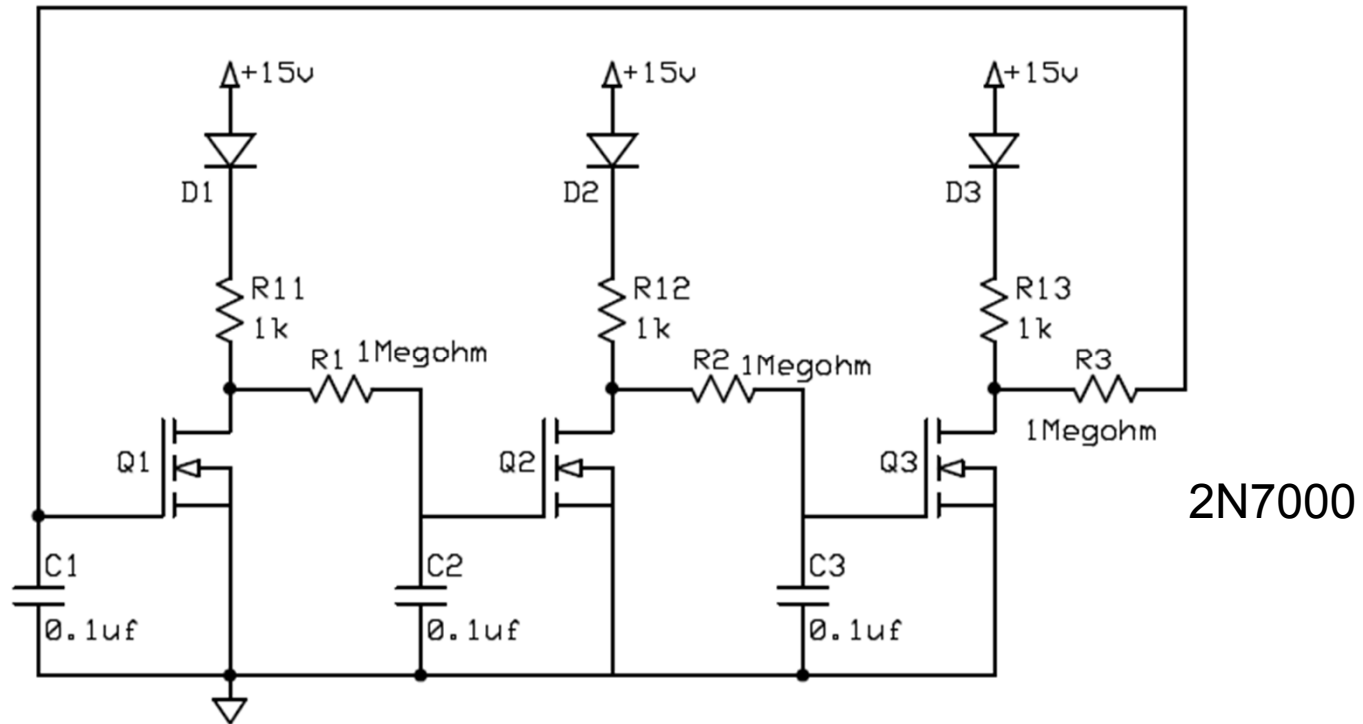
Neat Circuit Ideas

From <http://www.talkingelectronics.com/projects/MOSFET/MOSFET.html>

Make a classic phase shift oscillator (3 stages of 60 deg phase shift each – any three digital logic inverters will usually do) so you can WATCH the oscillation run around the loop! Works with any odd number of stages.

Question : Is this guaranteed to start up? Why?

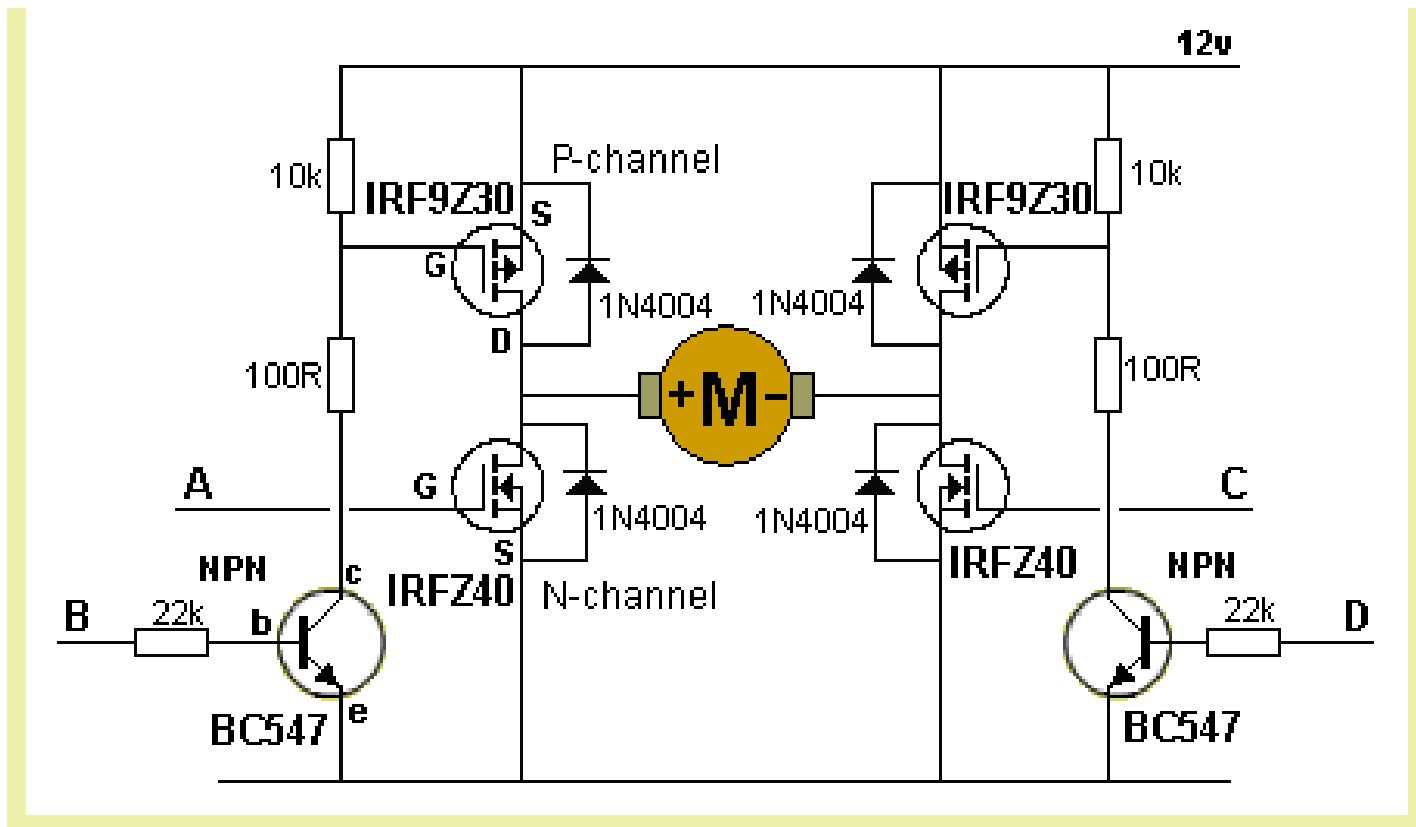
And what if you had a large (odd) number of stages – can you start a skinny pulse going around the loop? Will it stay skinny or widen and turn into 50-50% duty cycle?



Important basic power configuration

The H-bridge

Note how the high-side MOSFET's are driven by level shift. Four drive signals required. Note the trade-off in switching speed versus static power dissipation in level shifter. The 10k resistor will not turn off the IRF9Z30 very fast. But motor drives don't operate at very high frequencies.



WHY MOSFETs FAIL

There are quite a few possible causes for device failures, here are a few of the most important reasons:

Over-voltage: MOSFETs have very little tolerance to over-voltage. Damage to devices may result even if the voltage rating is exceeded for as little as a few nanoseconds. MOSFET devices should be rated conservatively for the anticipated voltage levels and careful attention should be paid to suppressing any voltage spikes or ringing.

Prolonged current overload: High average current causes considerable thermal dissipation in MOSFET devices even though the on-resistance is relatively low. If the current is very high and heatsinking is poor, the device can be destroyed by excessive temperature rise. MOSFET devices can be paralleled directly to share high load currents.

Transient current overload: Massive current overload, even for short duration, can cause progressive damage to the device with little noticeable temperature rise prior to failure.

MOSFET failure modes continued

Shoot-through - cross conduction: If the control signals to two opposing MOSFETs overlap, a situation can occur where both MOSFETs are switched on together. This effectively short-circuits the supply and is known as a shoot-through condition. If this occurs, the supply decoupling capacitor is discharged rapidly through both devices every time a switching transition occurs. This results in very short but incredibly intense current pulses through both switching devices. Allow a dead time between switching transitions, during which neither MOSFET is turned on. This allows time for one device to turn off before the opposite device is turned on.

No free-wheel current path: When switching current through any inductive load (such as a Tesla Coil) a back EMF is produced when the current is turned off. It is essential to provide a path for this current to free-wheel in the time when the switching device is not conducting the load current. This current is usually directed through a free-wheel diode connected anti-parallel with the switching device. When a MOSFET is employed as the switching device, the designer gets the free-wheel diode "for free" in the form of the MOSFETs intrinsic body diode. This solves one problem, but creates a whole new one...

MOSFET failure modes continued

Excessive gate drive:

If the MOSFET gate is driven with too high a voltage, then the gate oxide insulation can be punctured rendering the device useless. Gate-source voltages in excess of +/- 15 volts are likely to cause damage.

The actual failure mechanism is usually you melt the clamping zener, and the puddle of molten silicon forms a short. The MOSFET may be fine, but the gate is now shorted to the source, which makes it kind of hard to use.

MOSFET failure modes continued

Insufficient gate drive - incomplete turn on:

MOSFET devices are only capable of switching large amounts of power because they are designed to dissipate minimal power when they are turned on. If the device is not fully turned on then the device will have a high resistance during conduction and will dissipate considerable power as heat.

The newer power parts have long been based on the latest digital process: i.e., they're designed for 5V. Newer power MOSFET's have guaranteed on resistance at lower V_{gs} voltages consistent with use in 3.3V logic inputs, and have V_{ds} absolute maximum ratings of 6V or 7V, and similar abs max V_{gs} ratings. Modern logic requires lots of power conversion devices operating at these low voltages.

For further reading and possible inspiration for your projects, read Jim Williams app notes! You gotta love a guy who titles an app note (#25) :



Switching Regulators for Poets A Gentle Guide for the Trepidatious

Jim Williams

The above title is not happenstance and was arrived at after considerable deliberation... Mysterious modes, sudden, seemingly inexplicable failures, peculiar regulation characteristics and just plain explosions are common occurrences. Diodes conduct the wrong way. Things get hot that shouldn't. Capacitors act like resistors, fuses don't blow and transistors do. The output is at ground, and the ground terminal shows volts of noise. Added to this poisonous brew is the regulator's feedback loop, sampled in nature and replete with uncertain phase shifts. Everything, of course, varies with line and load conditions— and the time of day, or so it seems. In the face of such menace, what are Everyman and the poets to do?



(They told me I couldn't leave the last page blank)

William

'87



Analog Drawing Board
Nicholas Klugman & Henry Love