Crossover Distortion Analysis

The emitter follows the base by 0.6v, \( v_b \) incrementally follows \( v_e \).

The emitter current:
\[
I_e = \frac{v_b}{\beta} = \frac{v_b}{1000}
\]

The collector voltage, assuming large \( \beta \) (\( I_e = I_C \)):
\[
\Delta V_C = \frac{-I_e}{\beta} = \frac{v_b}{10000}
\]

Now we have enough information, i.e. equations to pull everything together:

\[
V_{in} = -570 \left( \frac{11}{10} v_{in} + \frac{1}{10} v_{out} \right)
\]

\[
V_{out} = \frac{570}{10} + \frac{570}{10} v_{in} = 10.8
\]

\[
V_{in} = \frac{-570}{11} v_e + \frac{1}{10} v_{out} + v_e
\]

\[
V_{out} = \frac{-570}{11} v_e + \frac{1}{10} v_{out} + v_e = 10.8 v_e + 0.0172 v_e
\]

- The distortion 0.6v in each direction or 1.2v total resulting in a hole that is:
  
  \[ 0.0172 \times 1.2 \approx 0.02v \]

- Increasing open loop gain will reduce the crossover distortion.
BJT - FET

Bipolar Junction Transistor
• Three terminal device
• Collector current controlled by base current $i_b = f(V_{be})$
• Think as current amplifier
• NPN and PNP

Field Effect Transistor
• Three terminal device
• Channel conduction controlled by electric field
• No forward biased junction i.e. no current
• JFETs, MOSFETs
• Depletion mode, enhancement mode

BJT - JFETS - MOSFETS

<table>
<thead>
<tr>
<th></th>
<th>BJT</th>
<th>JFET</th>
<th>MOSFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Circa</td>
<td>1960</td>
<td>1970</td>
<td>1980</td>
</tr>
<tr>
<td>Gm/I (signal gain)</td>
<td>Best</td>
<td>Better</td>
<td>Good</td>
</tr>
<tr>
<td>Isolation</td>
<td>PN Junction</td>
<td>Metal Oxide*</td>
<td></td>
</tr>
<tr>
<td>ESD</td>
<td>Low</td>
<td>Moderate</td>
<td>Very sensitive</td>
</tr>
<tr>
<td>Control</td>
<td>Current</td>
<td>Voltage</td>
<td>Voltage</td>
</tr>
<tr>
<td>Power</td>
<td>YES</td>
<td>No</td>
<td>Yes</td>
</tr>
</tbody>
</table>

*silicon dioxide

Voltage Noise *

FET Family Tree

* Horowitz & Hill, Art of Electronics 3rd Edition p 170
**MOSFET & JFETS**

- Much more finicky difficult process (to make) than JFET’s.
- Good news: Extremely high input impedance. Zero input current.
- Bad news: Easily blown up by ESD on the gate. Add protection circuit and input bias current becomes at best comparable to JFET’s.
- Good news: Essentially infinitely fast. If you change the gate voltage, the device will respond instantaneously! Essentially always in static equilibrium.
- Bad news: It can be *really* hard to change the gate voltage quickly! (especially power devices – BIG BIG capacitor)
- Much better power devices than JFET’s. (There were briefly power JFET’s as output devices in audio amps. Too many blew up.)
- And you can’t make digital VLSI out of JFET’s.

---

**MOSFET vs JFETS**

- JFET’s
  - Very simple manufacturing process like BJT’s. Much cheaper than (discrete) MOSFET’s. Quieter than MOSFET’s.
  - Low input bias current – like back biased diode. As low as 10pA.
  - But note this doubles every 6 deg C! At high temps a JFET op amp can have more input current than some bipolar op amps!
  - Used in microphones, hearing aids and other high impedance sources (electret microphones have very high output impedance) because of low noise and ruggedness compared to MOSFET’s.
  - Fast. Used on many high speed scope probes. Was major advance in bias current and speed over bipolar-input op amps. See data sheets of (JFET input) LF356 series and compare to then bipolar’s.
  - Downside is input capacitance can’t be as low as some BJT’s.
  - Wide spread in threshold voltage and zero-Vgs current. Sometimes requires sorting and selecting for a given circuit.

---

**MOSFET Symbols**

- **N-channel MOSFET**
  - **IRFD9110**
  - **2N7000**

- **P-channel MOSFET**
  - **IRFD9110**
  - **2N7000**

---

**Transistor Polarity Mapping**

* Horowitz & Hill, the Art of Electronics, 3rd Edition
**JFET: Junction FET Symbol**

N channel JFET  
D  
S  
G  

P channel JFET  
D  
S  
G  

**Simple Model of MOSFET**

MOSFET made VLSI (microprocessors and memories) possible.  
MOSFET is a voltage-controlled device with an operating voltage of ~25 V.  
High input resistance and high voltage control make MOSFETs suitable for use in microprocessors and memories.  

**MOSFETs: Gain & non-linearity**

MOSFETs (metal-oxide-semiconductor field-effect transistors) are four-terminal voltage-controlled switches. Current flows between the diffusion terminals if the voltage on the gate terminal is large enough to create a conducting “channel”, otherwise the mosfet is off and the diffusion terminals are not connected.  

**FETs as switches**

The four terminals of a Field Effect Transistor (gate, source, drain and bulk) connect to conductors that generate a complicated set of electric fields in the channel region which depend on the relative voltages of each terminal.  

INVERSION: A sufficiently strong vertical field will attract enough electrons to the surface to create a conductive n-type channel between the source and drain. The gate voltage when the channel first forms is called the *threshold voltage* – the mosfet switch goes from “off” to “on”.  

CONDUCTION: If a channel exists, a horizontal field will cause a drift current from the drain to the source.
Four states of MOSFET for different Vgs and Vds

What's the difference between the drain and the source?

MOSFETs can be symmetrical and drain and source interchangeable. Especially inside IC's.

But discrete devices (with few exceptions) have input protection networks on the gate to protect against ESD. Also, the substrate must connect somewhere.

Once the input protection clamping and the substrate are connected to a terminal, that must be the source.

Classic “ideal” MOSFET characteristics –
Flat curves in saturation region assume “long” channel

“ideal” MOSFET curves continued

Triode mode, or “linear” mode, or ohmic region.
\[ I_D = \frac{\mu_C W}{2} \left( (V_{GS} - V_T) V_{DS} - \frac{V_D^2}{2} \right) \]

Saturation or active mode.
\[ I_D = \frac{\mu_C W}{2} \left( V_{GS} - V_T \right) \left( 1 + \lambda (V_{DS} - V_T) \right) \]

As the channel length becomes short, these equations become inaccurate. At the channel ends, source and drain regions causing “fringing” effects and Distort the electric fields from the “ideal” case used to derive above eq’s.

For analog design, long-channel MOSFET’s can offer extremely high output impedance, making excellent “stiff” current sources. Minimum geometry transistors used in digital VLSI do not have such flat curves.
Channel Length Modulation: Early Voltage

\[ i_D = \frac{1}{F_0} \]

\[ -V_A = \frac{1}{\lambda} \]

JFET p-channel

Need gate-source cutoff voltage

2N7000 n-channel
MOSFET Configurations

- Analog switch - voltage controlled
- Digital logic – microprocessor, VLSI, ASIC
- Power switching – preferred over BJT
- Variable resistors – use linear region of drain curve
- Current sources
- General replacement for bjt (in some cases)
Simple NMOS Small-Signal Equivalent Circuit

\[ g_m = \frac{\partial i_d}{\partial v_g} = \frac{i_d}{v_g} \]

\[ g_m = 2K_n(V_{GSQ} - V_{TN}) = 2\sqrt{K_n} I_{DSQ} \]

\[ r_o = (\frac{\partial v_o}{\partial v_g})^{-1} = \frac{\partial 2K_n(V_{GSQ} - V_{TN})}{\partial v_g}^{-1} = \frac{\partial I_{DSQ}}{\partial v_g}^{-1} \]

Common-Source Configuration

DC analysis: Coupling capacitor is assumed to be open.

AC analysis: Coupling capacitor is assumed to be a short. DC voltage supply is set to zero volts.

Small-Signal Equivalent Circuit

Common Source

Neamen Ch 4.3

- More generalized common source with "source degeneration" and equations:

\[ A_v = V_o / V_i = -g_m (r_o || R_D) \left( \frac{R}{R_i + R_S} \right) \]

Usage: voltage amplifier, transconductance amplifier
**NMOS Source-Follower or Common Drain Amplifier**

![NMOS Source-Follower or Common Drain Amplifier Diagram]

**Small-Signal Equivalent Circuit for Source Follower**

\[ A_v = \frac{R_S || r_g}{1 + R_S || r_g \left( \frac{R_i}{R_i + R_{Si}} \right)} \]

**Common Drain – Source Follower**

- Usage: voltage buffer

<table>
<thead>
<tr>
<th>Current gain</th>
<th>[ A_I = \frac{I_o}{I_i} ]</th>
<th>NA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage gain</td>
<td>[ A_V = \frac{V_o}{V_i} ]</td>
<td>[ \frac{g_m R_s</td>
</tr>
<tr>
<td>Input resistance</td>
<td>[ \frac{V_i}{I_i} ]</td>
<td>Determined by biasing</td>
</tr>
<tr>
<td>Output resistance</td>
<td>[ \frac{V_o}{I_o} ]</td>
<td>[ R_s</td>
</tr>
</tbody>
</table>

**Common Gate**

- Usage: High frequency amplifier

| Current gain | \[ A_I = \frac{I_o}{I_i} \] | \[ \frac{R_D}{R_{o} + R_{L}} \left( \frac{g_m R_D}{1 + g_m R_{Si}} \right) \approx 1 \] |
| Voltage gain | \[ A_V = \frac{V_o}{V_i} \] | \[ \frac{g_m (R_o || R_D)}{1 + g_m R_{Si}} \] |
| Input resistance | \[ \frac{V_i}{I_i} \] | \[ \frac{1}{g_m} \] |
| Output resistance | \[ \frac{V_o}{I_o} \] | \[ R_D \] |
Comparison of 3 Basic Amplifiers

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Voltage Gain</th>
<th>Current Gain</th>
<th>Input Resistance</th>
<th>Output Resistance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Common Source</td>
<td>$A_v &gt; 1$</td>
<td>—</td>
<td>$\ast R_{TH}$</td>
<td>Moderate to high</td>
</tr>
<tr>
<td>Source Follower</td>
<td>$A_v \approx 1$</td>
<td>—</td>
<td>$\ast R_{TH}$</td>
<td>Low</td>
</tr>
<tr>
<td>Common Gate</td>
<td>$A_v &gt; 1$</td>
<td>$A_i \approx 1$</td>
<td>Low</td>
<td>Moderate to high</td>
</tr>
</tbody>
</table>

* Determined by biasing resistors

Cascode Configurations

All have the same purpose – to decouple the input terminal (of the bottom device) from capacitive feedback from the output by taking the output from a second device.

Bottom device: Current gain (no appreciable voltage gain)
Top device: Voltage gain (no current gain)

Combines common-emitter/source/cathode with common-base/gate/grid. Result is like a single common-emitter/source/cathode device with drastically reduced "Miller capacitance" from the output to the input.

Single devices with cascode like construction

Tetrode (tet for “4” terminal) vacuum tube adds a fourth grid called a “screen” to shield the grid and cathode from the anode

Similar MOSFET device incorporates a second gate. Useful for RF circuits.

JFET Amplifier Configurations

* For polarized [electrolytic] input coupling capacitor, the "+" should be oriented towards the most positive DC voltage. For example, if there is -2V on the gate, and -8V associated with $V_{in}$, then the capacitor orientation should be reversed as shown.

The input coupling cap for the common gate configuration will most often be a polarized electrolytic, since the impedance at the Source of the JFET is only $1/gm$ in parallel with $R_S$. 

6.101 Spring 2020 Lecture 6

37
Common Source JFET (bypassed source resistor)

\[ A_i = \frac{v_{out}}{v_{in}} = \frac{-g_m V_{gs} R_i}{v_{gs} + g_m v_{gs} R_S} = \frac{-g_m v_{gs} R_i}{v_{gs} [1 + g_m R_S]} \]

or \[ A_i = \frac{v_{out}}{v_{in}} = \frac{-g_m R_i}{1 + g_m R_S} \]

Common Drain Amplifier (Source Follower)

\[ A_i = \frac{v_{out}}{v_{in}} = \frac{g_m V_{gs} R_S}{v_{gs} + g_m v_{gs} R_S} = \frac{g_m V_{gs} R_S}{v_{gs} [1 + g_m R_S]} \]

\[ A_i = \frac{g_m R_S}{1 + g_m R_S} \]

Common Gate Amplifier

\[ A_i = \frac{v_{out}}{v_{in}} = \frac{v_{gs} - R_i}{g_m R_i + \frac{R_i}{R_S} + 1} \]

if \( R_i = 0 \), then \[ A_i = g_m R_i \]

Output Resistance – Source Follower

Remove \( R_S \) and replace it with a test AC voltage generator

Short the input signal \( V_i \) and replace it with its source resistance \( R_i \).

Solve for \( I_{test} \) which is a consequence of applying the test generator \( V_{test} \) and for \( V_{test} \) in terms of the hybrid-\( \pi \) parameters.

To correctly calculate the value of a bypass capacitor for \( R_S \), use the parallel combination of \( r_o \) and \( R_S \).

\[ r_o = \frac{V_{test}}{I_{test}} = -\frac{V_{gs}}{g_m V_{gs}} = \frac{1}{g_m} \]
Low Frequency Hybrid π Model

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Common Source</th>
<th>C Source with ( R_L )</th>
<th>Common Drain [Source Follower]</th>
<th>Common Gate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage Gain</td>
<td>( A_c = -\frac{g_m R_L}{1 + g_m R_s} )</td>
<td>( A_c = -\frac{g_m R_L}{1 + g_m R_s} )</td>
<td>( A_c = \frac{g_m R_L}{1 + g_m R_s + \frac{R_s}{R_L}} )</td>
<td>( A_c = -\frac{g_m R_L}{1 + g_m R_s + \frac{R_s}{R_L}} )</td>
</tr>
<tr>
<td>Current Gain</td>
<td>( I_{d1} )</td>
<td>( I_{d2} )</td>
<td>( I_{d3} )</td>
<td>( A_i = -\frac{g_m R_s}{g_m R_s + 1} )</td>
</tr>
<tr>
<td>Input Impedance</td>
<td>( R_{d1} )</td>
<td>( R_{d2} )</td>
<td>( R_{d3} )</td>
<td>( \frac{R_s}{g_m R_s + 1} )</td>
</tr>
<tr>
<td>Output Impedance</td>
<td>( R_{d1} )</td>
<td>( R_{d2} )</td>
<td>( R_{d3} )</td>
<td>( \frac{R_s}{g_m R_s + 1} )</td>
</tr>
<tr>
<td>Phase Reversal?</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
</tr>
</tbody>
</table>

OK, now what can we do with these things?

This schematic from the now obsolete Intersil 7662 datasheet shows how a “flying capacitor” generates a negative voltage from a positive voltage. Slightly different connections can double a voltage instead of inverting it.

Source Follower

\[
v_i = R_i i_d
\]
\[
i_d = g_m v_s = g_m (v_g - v_i)
\]
\[
v_s = \frac{R_i g_m}{1 + R_i g_m} v_g
\]
A JFET follower using matched (dual) JFET's. The bottom JFET automatically generates just the right amount of current to bias the top one so Vin is approximately equal to Vout.

\[ R_1 = R_2 \text{ guarantees } V_{out} = V_{in} \text{ if } Q1 \text{ and } Q2 \text{ are matched.} \]

Horowitz Hill, 3rd Edition p160

The Dolby B noise reduction circuit used this circuit as a Variable attenuator. By adding \( \frac{1}{2} \) the drain voltage back to the gate voltage linearizes the JFET resistance.

\[
\frac{1}{r_{DS}} = 2k \left[ \left( V_{GS} - V_{th} \right) - \frac{V_{DS}}{2} \right]
\]

From An introduction to electronics, Cambridge Univ Press

n-Channel JFET Current Source
2N5459

P-Channel JFET Current Source
2N5462

\[ +15 \text{ V} \]

\[ I_{out} \]

\[ V_{DS} - \text{DRAIN-SOURCE VOLTAGE (V)} \]
Neat Circuit Ideas

Make a classic phase shift oscillator (3 stages of 60 deg phase shift each — any three digital logic inverters will usually do) so you can WATCH the oscillation run around the loop! Works with any odd number of stages.

Question: Is this guaranteed to start up? Why?

And what if you had a large (odd) number of stages — can you start a skinny pulse going around the loop? Will it stay skinny or widen and turn into 50-50% duty cycle?

Important basic power configuration

The H-bridge

Note how the high-side MOSFET's are driven by level shift. Four drive signals required. Note the trade-off in switching speed versus static power dissipation in level shifter. The 10k resistor will not turn off the IRF9230 very fast. But motor drives don’t operate at very high frequencies.

WHY MOSFETs FAIL

There are quite a few possible causes for device failures, here are a few of the most important reasons:

Over-voltage: MOSFETs have very little tolerance to over-voltage. Damage to devices may result even if the voltage rating is exceeded for as little as a few nanoseconds. MOSFET devices should be rated conservatively for the anticipated voltage levels and careful attention should be paid to suppressing any voltage spikes or ringing.

Prolonged current overload: High average current causes considerable thermal dissipation in MOSFET devices even though the on-resistance is relatively low. If the current is very high and heatsinking is poor, the device can be destroyed by excessive temperature rise. MOSFET devices can be paralleled directly to share high load currents.

Transient current overload: Massive current overload, even for short duration, can cause progressive damage to the device with little noticeable temperature rise prior to failure.

Shoot-through - cross conduction: If the control signals to two opposing MOSFETs overlap, a situation can occur where both MOSFETs are switched on together. This effectively short-circuits the supply and is known as a shoot-through condition. If this occurs, the supply decoupling capacitor is discharged rapidly through both devices every time a switching transition occurs. This results in very short but incredibly intense current pulses through both switching devices. Allow a dead time between switching transitions, during which neither MOSFET is turned on. This allows time for one device to turn off before the opposite device is turned on.

No free-wheel current path: When switching current through any inductive load (such as a Tesla Coil) a back EMF is produced when the current is turned off. It is essential to provide a path for this current to free-wheel in the time when the switching device is not conducting the load current. This current is usually directed through a free-wheel diode connected anti-parallel with the switching device. When a MOSFET is employed as the switching device, the designer gets the free-wheel diode "for free" in the form of the MOSFETs intrinsic body diode. This solves one problem, but creates a whole new one...
MOSFET failure modes continued

**Excessive gate drive:**
If the MOSFET gate is driven with too high a voltage, then the gate oxide insulation can be punctured rendering the device useless. Gate-source voltages in excess of +/- 15 volts are likely to cause damage.

The actual failure mechanism is usually you melt the clamping zener, and the puddle of molten silicon forms a short. The MOSFET may be fine, but the gate is now shorted to the source, which makes it kind of hard to use.

---

MOSFET failure modes continued

**Insufficient gate drive - incomplete turn on:**
MOSFET devices are only capable of switching large amounts of power because they are designed to dissipate minimal power when they are turned on. If the device is not fully turned on then the device will have a high resistance during conduction and will dissipate considerable power as heat.

The newer power parts have long been based on the latest digital process: i.e., they’re designed for 5V. Newer power MOSFET’s have guaranteed on resistance at lower Vgs voltages consistent with use in 3.3V logic inputs, and have Vds absolute maximum ratings of 6V or 7V, and similar abs max Vgs ratings. Modern logic requires lots of power conversion devices operating at these low voltages.

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For further reading and possible inspiration for your projects, read Jim Williams app notes! You gotta love a guy who titles an app note (#25):

**LINEAR TECHNOLOGY**

*Application Note 25*

*September 1987*

*Switching Regulators for Poets*
*A Gentle Guide for the Trepidacious*

-Jim Williams

The above title is not happenstance and was arrived at after considerable deliberation… Mysterious modes, sudden, seemingly inexplicable failures, peculiar regulation characteristics and just plain explosions are common occurrences. Diodes conduct the wrong way. Things get hot that shouldn’t. Capacitors act like resistors, fuses don’t blow and transistors do. The output is at ground, and the ground terminal shows volts of noise. Added to this poisonous brew is the regulator’s feedback loop, sampled in nature and replete with uncertain phase shifts. Everything, of course, varies with line and load conditions— and the time of day, or so it seems. In the face of such menace, what are Everyman and the poets to do?
Analog Drawing Board
Nicholas Klugman & Henry Love