- MOSFET
- Op Amps
- 741, 356
- Imperfections
- Op-amp applications

Acknowledgements:
Ron Roscoe,
Neamen, Donald: Microelectronics Circuit Analysis and Design, 3rd Edition

◄ February

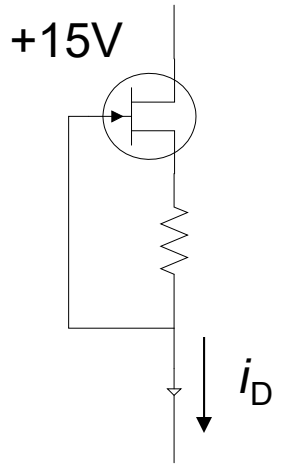
March 2020

April ►

Sun	Mon	Tue	Wed	Thu	Fri	Sat
1	2	3	4	5 Lab 4	6 Add date	7
8 Daylight savings	9	10	11 Pizza 6:30	12 Lab 5	13	14
15	16	17 Quiz Review	18	19 Quiz	20	21
22	23 Spring break	24 Spring break	25 Spring break	26 Spring break	27 Spring break	28

JFET Application Current Source

- Household application: battery charger (car, laptop, mp3 players)
- Differential amplifier current source
- Ramp waveform generator
- High Speed DA converter using capacitors
- Simple circuit: 2N5459 Nchannel JFET



I_{DSS} = current with V_{GS}=0

V_P = pinchoff voltage

$$i_D = I_{DSS}\left(1 - \frac{v_{GS}}{V_P}\right)^2$$

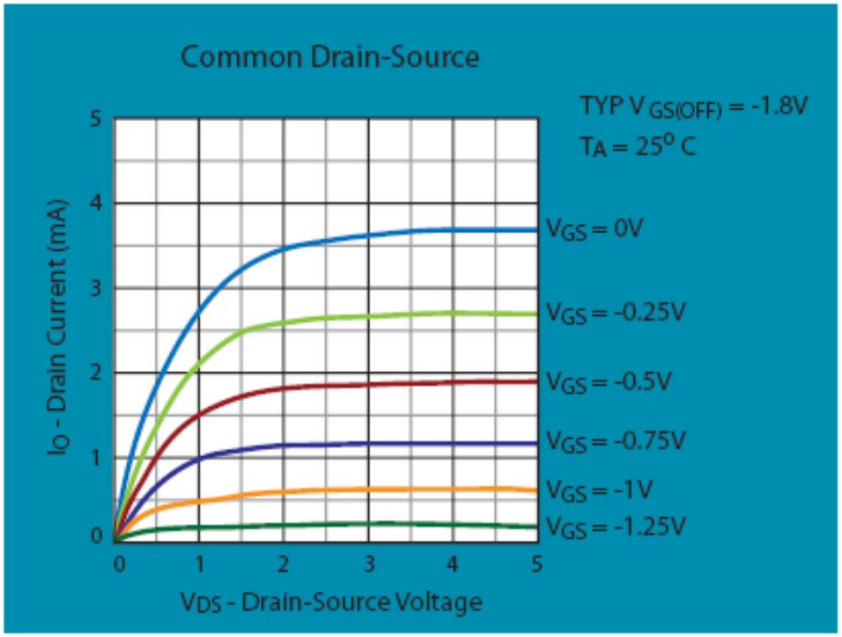
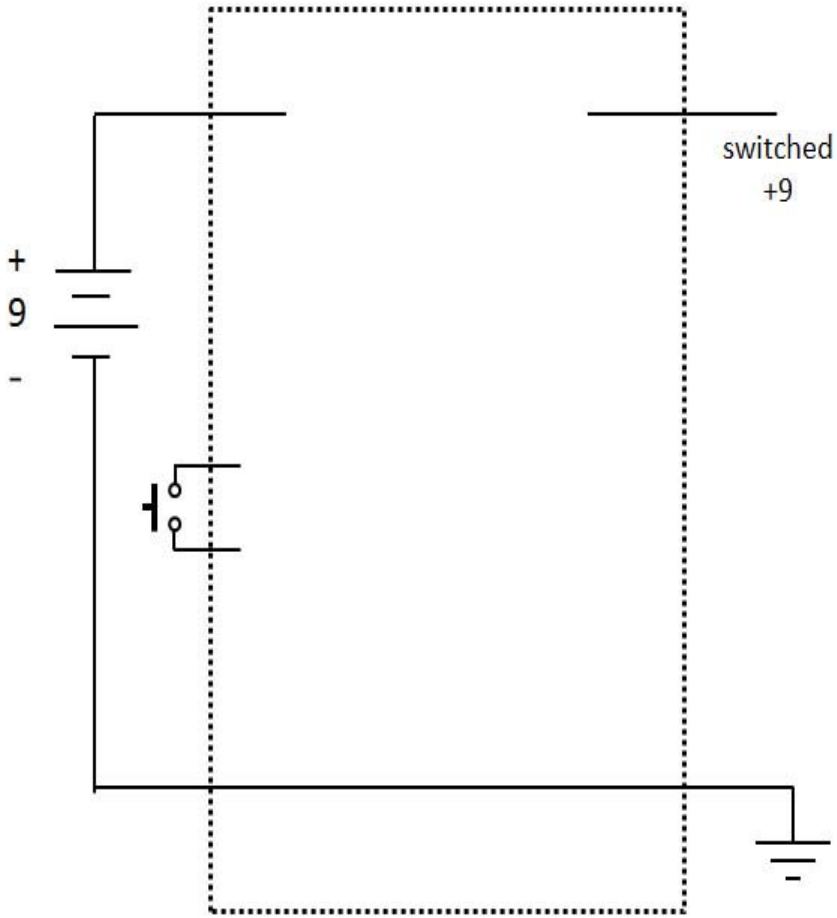


Figure by MIT OpenCourseWare.

2017 Quiz Design Question



Design a circuit such that when a momentary push button switch is closed, "switched 9v" will be supplied to your design under test for exactly two minutes.

You have available a 2N7000 (n-channel MOSFET) and a ZVP2106A which is a p-channel complement to the 2N7000.

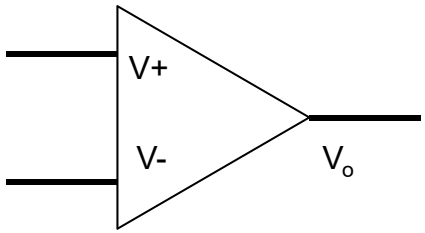
You have a 100uf capacitor that is exactly 100uf with negligible leakage current.

Based on measurements, your 2N7000 has a V_{GS}(th) 3.0 volts and the ZVP2106A has a V_{GS}(th) -3.0.

The 9V battery is a constant 9V during the test.
ln(.3333) = -1.0986
ln(.2222) = -1.5041
ln(.1111) = -2.1972 [one or more of these constants may be required for your design]

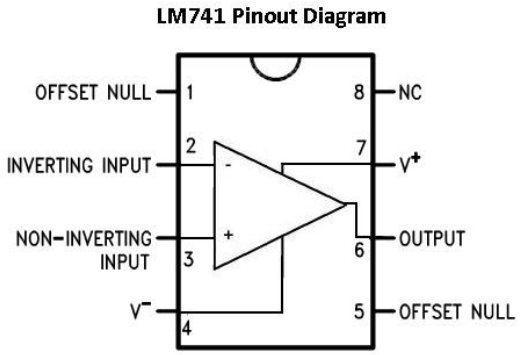
Op-Amps

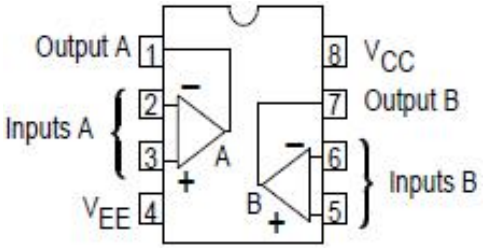
- Active device: $V_0 = a(V_+ - V_-)$; note that it is the difference of the input voltage!



- a=open loop gain ~ $10^5 - 10^6$
- Most applications use negative feedback.
- Comparator: no feedback
- Active device requires power. No shown for simplicity.
- Classics op-amps: 741, 357 ~ $0.20; one, two or four in a package.
- Newer op-amps operate at <3.3V (OPA369 1.8V)

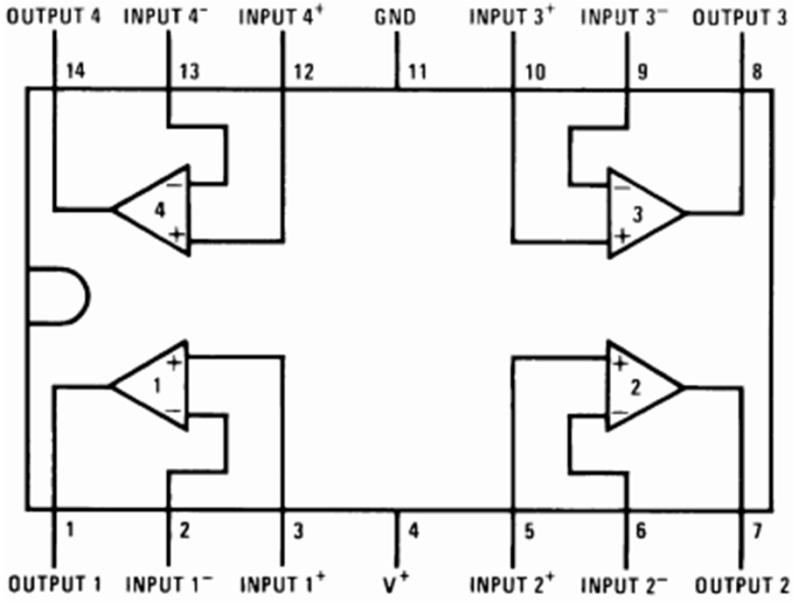
Op-Amp Packaging



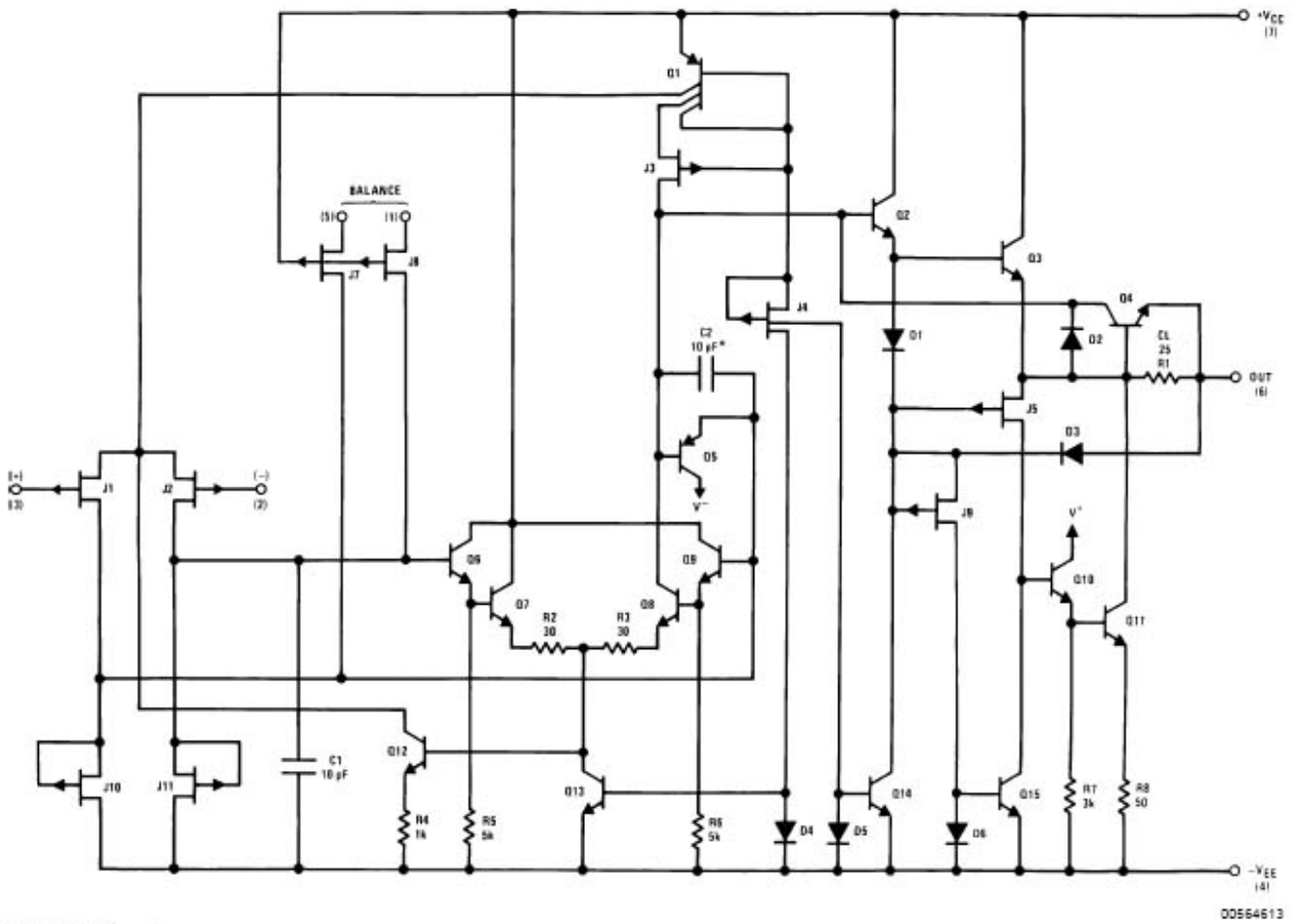


LF353

LM324

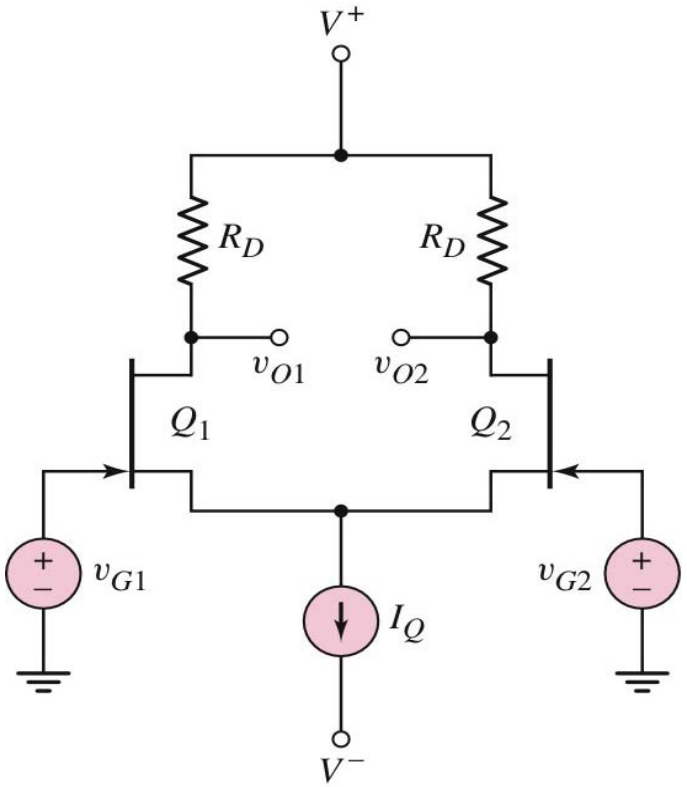


356 JFET Input Op-amp

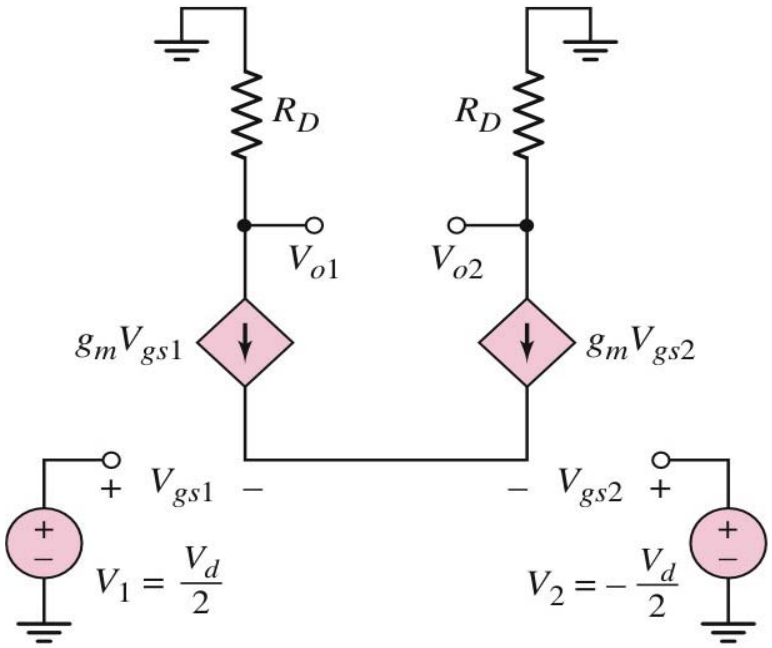


*C = 3pF in LF357 series.

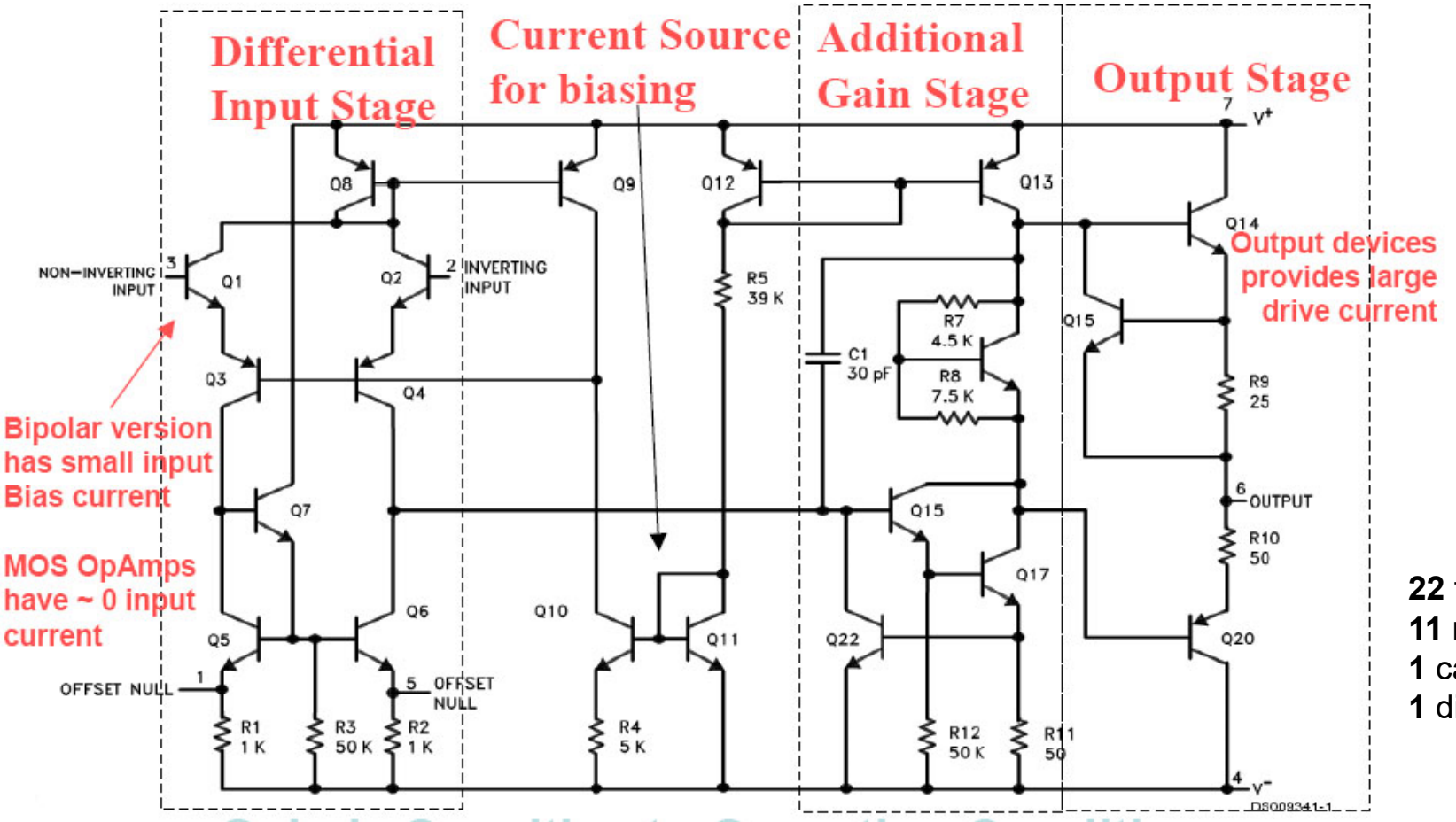
JFET Differential Pair



Small Signal Model

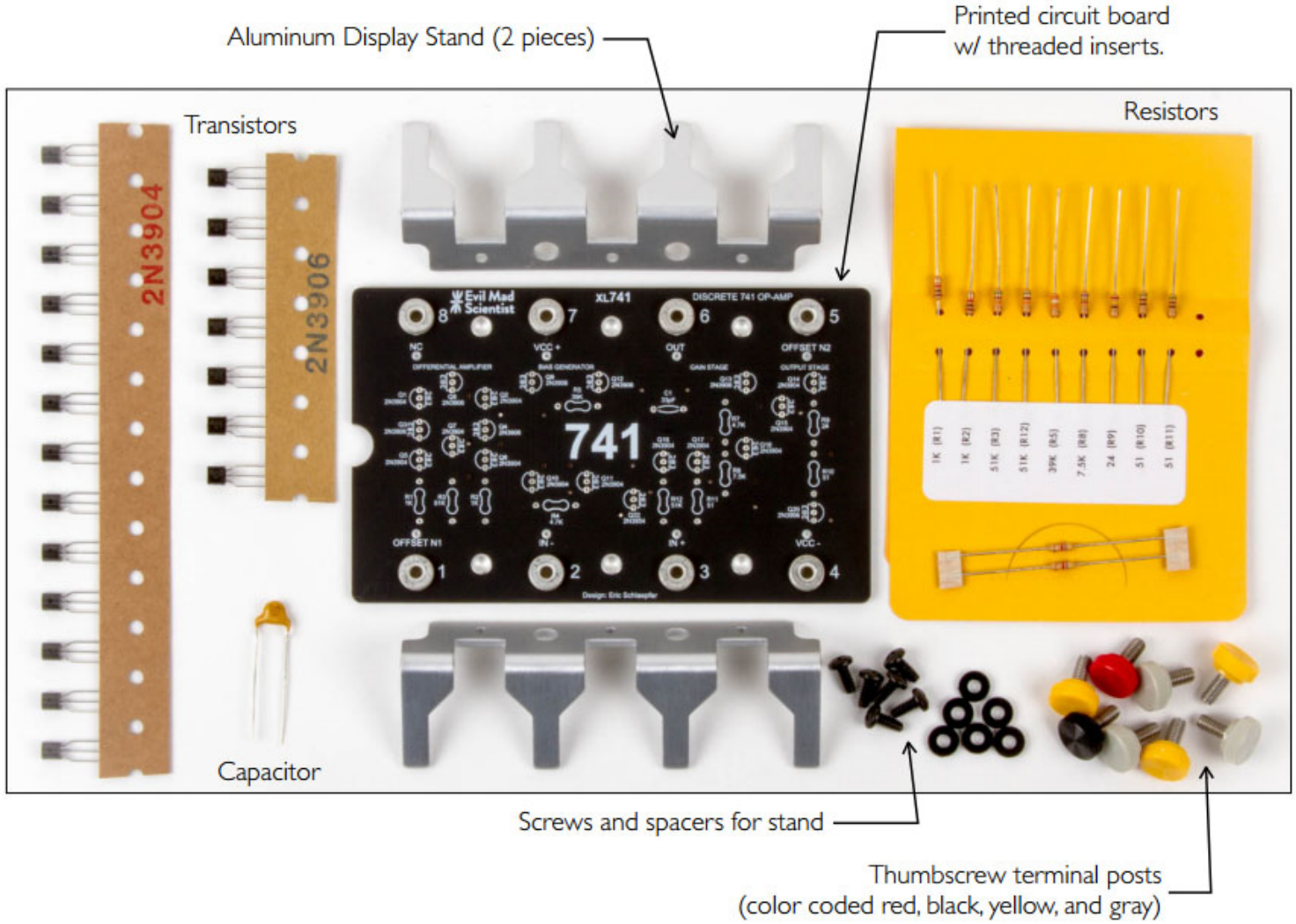


741 Circuit



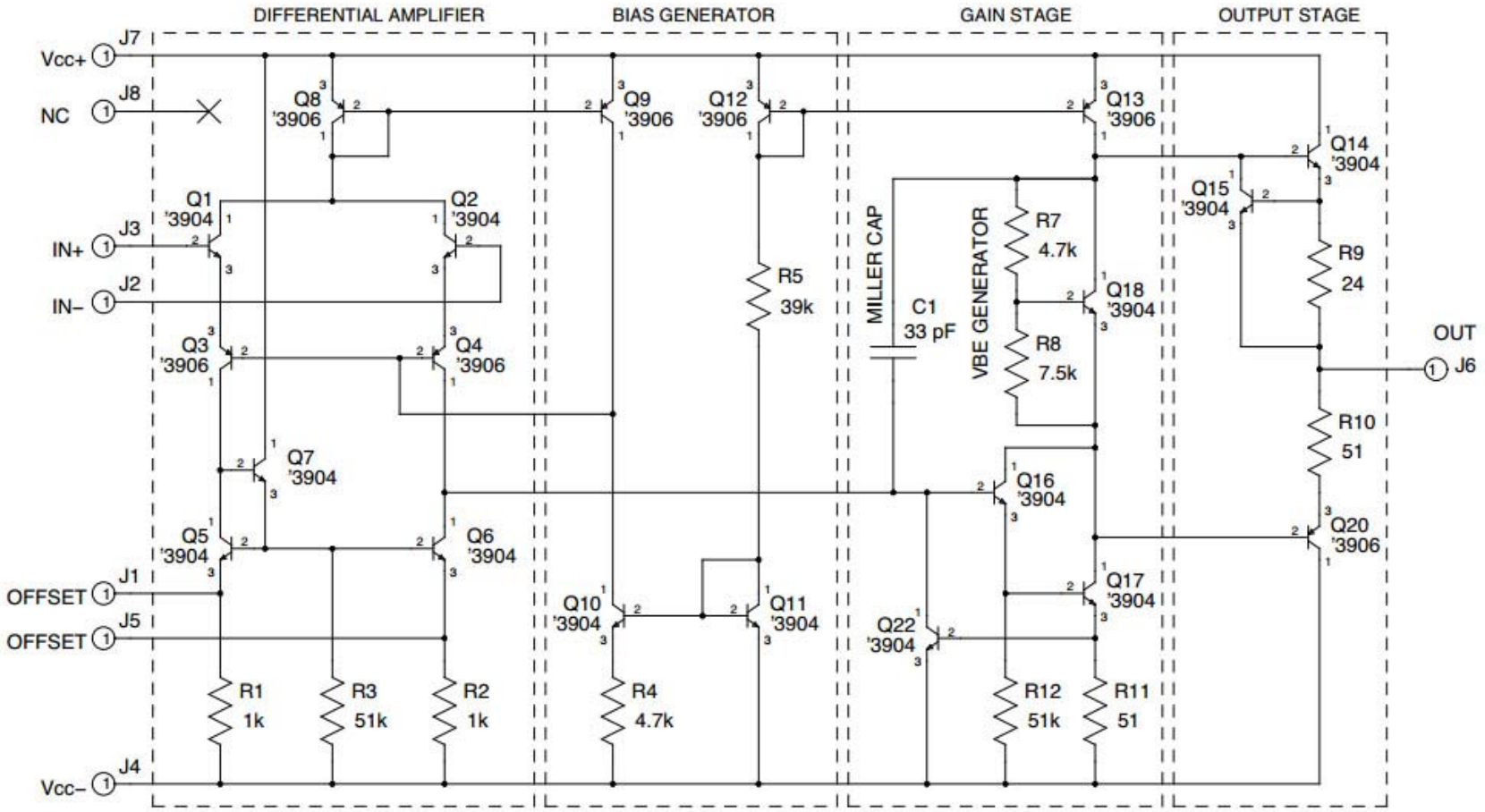
22 transistors,
11 resistors,
1 capacitor,
1 diode

Discrete 741



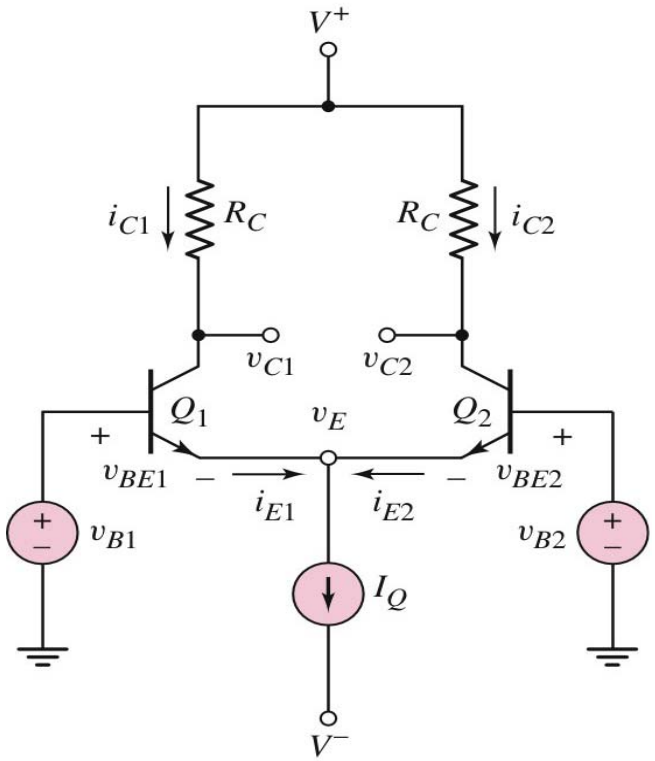
Discrete 741

Schematic Diagram

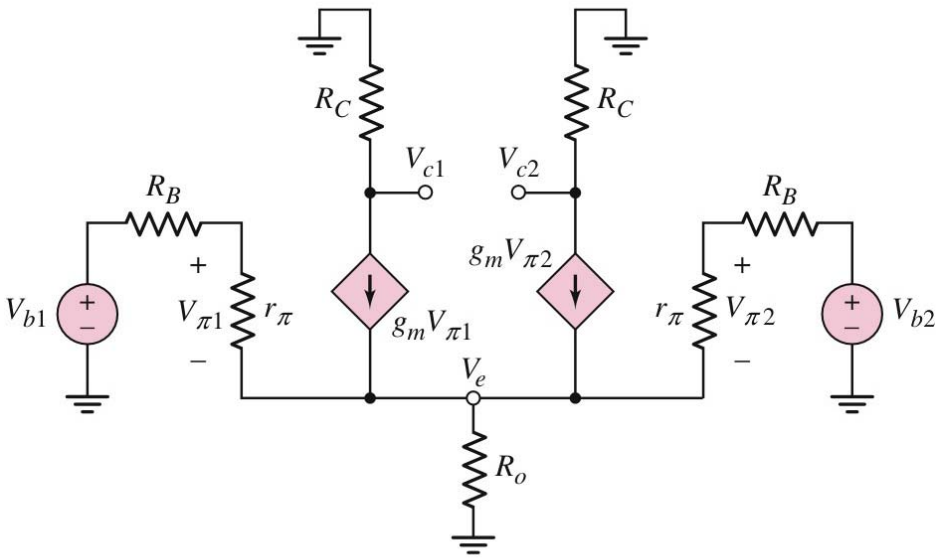


Differential (Emitter Coupled) Pair

BJT Diff Pair

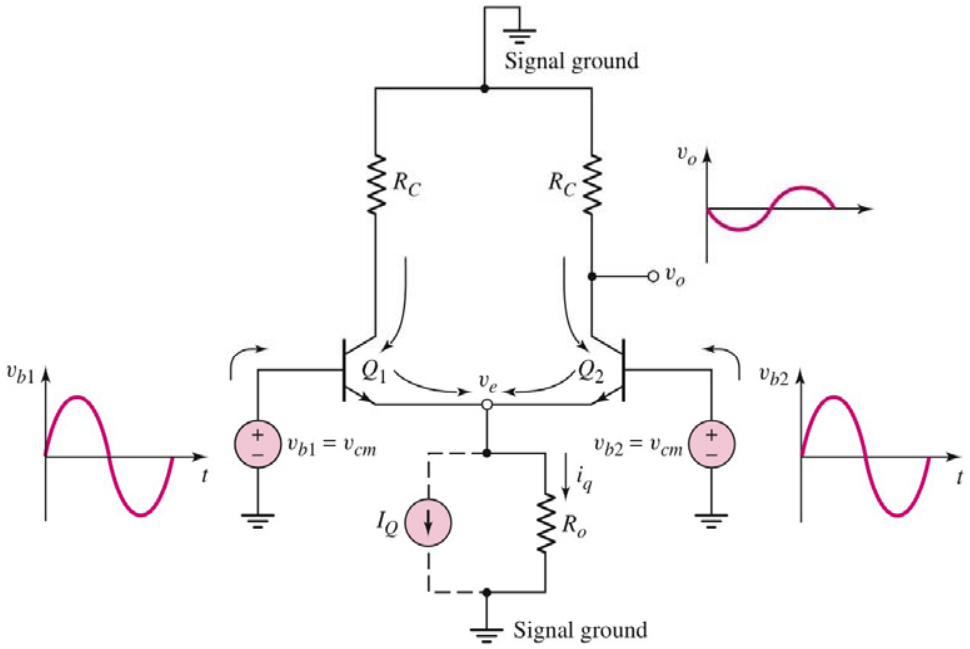


Small Signal Model

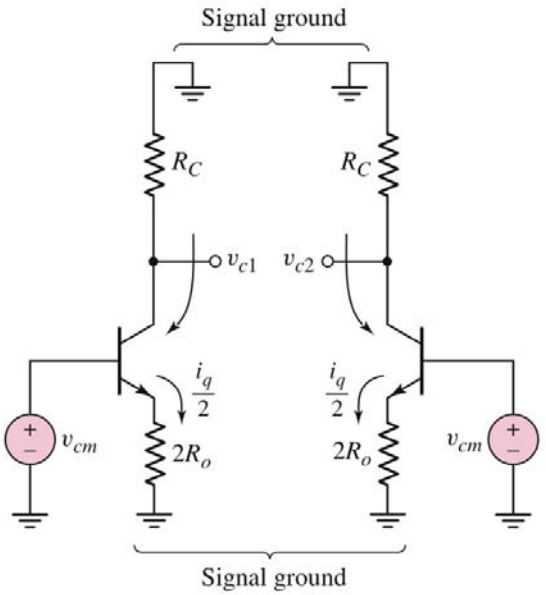


Differential Pair – Common Mode Voltage

Small Signal Model

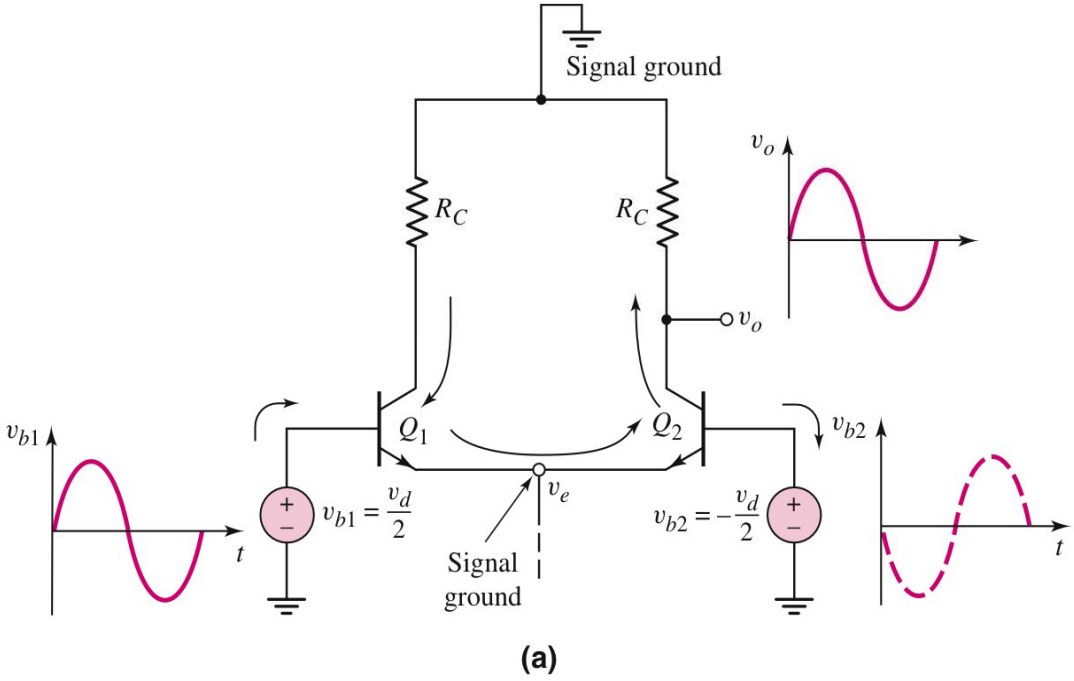


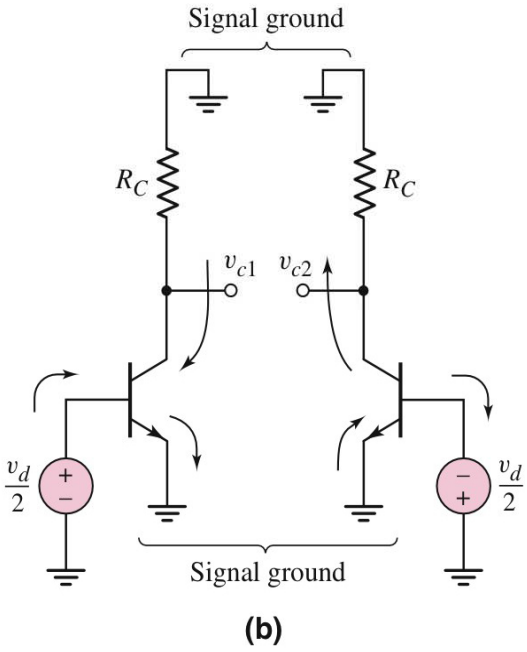
(a)



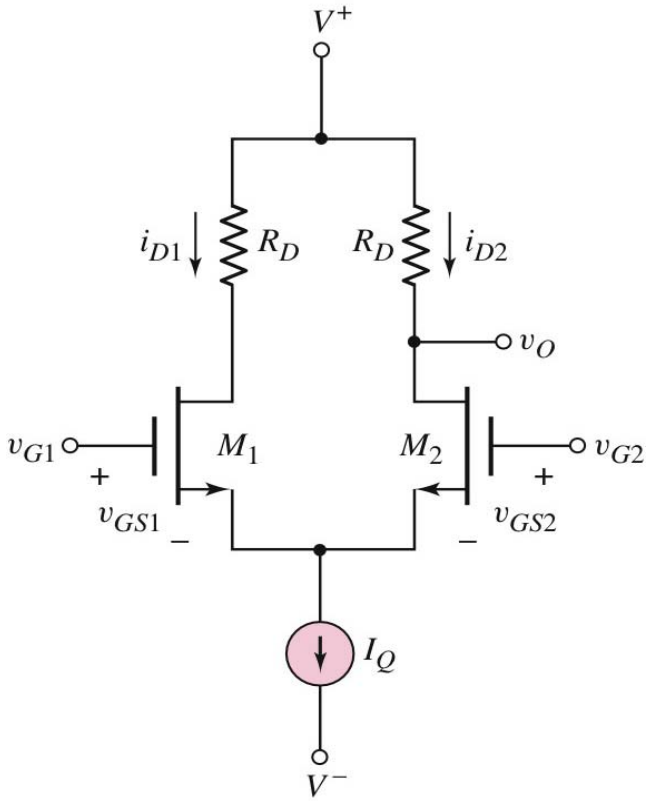
(b)

Differential Pair – Differential Mode Voltage

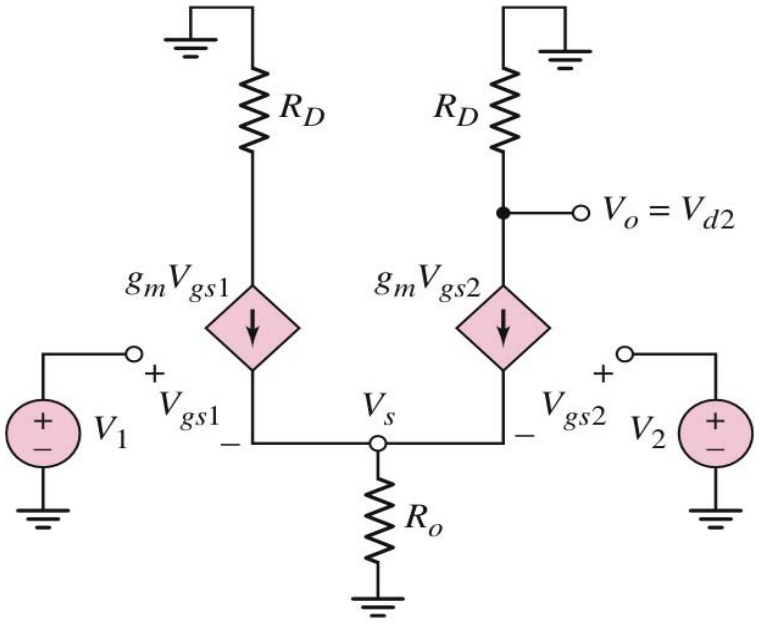




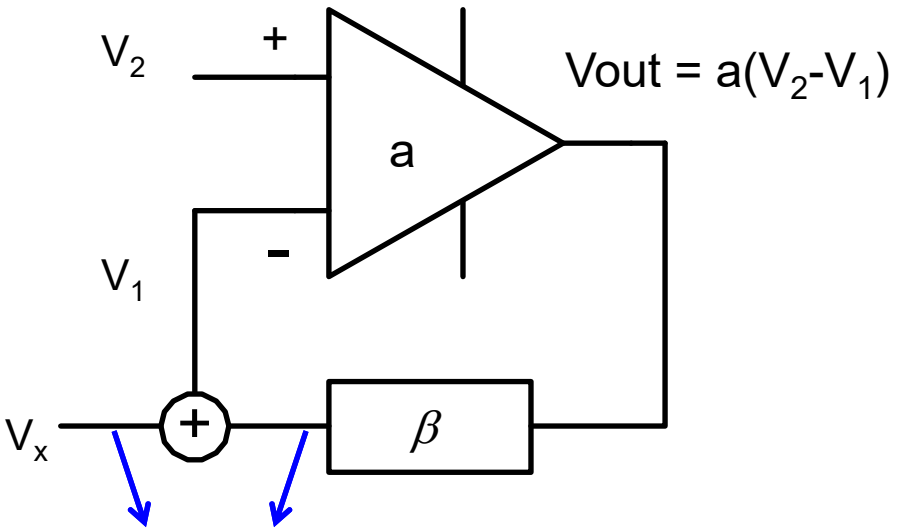
MOSFET Differential Pair



Small Signal Model



Virtual Node Analysis



$$V_1 = V_x + \beta V_{out}$$

$$V_1 = V_x + a\beta V_2 - a\beta V_1$$

$$V_1(1 + a\beta) = V_x + a\beta V_2$$

$$V_1 = V_x\left(\frac{1}{1+a\beta}\right) + \left(\frac{a\beta}{1+a\beta}\right)V_2 \approx V_2$$

a = gain
β = feedback or loop function

- If a>>1 and a>> β then v1 ~ v2
- Current into input terminals zero by design
- Typical values:
  a~100,000 & a β >>1
- ok for a=a(s) and β = β(s) as long as a(s) β(s) >> 1
- β is the loop transfer function
  (not to be confused of β of a BJT)
- a β is the loop gain

Op Amps – Virtual Node

- With negative feedback, output will drive the input voltage difference to zero => $V_+ = V_-$
- Input current = 0

Benefits of Feedback

Stabilize gain against device variations, temperature, aging	Reduce distortion by the feedback factor [(1+aβ)]
Input and output impedances adjusted by (1+aβ)	Gain determined by passive components

Disadvantages of Feedback

Loss of gain; need more stages	Greater tendency for instability (oscillations)

$$V_1 = V_x\left(\frac{1}{1+a\beta}\right)+\left(\frac{a}{1+a\beta}\right)V_2 \approx V_2$$

741 Op Amp Max Ratings

common mode voltage appears at both inputs

Need +Vcc, -Vee for operation

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}, V_{EE}	±18	Vdc
Input Differential Voltage	V_{ID}	±30	V
Input Common Mode Voltage (Note 1.)	V_{ICM}	±15	V
Output Short Circuit Duration (Note 2.)	t_{SC}	Continuous	–
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C

1. For supply voltages less than +15 V, the absolute maximum input voltage is equal to the supply voltage.
2. Supply voltage equal to or less than 15 V.

Idiot proof

741 Electrical Characteristics

Almost zero

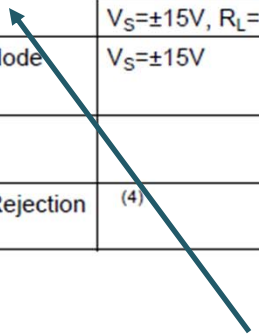
ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S \le 10$ k)	V_{IO}	–	2.0	6.0	mV
Input Offset Current	I_{IO}	–	20	200	nA
Input Bias Current	I_{IB}	–	80	500	nA
Input Resistance	r_i	0.3	2.0	–	MΩ
Input Capacitance	C_i	–	1.4	–	pF
Offset Voltage Adjustment Range	V_{IOR}	–	±15	–	mV
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	V
Large Signal Voltage Gain (V_O = ±10 V, $R_L \ge 2.0$ k)	A_{VOL}	20	200	–	V/mV
Output Resistance	r_o	–	75	–	Ω
Common Mode Rejection ($R_S \le 10$ k)	CMR	70	90	–	dB
Supply Voltage Rejection ($R_S \le 10$ k)	PSR	75	–	–	dB
Output Voltage Swing ($R_L \ge 10$ k) ($R_L \ge 2.0$ k)	V_O	 ±12 ±10	 ±14 ±13	 – –	V
Output Short Circuit Current	I_{SC}	–	20	–	mA
Supply Current	I_D	–	1.7	2.8	mA
Power Consumption	P_C	–	50	85	mW
Transient Response (Unity Gain, Noninverting) (V_I = 20 mV, $R_L \ge$ 2.0 k, $C_L \le$ 100 pF) Rise Time (V_I = 20 mV, $R_L \ge$ 2.0 k, $C_L \le$ 100 pF) Overshoot (V_I = 10 V, $R_L \ge$ 2.0 k, $C_L \le$ 100 pF) Slew Rate	 t_{TLH} os SR	 – – –	 0.3 15 0.5	 – – –	 µs % V/µs

LF356

DC Electrical Characteristics

Symbol	Parameter	Conditions	LF155/6			LF256/7 LF356B			LF355/6/7			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S=50Ω, T_A=25°C		3	5		3	5		3	10	mV
		Over Temperature			7			6.5			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S=50Ω		5			5			5		µV/°C
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	R_S=50Ω, (2)		0.5			0.5			0.5		µV/°C per mV
I_{OS}	Input Offset Current	T_J=25°C, (1) (3)		3	20		3	20		3	50	pA
		$T_J \leq T_{HIGH}$			20			1			2	nA
I_B	Input Bias Current	T_J=25°C, (1) (3)		30	100		30	100		30	200	pA
		$T_J \leq T_{HIGH}$			50			5			8	nA
R_{IN}	Input Resistance	T_J=25°C		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S=±15V, T_A=25°C	50	200		50	200		25	200		V/mV
		V_O=±10V, R_L=2k										
		Over Temperature	25			25			15			V/mV
V_O	Output Voltage Swing	V_S=±15V, R_L=10k	±12	±13		±12	±13		±12	±13		V
		V_S=±15V, R_L=2k	±10	±12		±10	±12		±10	±12		V
V_{CM}	Input Common-Mode Voltage Range	V_S=±15V	±11	+15.1		±11	±15.1		+10	+15.1		V
				−12			−12			−12		V
CMRR	Common-Mode Rejection Ratio		85	100		85	100		80	100		dB
PSRR	Supply Voltage Rejection Ratio	(4)	85	100		85	100		80	100		dB



not rail to rail

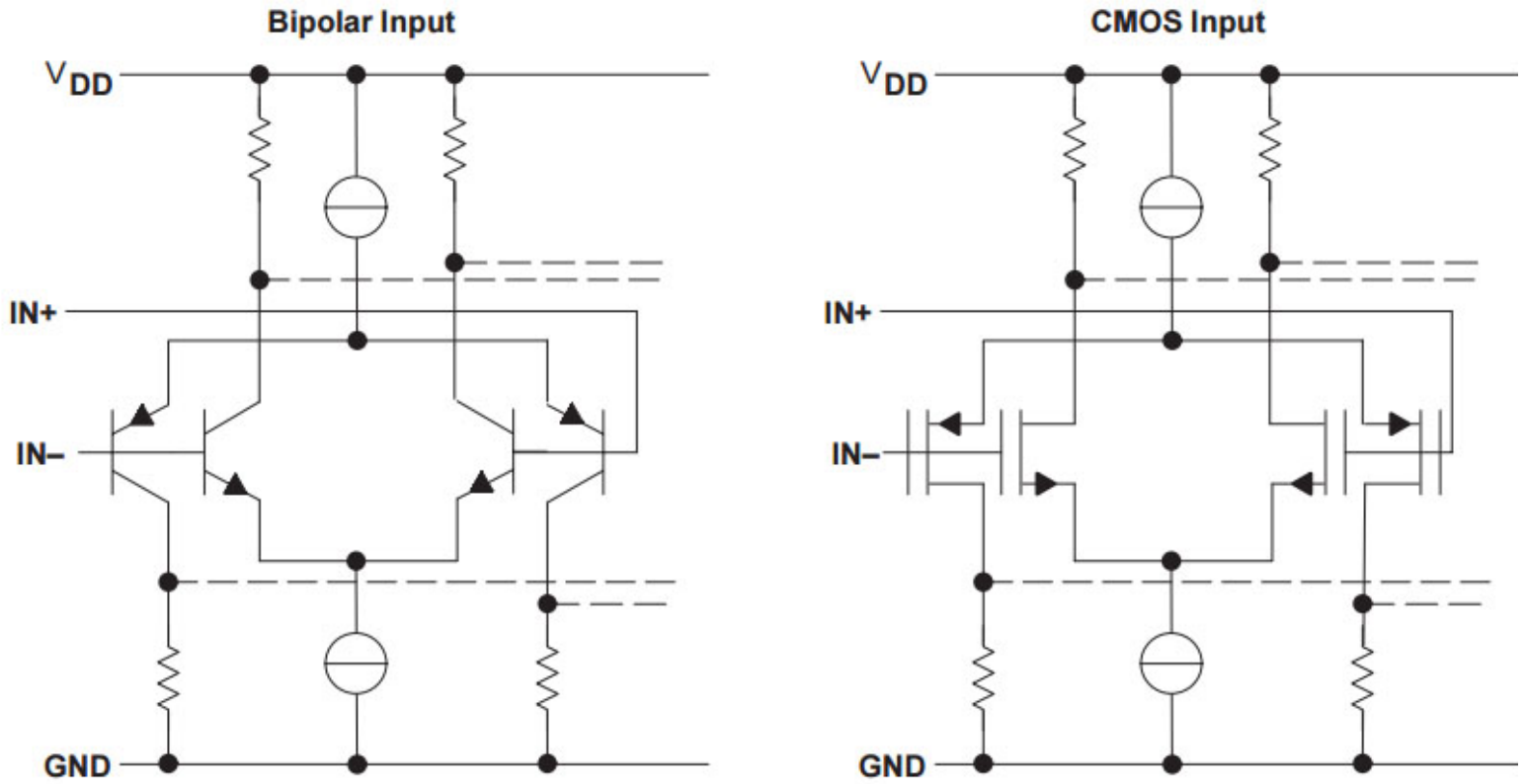
LM6132 – Rail to Rail Output

6.6 5.0V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for V^+ = 5.0V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and R_L > 1 MΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes

	PARAMETER	TEST CONDITIONS	TYP (1)	LM6134AI LM6132AI LIMIT (2)	LM6134BI LM6132BI LIMIT (2)	UNIT
V_{OS}	Input Offset Voltage		0.25	2 **4**	6 **8**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		**5**			µV/C
I_B	Input Bias Current	0V ≤ V_{CM} ≤ 5V	110	140 **300**	180 **350**	nA max
I_{OS}	Input Offset Current		3.4	30 **50**	30 **50**	nA max
R_{IN}	Input Resistance, CM		104			MΩ
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 4V	100	75 **70**	75 **70**	dB min
		0V ≤ V_{CM} ≤ 5V	80	60 **55**	60 **55**	
PSRR	Power Supply Rejection Ratio	±2.5V ≤ V^+ ≤ ±12V	82	78 **75**	78 **75**	dB min
V_{CM}	Input Common-Mode Voltage Range		−0.25 5.25	**0** **5.0**	**0** **5.0**	V
A_V	Large Signal Voltage Gain	R_L = 10k	100	25 **6**	15 **6**	V/mV min
V_O	Output Swing	100k Load	4.992	4.98 **4.93**	4.98 **4.93**	V min
			0.007	0.017 **0.019**	0.017 **0.019**	V max
		10k Load	4.952	4.94 **4.85**	4.94 **4.85**	V min
			0.032	0.07 **0.09**	0.07 **0.09**	V max
		5k Load	4.923	4.90 **4.85**	4.90 **4.85**	V min
			0.051	0.095 **0.12**	0.095 **0.12**	V max

Rail to Rail Input



Decibel (dB)

$$dB = 20\log\left(\frac{V_o}{V_i}\right) \qquad dB = 10\log\left(\frac{P_o}{P_i}\right)$$

$\log_{10}(2)=.301$

3 dB point = half power point

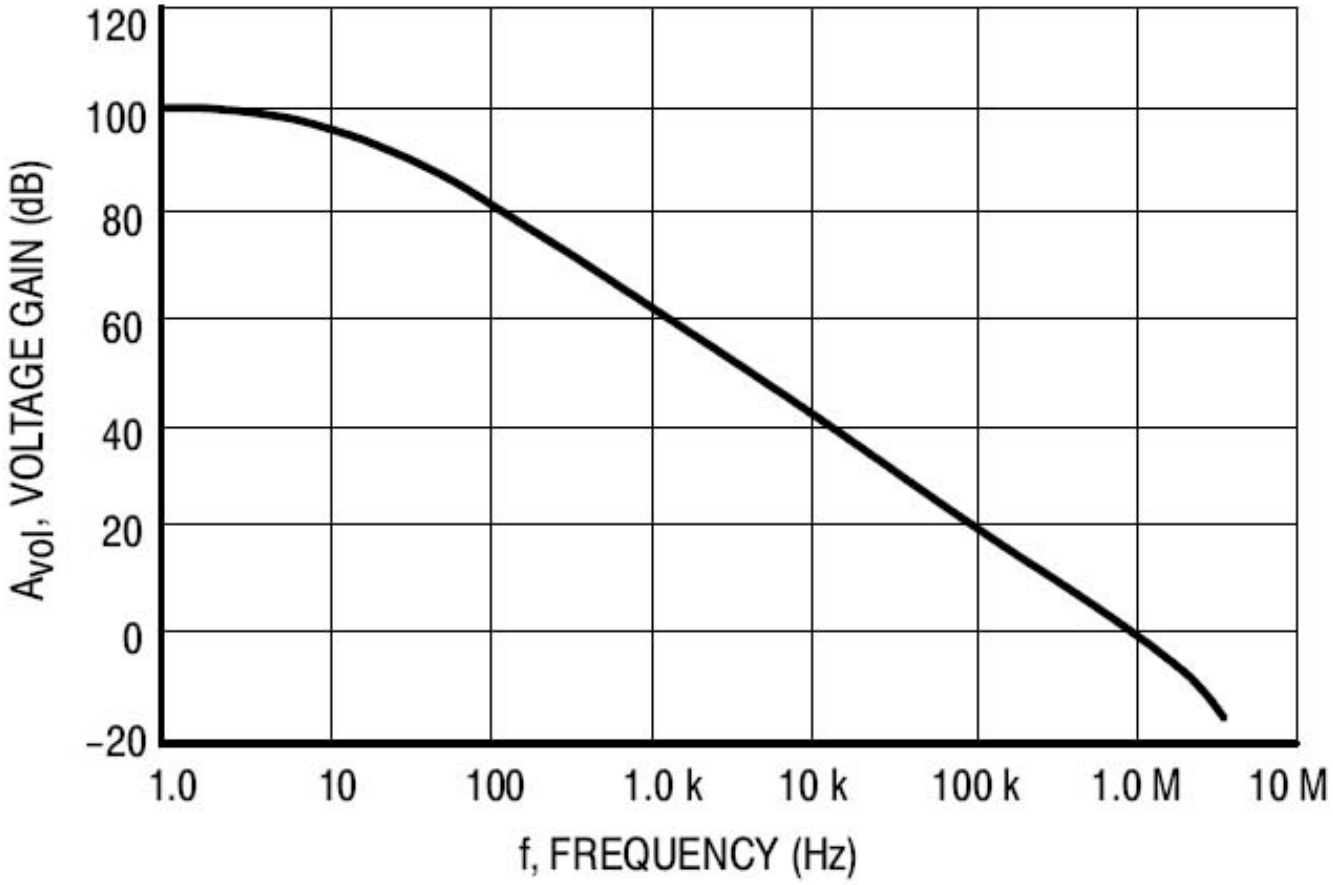
100 dB = 100,000 = 10^5

80 dB = 10,000 = 10^4

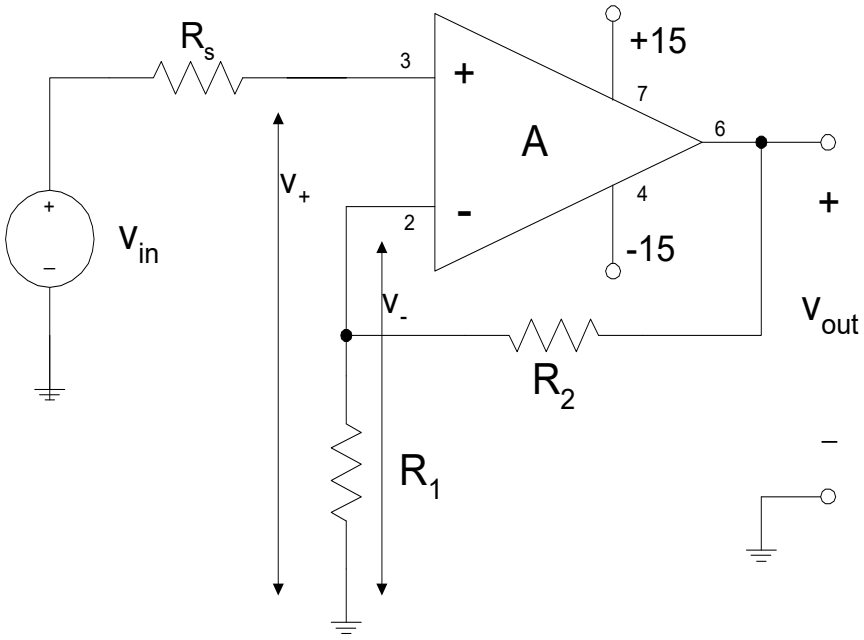
60 dB = 1,000 = 10^3

40 dB = 100 = 10^2

741 Open Loop Frequency Gain



Non-Inverting Amplifer



Zero input current;

therefore $v_+ = v_{in}$

$$v_- = \frac{R_1}{R_1 + R_2} \times v_{out} \quad but \; v_+ = v_-$$

$$so \; v_{in} = \frac{R_1}{R_1 + R_2} \times v_{out};$$

$$\frac{v_{out}}{v_{in}} = \frac{R_1 + R_2}{R_1}$$

$$or \; A_v = 1 + \frac{R_2}{R_1}$$

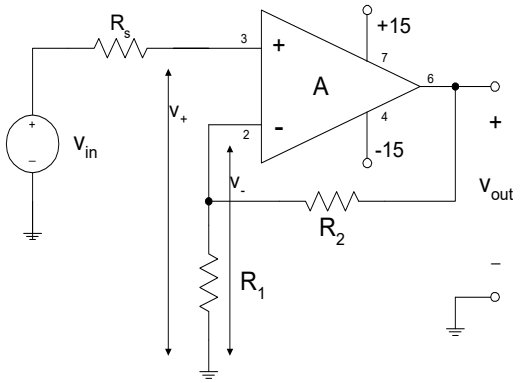
β (not to be confused with β of a BJT)

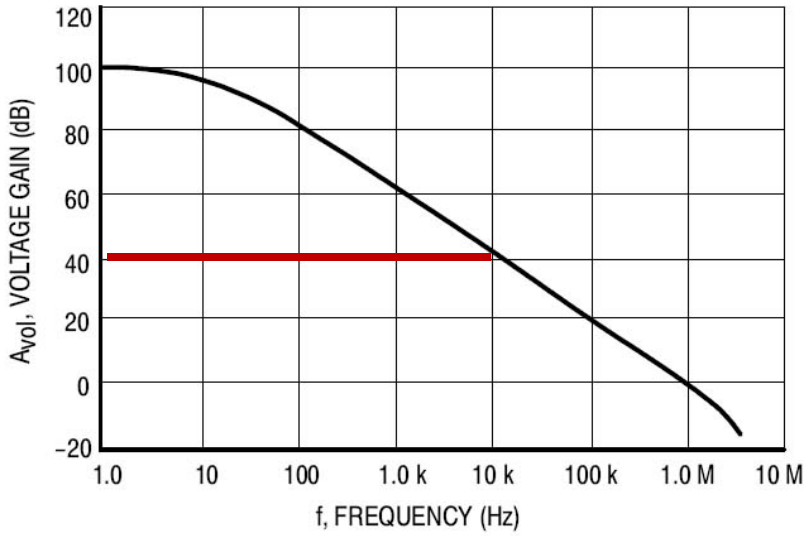
for finite A

$$\beta = \frac{R_1}{R_1 + R_2}$$

$$\frac{v_{out}}{v_{in}} = A_v = \frac{A}{1 + A\beta}$$

741 Open Loop Frequency Gain





Examples at 1 Hz, 1000 Hz, and 10kHz

Voltage gain A_v=40dB = 100; R_2= 100kΩ, R_1= 1kΩ; [101 = 40.1dB!] β=0.01

At 1 Hz, A_{vol} = 100 dB = 1 x 10^5 = 100,000.

$$A_v = \frac{A}{1+A\beta} = \frac{10^5}{1+10^5 \times .01} = \frac{10^5}{10^3} = 100 = 40dB$$

At 1000 Hz, A_{vol} = 60 dB = 10^3 = 1000.

$$A_v = \frac{A}{1+A\beta} = \frac{10^3}{1+10^3 \times .01} = \frac{10^3}{1+10} = \frac{1000}{11} = 90.9 = 39.2\ dB$$

At 10 kHz, A_{vol} = 42 dB = 1.26 x 10^2 = 126.

$$A_v = \frac{A}{1+A\beta} = \frac{126}{1+126 \times .01} = \frac{126}{1+1.26} = \frac{126}{2.26} = 55.8 = 34.9dB$$

β is the loop transfer function

aβ is the loop gain

741 vs 356 Comparison

	741	356
Input device	BJT	JFET
Input bias current	0.5uA	0.0001uA
Input resistance	0.3 MΩ	10^6 MΩ
Slew rate*	0.5 v/μs	7.5 v/μs
Gain Bandwidth product	1 Mhz	5 Mhz
Output short circuit duration	continuous	continuous
Identical pin out		

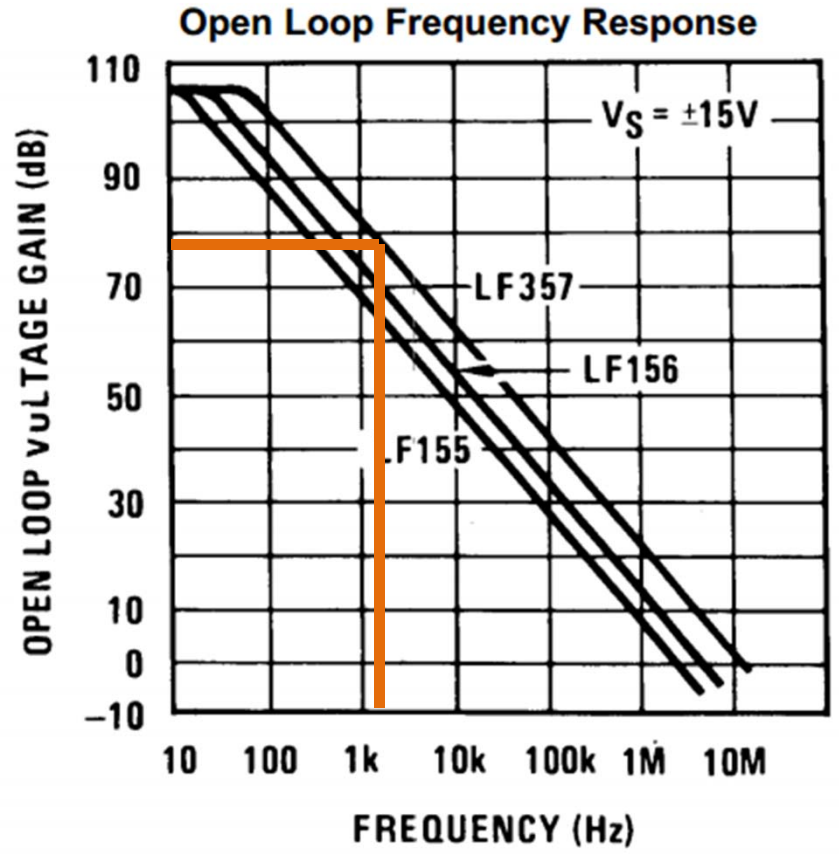
* comparators have >50 v/μs slew rate

So Why BJT in Op-amps?

BJTs have higher transconductance (gain), better consistency in spec between pieces, and in some applications, lower noise than FETs.

Like most JFET op amps, the LF356 has a relatively high offset voltage, and relatively high drifts. BJT op-amps tend to have much lower offset voltage and drifts.

Gain Bandwidth Product = Constant
(No free lunch)



Gain: 60dB = 10^3
Bandwidth = $5x10^3$

Gain Bandwidth product = $5x10^6$

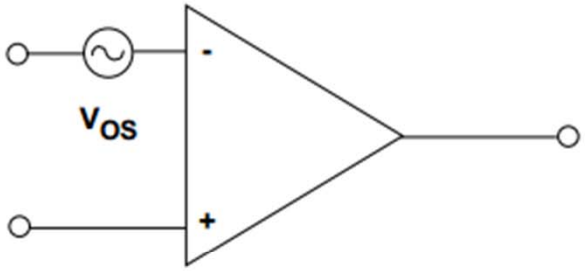
Op-Amp Imperfections – Real World

- Input offset voltage
- Input Current Bias
- Input Offset Current
- Finite Output Voltage Swing
- Finite Current
- Finite Gain, gain bandwidth product
- Voltage Noise – Johnson Noise
- Phase Shifts
- Slew Rate

Input Offset Voltage *

DEFINITION OF INPUT OFFSET VOLTAGE

Ideally, if both inputs of an op amp are at exactly the same voltage, then the output should be at zero volts. In practice, a small differential voltage must be applied to the inputs to force the output to zero. This is known as the *input offset voltage*, V_{OS}. Input offset voltage is modeled as a voltage source, V_{OS}, in series with the inverting input terminal of the op amp as shown in Figure 1.



- **Offset Voltage: The differential voltage which must be applied to the input of an op amp to produce zero output.**
- **Ranges:**
  - **Chopper Stabilized Op Amps: <1μV**
  - **General Purpose Precision Op Amps: 50-500μV**
  - **Best Bipolar Op Amps: 10-25μV**
  - **Best JFET Input Op Amps: 100-1,000μV**
  - **High Speed Op Amps: 100-2,000μV**
  - **Untrimmed CMOS Op Amps: 5,000-50,000μV**
  - **DigiTrim™ CMOS Op Amps: <100μV-1,000μV**

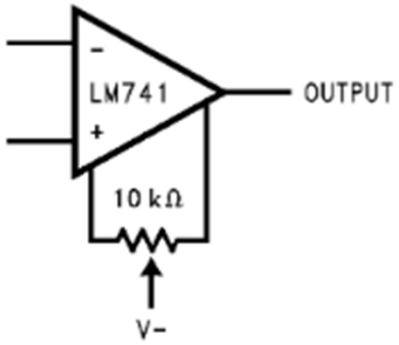
Figure 1: Typical Op Amp Input Offset Voltage

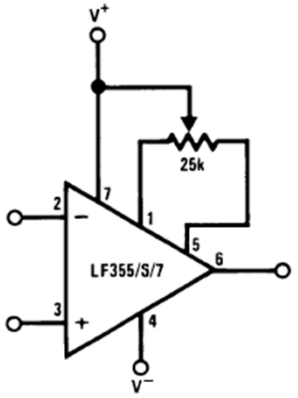
741: 6000μv
357: 10,000μv

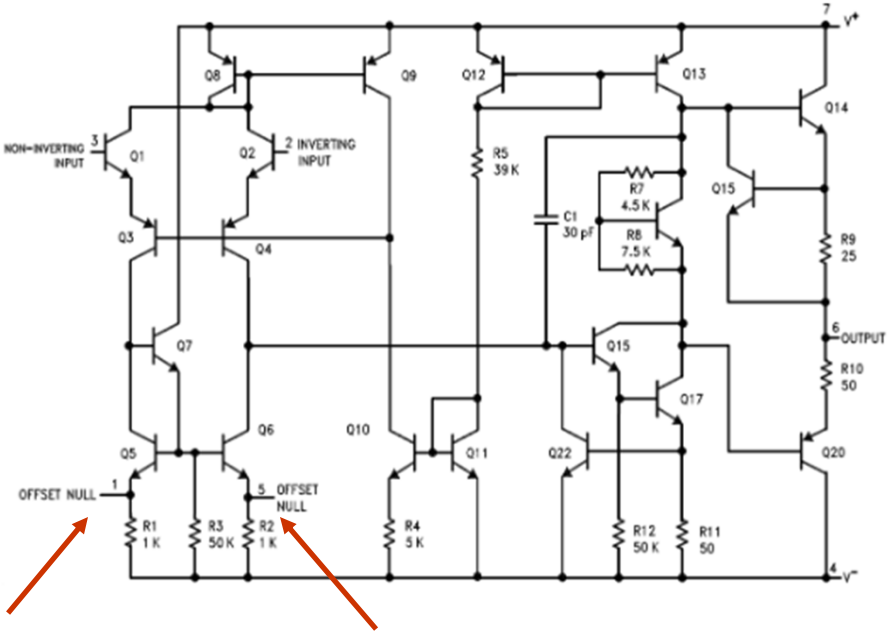
Current technology:
10μv

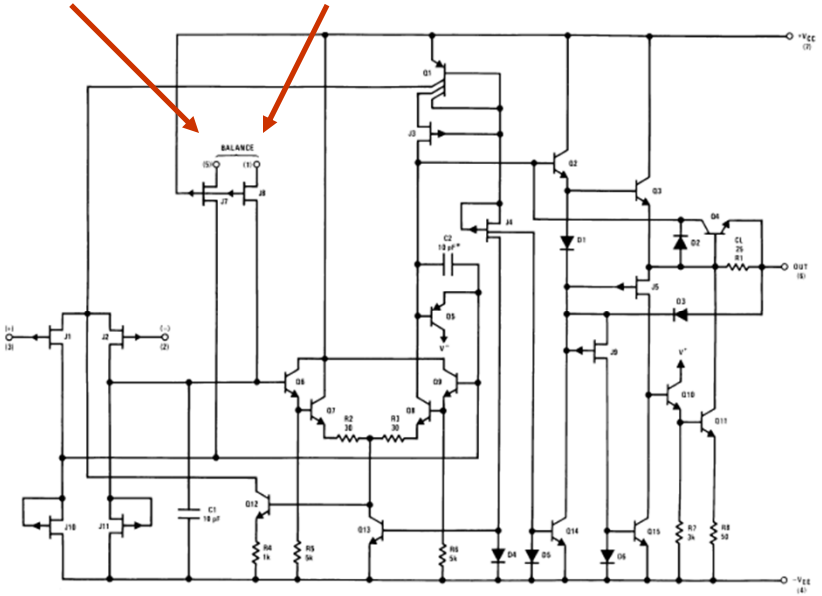
* Analog Devices MT-037 Tutorial

Offset Adjustments







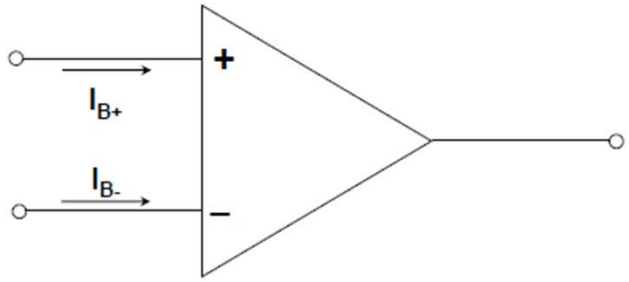


C = 3pF in LF357 series.

Input Bias Current *

DEFINITION OF INPUT BIAS CURRENT

Ideally, no current flows into the input terminals of an op amp. In practice, there are always two *input bias currents*, I_{B+} and I_{B-} (see Figure 1).



- **A very variable parameter!**
- **I_B can vary from 60 fA (1 electron every 3 µs) to many µA, depending on the device.**
- **Some structures have well-matched I_B, others do not.**
- **Some structures' I_B varies little with temperature, but a FET op amp's I_B doubles with every 10°C rise in temperature.**
- **Some structures have I_B which may flow in either direction.**

Figure 1: Op Amp Input Bias Current

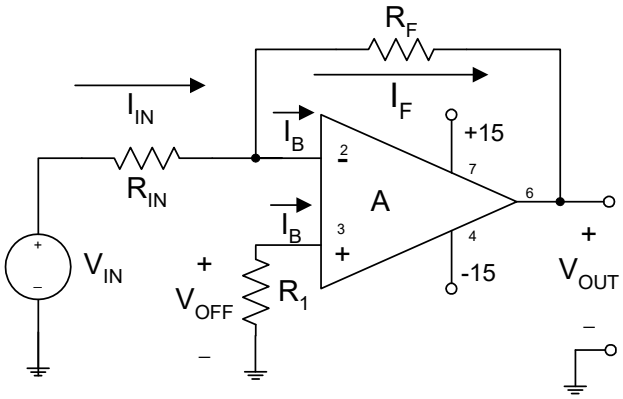
The *input offset* current, I_{OS}, is the difference between I_{B-} and I_{B+}, or $I_{OS} = I_{B+} - I_{B-}$.

741: 200na
357: 0.05na

Current technology:
3fA LTC6268

* Analog Devices MT-038 Tutorial

Inverting Amplifier Bias Current Compensation



$$I_{IN} - I_B - I_F = 0$$

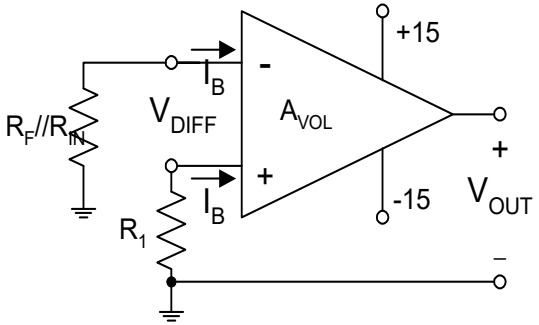
$$V_{OFF} = -R_1 I_B$$

$$\frac{V_{IN} - V_{OFF}}{R_{IN}} - I_B - \frac{V_{OFF} - V_{OUT}}{R_F} = 0$$

but with no input signal, V_{IN} and we want $V_{OUT} = 0$, so :

$$-I_B = V_{OFF}\left[\frac{1}{R_{IN}} + \frac{1}{R_F}\right]; \quad -I_B = -R_1 I_B\left[\frac{1}{R_{IN}} + \frac{1}{R_F}\right]$$

thus : $\left[\frac{1}{R_{IN}} + \frac{1}{R_F}\right] = \left[\frac{1}{R_1}\right]$ as a condtion for no offset at V_o



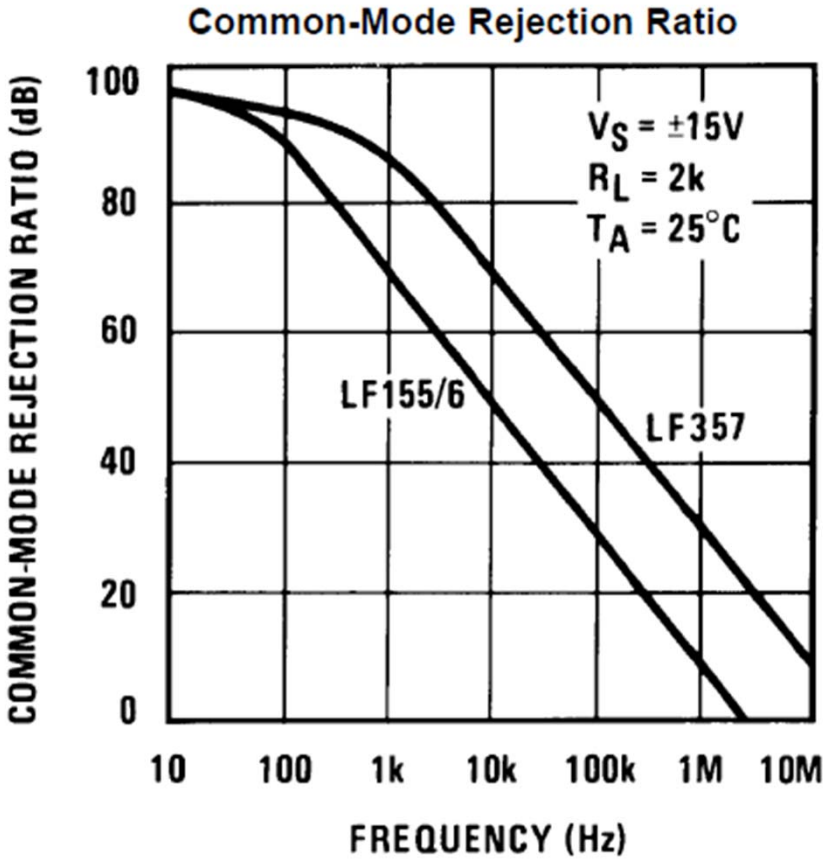
$$V_{OUT} = \left[+ I_B R_F // R_{IN} - I_B R_1\right] A_{VOL}$$

$$V_{OUT} = 0 \; if \; R_F // R_{IN} = R_1$$

$$V_{OUT} = \left[+ I_B R_F // R_{IN} - I_B R_1\right] A_{VOL}$$

$$V_{OUT} = 0 \; if \; R_F // R_{IN} = R_1$$

Common Mode Rejection Ratio CMRR



CMRR: ratio of the common-mode gain to differential-mode gain.

Example, if a differential input change of Y volts produces a change of 1 V at the output, and a common-mode change of X volts produces a similar change of 1 V, then the CMRR is X/Y.

CMRR often expressed in dB:

$$CMRR = 20\log\frac{A_{OL}}{A_{CM}}$$

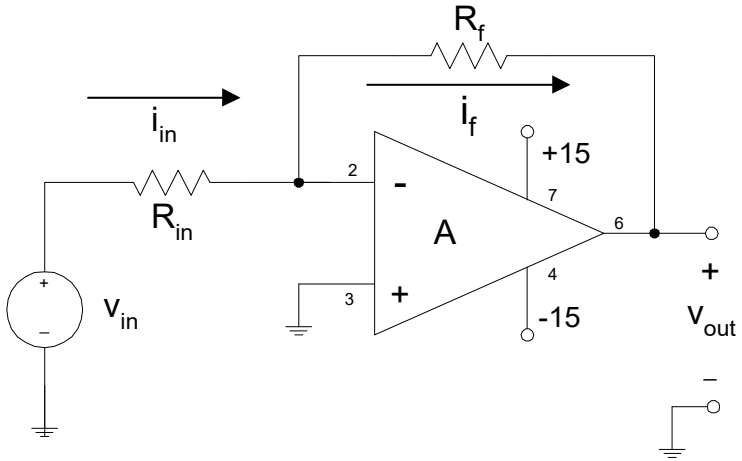
Inverting Amplifer – Virtual Ground Analysis

Assumptions

Infinite input impedance: $\therefore i_+ = 0; \quad i_- = 0$

$A = \infty \qquad v_- = 0 \; because \; v_+ \; is \; grounded.$

$$A >> A_V = \frac{-R_f}{R_{in}}$$

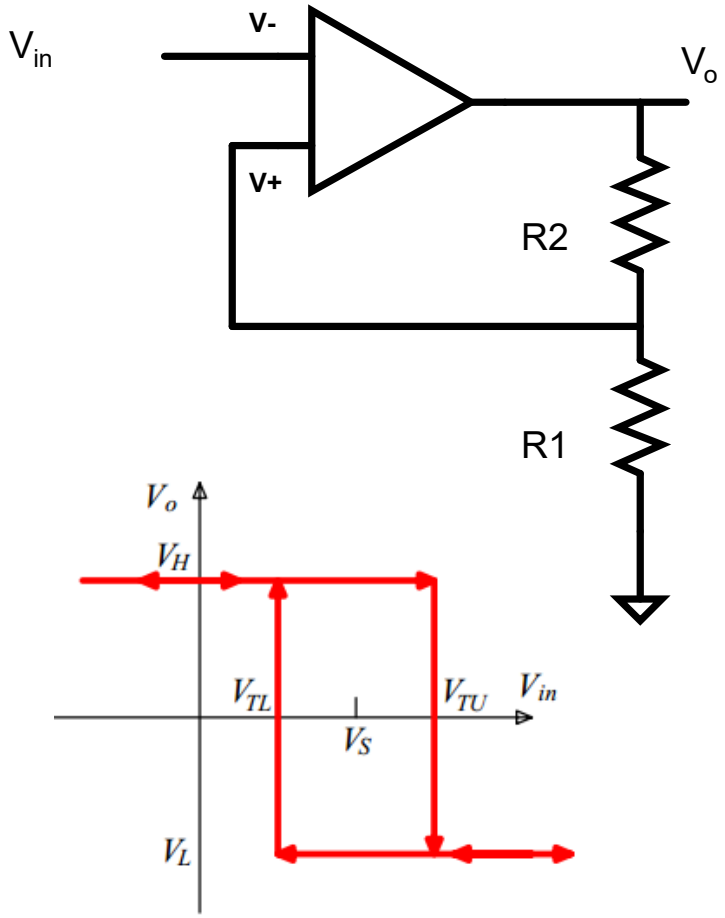


$$i_{in} - i_f = 0$$

$$\frac{v_{in} - 0}{R_{in}} - \frac{0 - v_{out}}{R_f} = 0$$

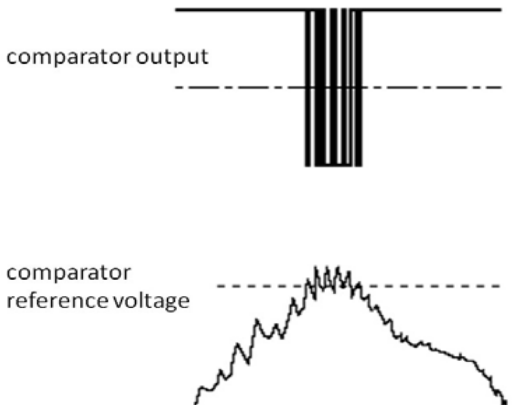
$$\frac{v_{out}}{v_{in}} = \frac{-R_f}{R_{in}} = A_v$$

Schmitt Trigger



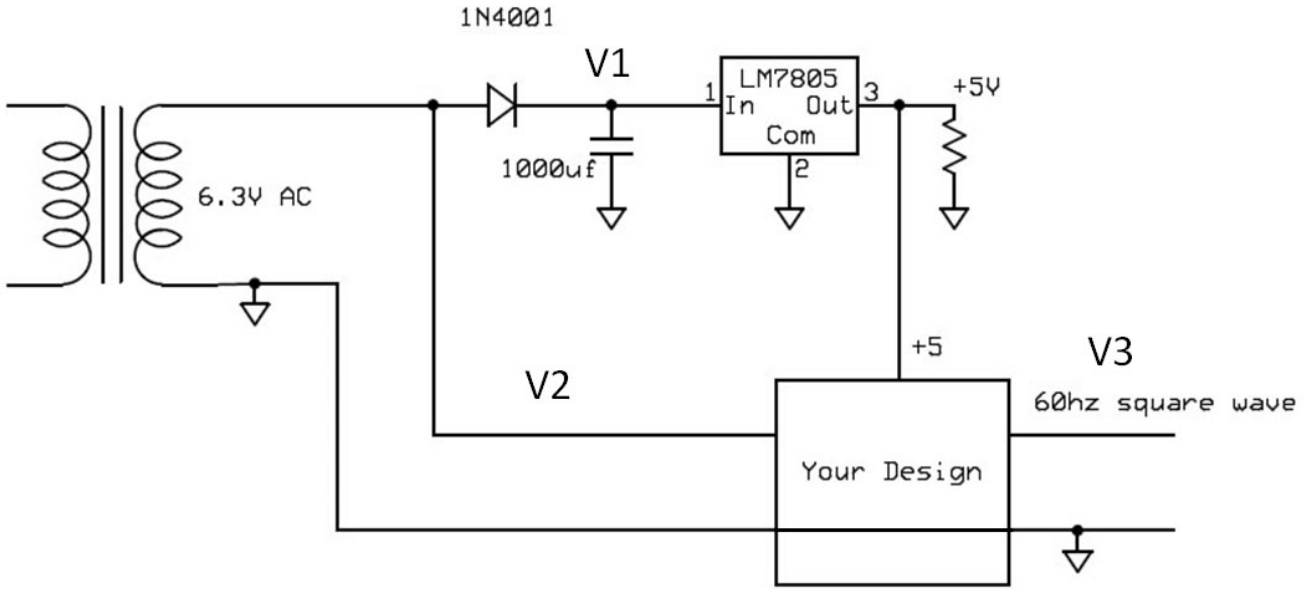
- Schmitt trigger have different triggers points for rising edge and falling edge.
- Can be used to reduce false triggering
- This is NOT a negative feedback circuit.

2015 Quiz Question – Digital Clock Using 60Hz

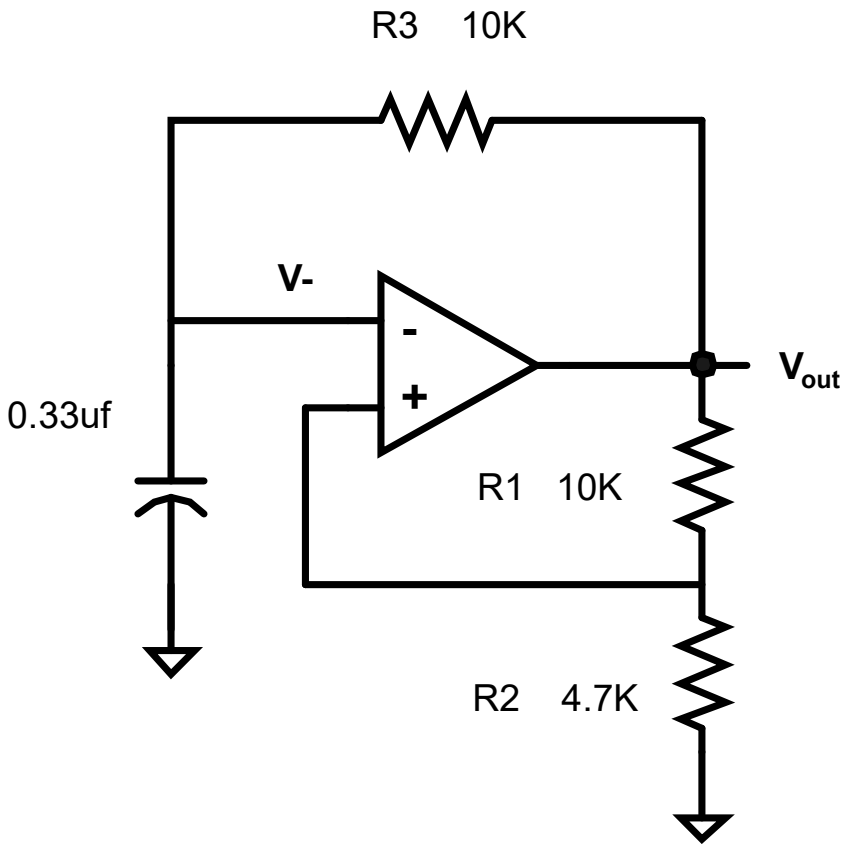


The 60 Hz waveform crosses the reference voltage multiple times because of the 200mv noise.

Design a circuit with a Schmitt trigger ("Your design") using a LM6132 with the thresholds greater than 200mv to fix the problem. A LM7805 voltage regulator IC is used to provide a 5V output to power the digital clock circuit (modeled as a resistor) as well as to supply +5V for the LM6132 in "Your design".

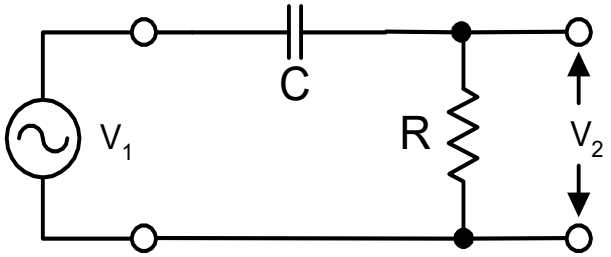


Schmitt Trigger + RC Feedback = Oscillator

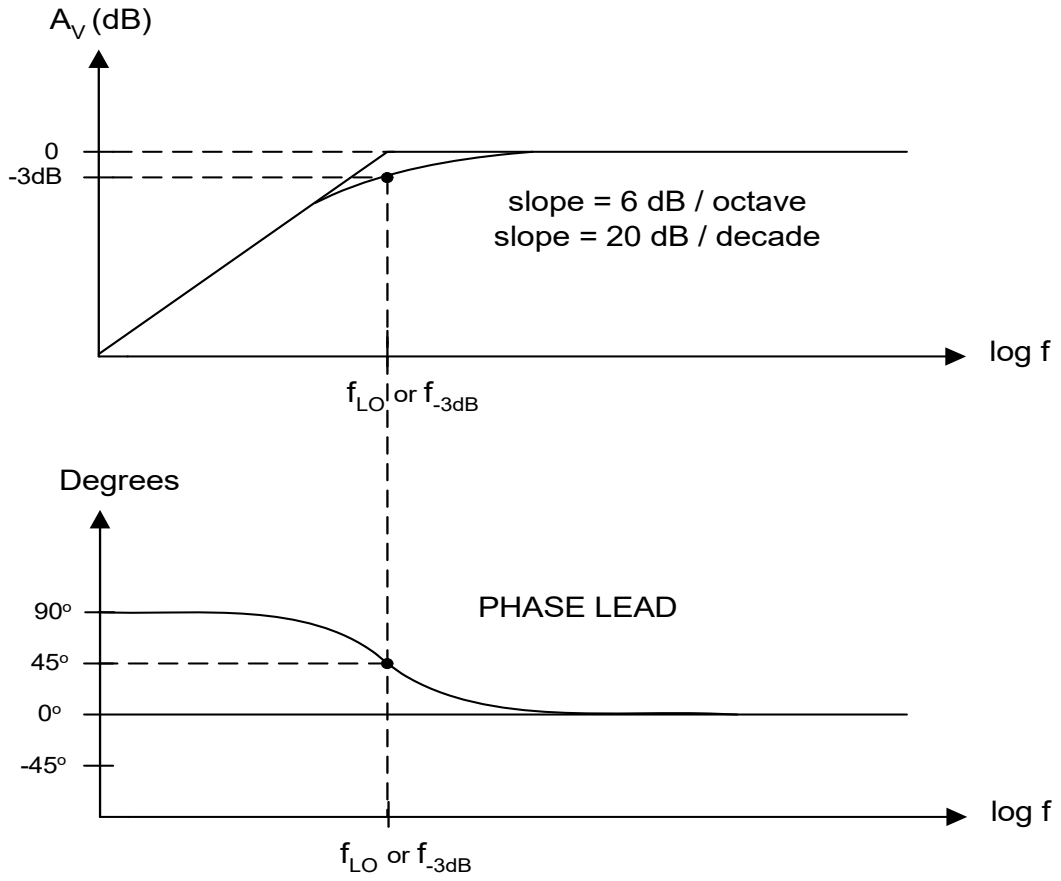


- 741 op-amp.
- R1=10k, R2=4.7k, R3=10K, C=.33uf
- Display V- and V_{out} on the scope. Set R3=4.7k. Predict what happens to the frequency.

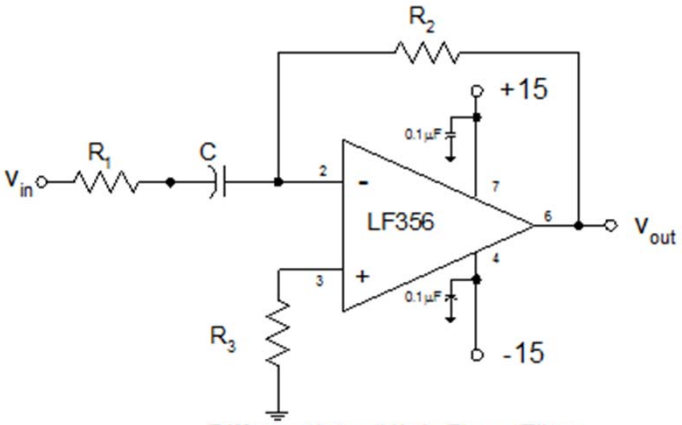
High Pass Filter HPF



$$A_v = \frac{V_2}{V_1} = \frac{R}{R + \frac{1}{j\omega C}} = \frac{j\omega CR}{j\omega CR + 1} = \frac{s\,CR}{s\,CR + 1}$$



Differentiator Insights



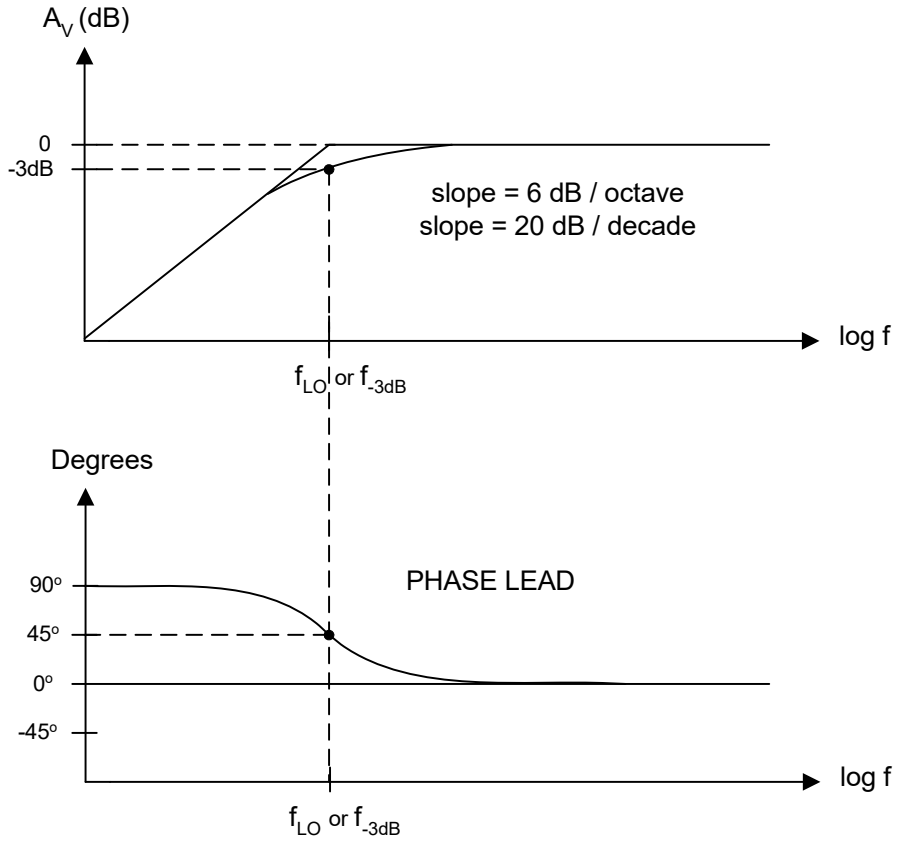
Differentiator/High Pass Filter

$$A_v = \frac{-R_2}{R_1 + \frac{1}{sC}} = \frac{-sCR_2}{sCR_1 + 1}; \quad s = j\omega;$$

at low frequency $sCR_1 << 1$

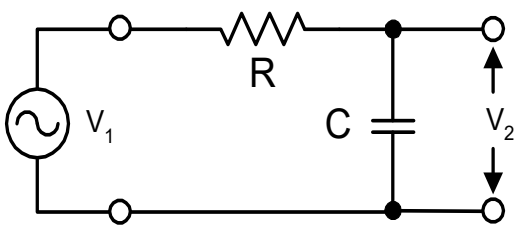
$$A_v = -sCR_2$$

multiplying by s equals differentiation



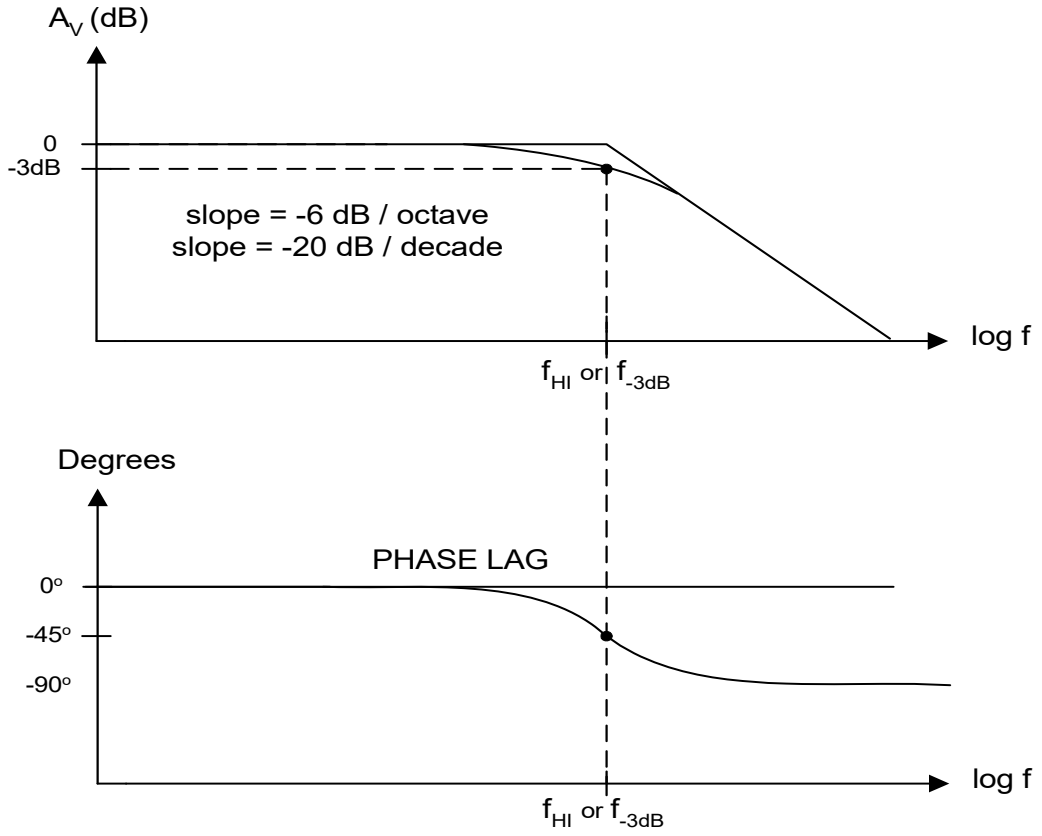
differentiation works only at f << f_{lo}

Low Pass Filter LPF

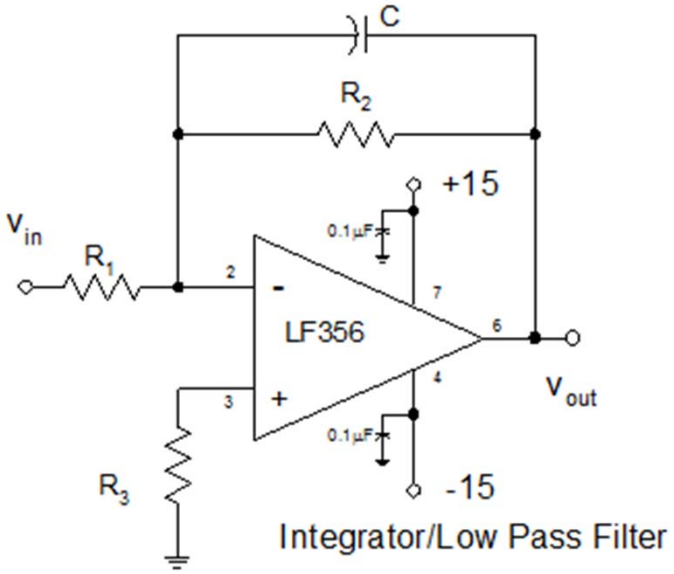


$$A_v = \frac{V_2}{V_1} = \frac{j\,X_C}{R + j\,X_C} = \frac{\frac{1}{j\,\omega C}}{R + \frac{1}{j\,\omega C}} = \frac{1}{j\,\omega RC + 1}$$

$$A_v = \frac{1}{sRC + 1}$$



Integrator Insights



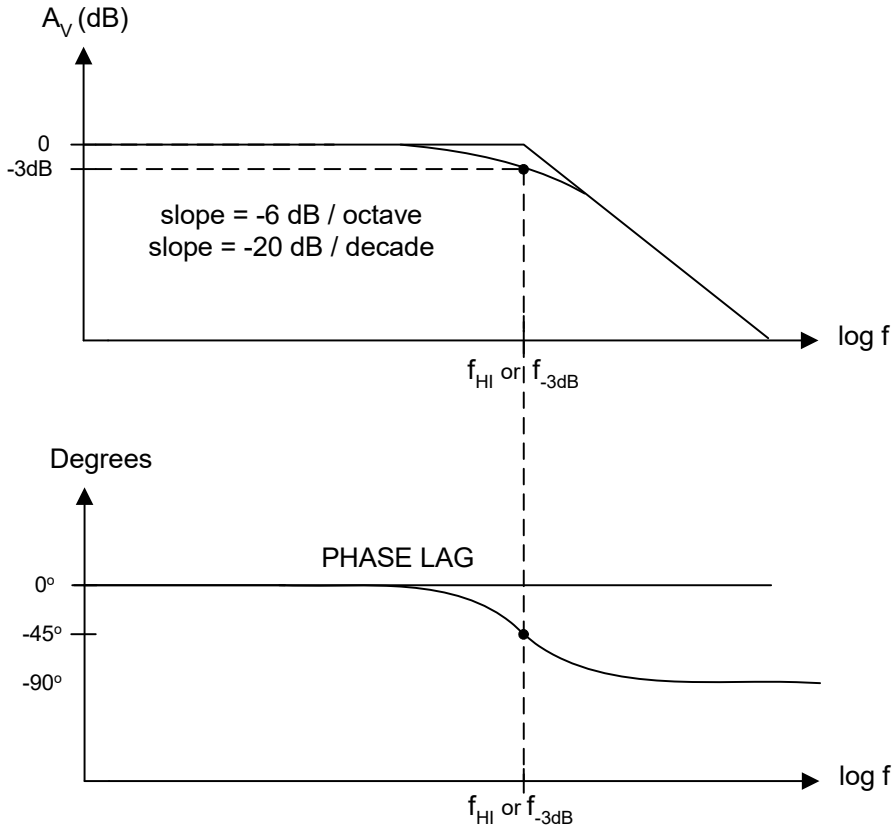
Integrator/Low Pass Filter

$$A_v = -\frac{R_2 / R_1}{1 + sCR_2}; \quad s = j\omega;$$

at high frequency $sCR_2 >> 1$

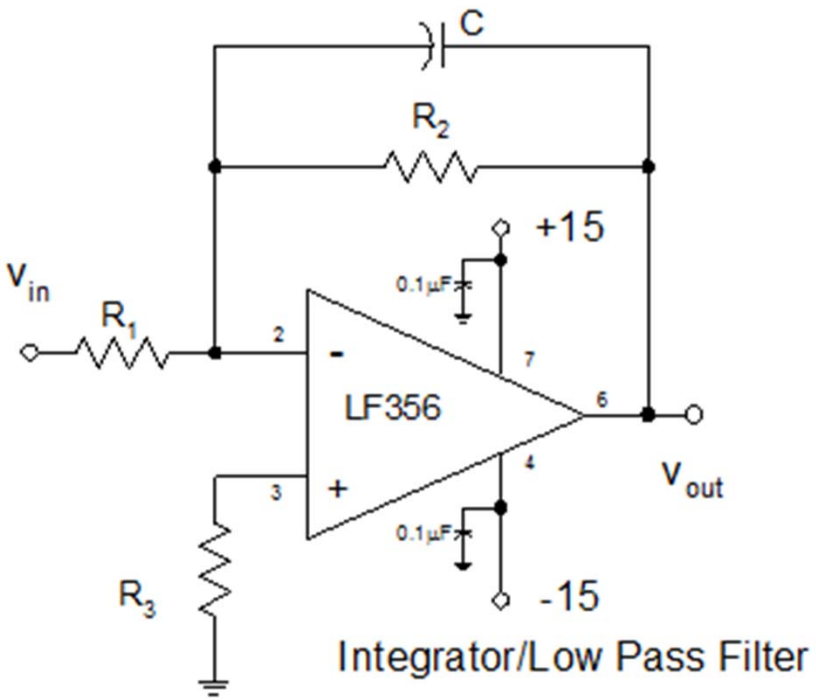
$$A_v = -\frac{R_2 / R_1}{sCR_2} = -\frac{1}{sCR_1}$$

dividing by s equals integration



integration works only at f >> f_{HI} $sCR_2 >> 1$

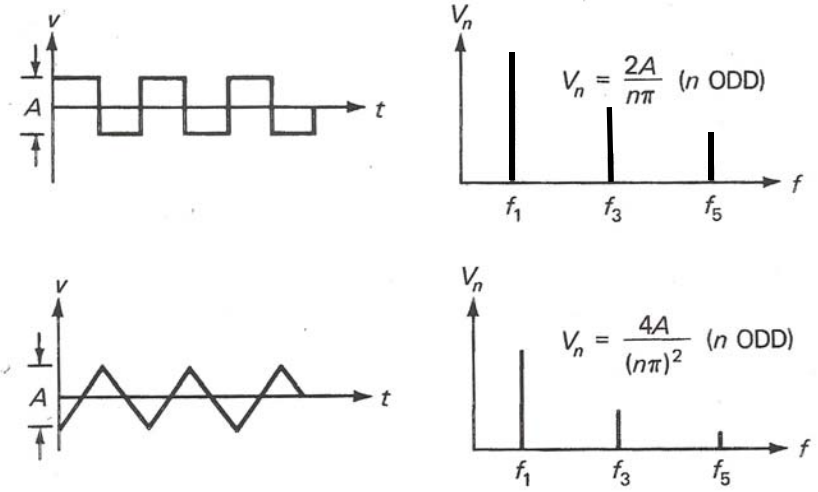
Why R2?



Without R2, any DC bias current will saturate V_{out} since the DC gain is the open loop gain

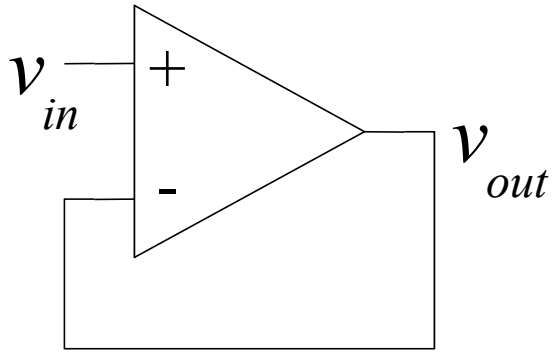
Frequency Domain Insight

- Integration and differentiation easy to understand in time domain
- In frequency domain, difference between square wave and triangle wave is amplitude and phase – same harmonics.
- Integrator (LPF) rolls off harmonics and phase shift to create a triangle wave
- Differentiator (HPF) amplifies harmonics and phase shift to create a square wave.



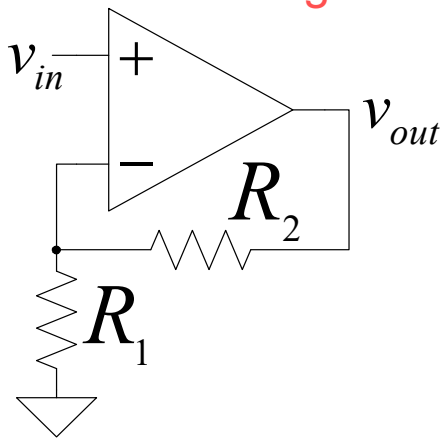
Basic OpAmp Circuits

Voltage Follower (buffer)



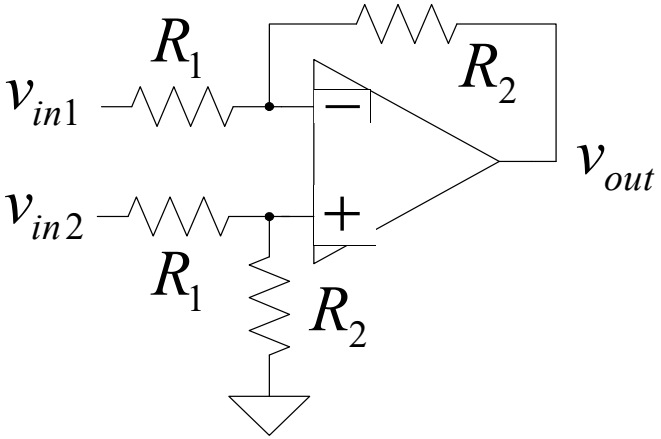
$$v_{out} \approx v_{in}$$

Non-inverting



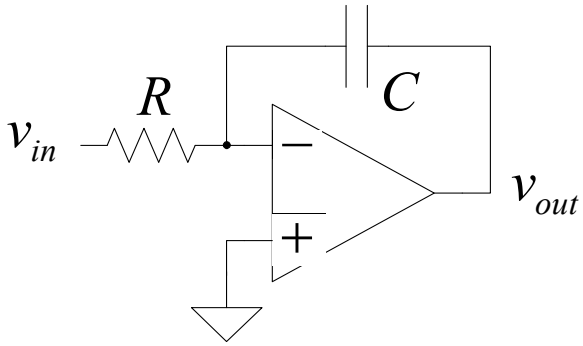
$$v_{out} \approx \frac{R_1+R_2}{R_1} v_{in}$$

Differential Input



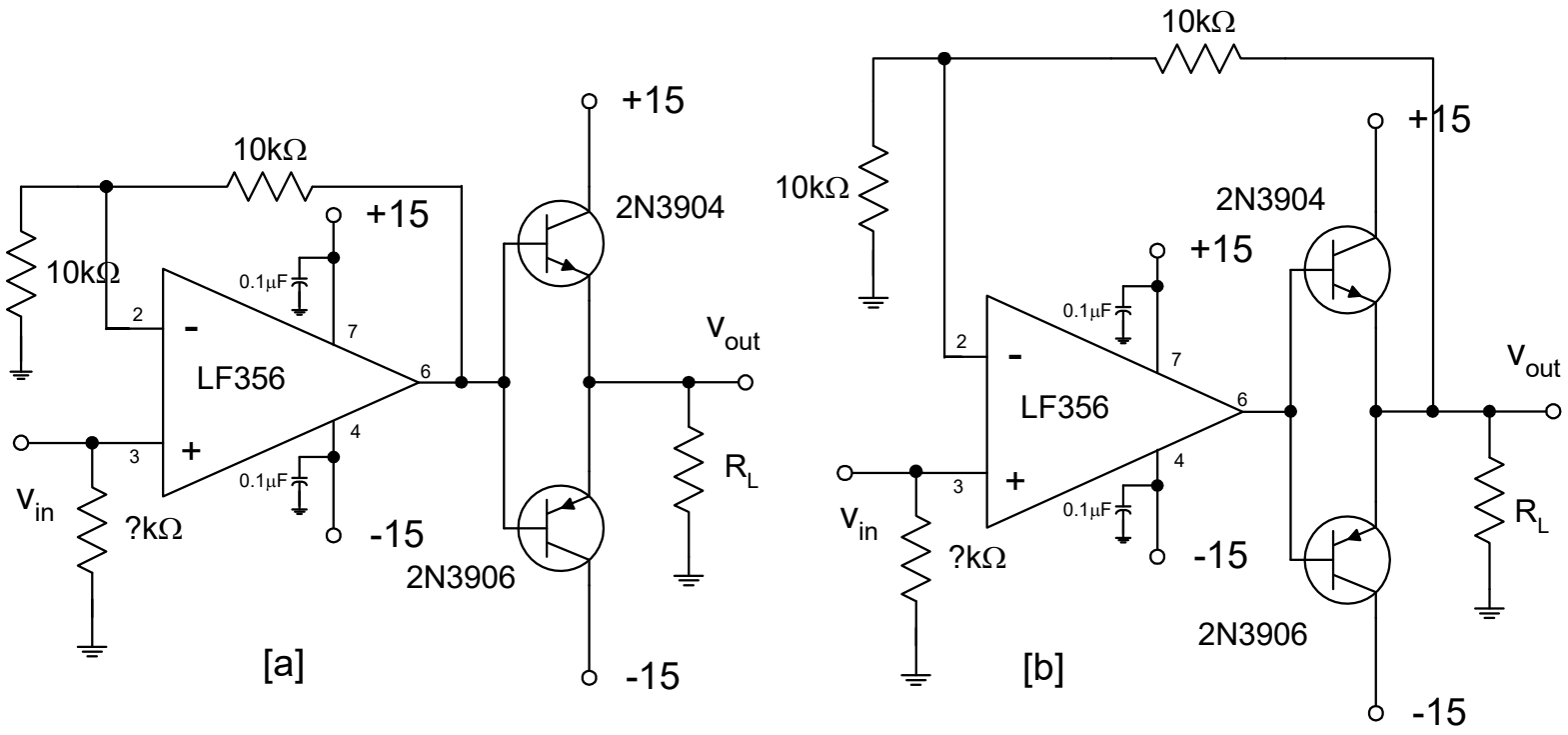
$$v_{out} \approx \frac{R_2}{R_1}\left(v_{in2} - v_{in1}\right)$$

Integrator



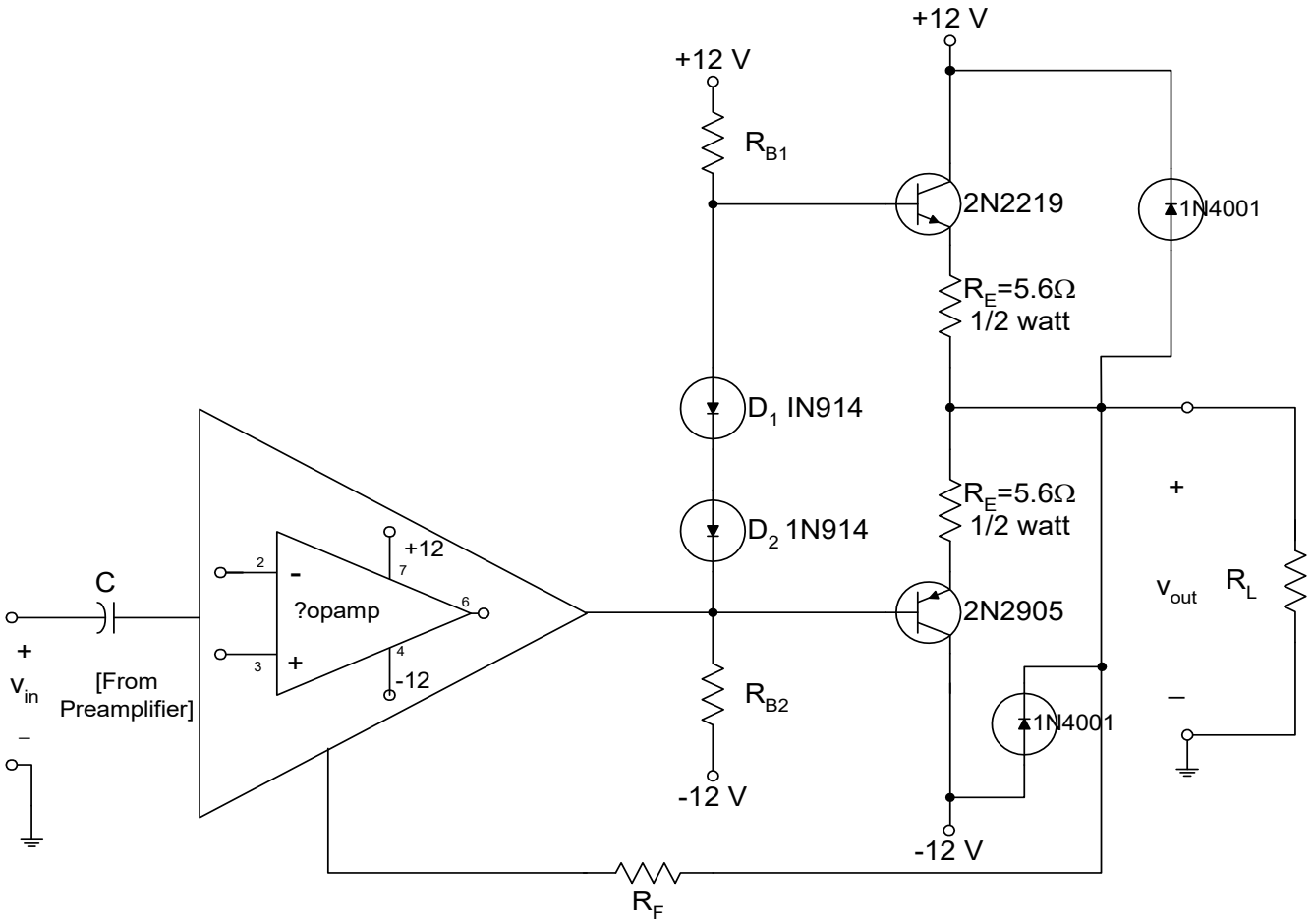
$$v_{out} \approx -\frac{1}{RC}\int_{-\infty}^{t} v_{in}\,dt$$

Crossover Distortion (hole)



Why is [b] better?

Diode Biasing




Analog Color Organ
Mark Vrablic