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Picowatt, 0.45-0.6 V Self-Biased Subthreshold CMOS Voltage Reference

Arthur Campos de Oliveira, *Student Member, IEEE,* David Cordova, *Student Member, IEEE,* Hamilton Klimach, *Member, IEEE,* and Sergio Bampi, *Member, IEEE*

***Abstract*—In this paper, a self-biased temperature-compensated CMOS voltage reference operating at picowatt-level power consumption is presented. The core of the proposed circuit is the self-cascode MOSFET (SCM) and two variants are explored: a self-biased self-cascode MOSFET (SBSCM) and a self-biased NMOS (SBNMOS) voltage reference. Power consumption and silicon area are remarkably reduced by combining subthreshold operation with a self-biased scheme. Trimming techniques for both circuits are discussed aiming at the reduction of the process variations impact. The proposed circuits were fabricated in a standard 0.18-µm CMOS process. Measurement results from 24 samples of the same batch show that both circuits herein proposed can operate at 0.45/0.6 V minimum supply voltage, consuming merely 55/184 pW at room temperature. Temperature coefficient (TC) around 104/495 ppm/ºC across a temperature range from 0 to 120 ºC was measured. By adding a trimming scheme one can reduce the average TC to 72.4/11.6 ppm/ºC for the same temperature range. Both variants of the proposed circuit achieve a line sensitivity of 0.15/0.11 %/V and a power supply rejection better than -44/-45 dB from 10 Hz to 10 kHz. In addition, SBSCM and SBNMOS prototypes occupy a silicon area of 0.002 and 0.0017 mm^2, respectively.**

***Index Terms*—Subthreshold, voltage reference, self-biased, low power, low voltage, picowatt.**

I. Introduction

THE advent of the Internet of Things (IoT) has been a technological booster for the research efforts towards the design of low-power and low-voltage integrated circuits. The main target of these designs are intra-body and portable biomedical devices [1], [2], energy harvesting systems [3], and energy-autonomous wireless sensors platforms [4], [5]. Since such systems are very power constrained, their building blocks must also operate with very limited power.

One of the fundamental blocks for analog and mixed-signal applications is the voltage reference (VR). Its most common implementation strategy is the so-called bandgap voltage reference (BGR). In the BGR, temperature compensation is achieved when the junction diode (usually implemented as a bipolar transistor) complementary-to-absolute-temperature (CTAT) voltage behavior is counterbalanced by a proportional-to-absolute-temperature (PTAT) source, resulting in the silicon bandgap voltage as the reference output, which is approximately 1.2 V. Although BJT based BGR presents adequate performance for many applications, it cannot operate with power supplies lower than around 1.5 to 1.8 V, implying that supply voltage scaling of such BGRs is impractical. Voltage dividers [7], [8] or Schottky barrier diodes (SBD) [22] are an alternative strategy to realize lower supply voltage references. Nonetheless, the minimum supply voltage and current remain constrained by BJT and SBD characteristics. In contrast, MOSFET subthreshold operation [6] can offer an interesting alternative for both low power and low voltage operation.

Throughout the years, several MOSFET subthreshold solutions were proposed in order to improve the design of voltage references for both low power and low voltage operation [6–21]. In [9], the usage of transistors with different V_Ts in both weak and strong inversion allows complete suppression of mobility temperature dependence while consuming tens of nanowatts operating below 1 V. A reference voltage based on SCM with different V_Ts was presented in [10], however current source transistors operating in moderate inversion restrain the minimum supply voltage. A temperature-compensated NMOS load in weak inversion was proposed in [11], which consumes less than 3 nW. The authors in [15] proposed a bulk-driven scheme that allows low voltage and low power operation even with transistors operating in moderate inversion. A voltage reference based on the zero temperature coefficient (ZTC) point was proposed in [17], yet not only its moderate inversion operation limits the minimum supply but also low power operation results in larger silicon area. Although presenting good performance for some applications, the works described above require additional current references to bias the voltage reference core, thus increasing area and total power consumption. Here we refer to the aforementioned circuits as non-self-biased (Non-SB). Such circuits can consume units to tens of nW whereas current leading-edge building blocks for ultra-low power (ULP) applications, e.g. miniature sensing systems, require reduction to the pW level range.

Just a few voltage references operating at such pW consumption levels have been proposed in the literature so far [12–14], [18–21], but these circuits do not offer a well defined current to bias the voltage reference main core since they are biased with the leakage current of a native MOS [12], [14], [18], [20], of a standard NMOS [13], [19] or of a PMOS transistor [14]. Even though leakage based strategy provides a solution for pW voltage reference biasing, the current generated by these structures cannot be simultaneously mirrored through PMOS and NMOS branches for subsequent blocks.

In this work, we explore the usage of a self-biasing scheme to further reduce power consumption of subthreshold voltage references further providing an alternative for biasing subsequent blocks. Two self-biased variants are presented. The first

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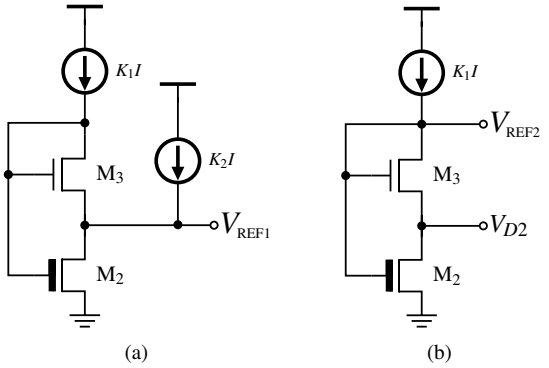


Fig. 1. Simplified scheme of the voltage reference variants.

one is a self-biased self-cascode MOSFET (SBSCM) and the second one is a temperature-compensated self-biased NMOS (SBNMOS) active load in weak inversion. Results show that, by employing the proposed approach, power consumption and silicon area can be remarkably reduced when compared to non-self-biased solutions, while staying among the best low power all-CMOS voltage references in the literature.

This paper is organized as follows: Section II presents the operation principle of the proposed circuit and its variants; Section III discusses the key design considerations of the proposed structure; Section IV reports the prototype measurement results; compensation after fabrication process is presented in Section V; Section VI compares the obtained results of the proposed circuits with other voltage references published. Finally, the paper conclusions are drawn in Section VII.

II. Operation Principle

The simplified circuit schematics of both proposed voltage references are shown Fig 1. In both cases, the SCM [6] is composed of transistors with different threshold voltages: M_2 is a high-V_T transistor (3.3 V) and M_3 is the standard one (1.8 V). The threshold voltage values specifically used in this paper are derived from the target process herein used for IC prototyping, but the design principle itself is applicable to other CMOS processes as well.

A. Unified Current Control Model

Since the circuit under study is based on subthreshold MOSFET operation aiming for low power consumption, a transistor model appropriate for the weak inversion region must be used. According to the Unified Current Control Model (UICM) [23], the drain current of a MOSFET can be described as the superposition of a forward (I_F) and a reverse (I_R) current components

$$I_D = I_F - I_R = I_S(i_f - i_r) \tag{1}$$

where $I_S = I_{SQ}S$, S is the transistor aspect ratio W/L and W and L are the channel width and length, respectively. The inversion coefficients i_f and i_r are the forward and reverse normalized currents; $I_{SQ} = \mu C'_{ox} n \frac{\phi_t^2}{2}$ is the sheet normalization current, which is process related, μ represents the carrier mobility, n the subthreshold slope factor, C'_{ox} is the gate capacitance per unit area, and $\phi_t = kT/q$ the thermal voltage. The relationship between the normalized currents and voltages is given by

$$\frac{V_G - V_T - nV_{S(D)}}{n\phi_t} = \sqrt{1+i_{f(r)}} - 2 + \ln\left(\sqrt{1+i_{f(r)}} - 1\right) \tag{2}$$

where V_G, V_S and V_D are the gate, source and drain voltages referenced to the bulk terminal, and V_T is the threshold voltage.

From expressions (1) and (2), the drain current of a long channel NMOS transistor operating in WI ($i_f \ll 1$) is given by

$$I_D = 2eI_S \exp\left(\frac{V_G - V_T}{n\phi_t}\right)\left[\exp\left(\frac{-V_S}{\phi_t}\right) - \exp\left(\frac{-V_D}{\phi_t}\right)\right] \tag{3}$$

in which, for $V_D \geq 3 \sim 4\phi_t$ the drain current becomes almost independent of the drain voltage expressed inside the brackets in (3). Such current saturation at low drain-to-source voltages is observed in long channel MOSFETs, in which the drain-induced barrier lowering effect (which affects the short-channel V_T by raising the drain voltage) is negligible.

B. Self-Biased Self-Cascode Voltage Reference - SBSCM

As Fig. 1(a) shows, V_{REF1} is generated through the self-cascode MOSFET (SCM) connection of M_2 and M_3 which have the same gate-to-bulk voltage. The SCM, in turn, is biased by two current branches that allow independent control of the inversion coefficient of M_2 and M_3. The generation of a voltage reference through the SCM is a good choice for low power since it can operate at very low current levels.

Usually, the bottom transistor of the self-cascode (M_2) is considered to be in triode. However, since the value of $V_{REF1}(V_{D2})$ is expected to be much greater than $4\phi_t$, M_2 is considered to be saturated in both cases of Fig. 1. The drain currents in Fig. 1(a) can be estimated through (1)-(2). Supposing that M_2 and M_3 are saturated ($i_{r2,3} = 0$), both operate in WI ($i_{f2,3} \ll 1$) and, with all voltages referenced to their bulk terminals, which are connected to ground, they can be written as

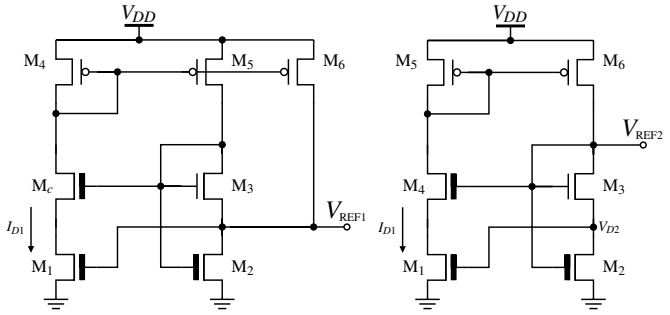
$$I_{D2} = 2eI_{S2} \exp\left(\frac{V_{G2} - V_{T2}}{n_2\phi_t}\right) \tag{4}$$

$$I_{D3} = 2eI_{S3} \exp\left(\frac{V_{G3} - V_{T3}}{n_3\phi_t} - \frac{V_{REF1}}{\phi_t}\right) \tag{5}$$

Since $I_{D2} = (K_1 + K_2)I$, $I_{D3} = K_1 I$ and $V_{G2} = V_{G3}$, the voltage reference of Fig. 1(a) is given by

$$V_{REF1} = \frac{V_{T2} - V_{T3}}{n_3} + \frac{\phi_t}{n_3}\ln\left(\frac{I_{S3}^{n_3}(K_1+K_2)^{n_2}}{I_{S2}^{n_2}K_1^{n_3}}\right) + \frac{n_2 - n_3}{n_3}\phi_t \ln\left(\frac{I}{2e}\right) \tag{6}$$

Therefore, the SCM of Fig. 1(a) provides an output voltage reference that is mainly defined by the difference between the threshold voltages of the 3.3 V and 1.8 V transistors, as shown in (6). The second component in (6) is PTAT and depends



(a) SBSCM (b) SBNMOS

Fig. 2. Schematic of the proposed voltage references.

on geometric and process parameters only. Additionally, it can also be seen that a last PTAT component is added which depends on the bias current (I) and results from the difference of subthreshold slope factors (n) of the transistors M_2 and M_3, which have different threshold voltages.

For the SCM to operate with a current as low as possible, the bias current I is derived from the SCM output voltage itself through a feedback path, as in the current reference proposed in [11]. Hence, our voltage reference circuit herein proposed is called a self-biased self-cascode MOSFET (SBSCM) voltage reference.

The schematic of the proposed SBSCM voltage reference is shown in Fig. 2(a) where M_2 and M_3 compose the SCM, and M_1 defines the current reference I_{D1}. The SBSCM uses a high-V_T transistor for M1 (for which the nominal supply can be as high as 3.3V), since the target is a sub-nA bias current. The PMOS transistors form the current mirror and define the current ratios $K_1 = S_5/S_4$ and $K_2 = S_6/S_4$. Additionally, paths K_1 and K_2 provide an alternative way for a trimming scheme to compensate TC for fabrication variations, as it will be presented further in section V. The M_c transistor implements a cascode current source that can be used to improve the line sensitivity (LS) at the cost of increasing the minimum supply voltage, making its usage conditional on the target performance. In the fabricated version of the SBSCM, the core generated current is simply the drain current of M_1 without the use of M_c.

The core generated current of the proposed circuit is simply the drain current of M_1

$$I_{D1} = 2eI_{S1}\exp\left(\frac{V_{\mathrm{REF1}} - V_{T1}}{n_1\phi_t}\right) \tag{7}$$

By replacing (7) in (6), and defining $\varepsilon = 1 - \frac{n_2 - n_3}{n_1 n_3}$, the SBSCM generated voltage reference is now given by

$$V_{\mathrm{REF1}} = \frac{V_{T2} - V_{T3}}{n_3\varepsilon} + \frac{\phi_t}{n_3\varepsilon}\ln\left(\frac{(K_1+K_2)^{n_2} I_{S3}^{n_3} I_{S1}^{n_2-n_3}}{I_{S2}^{n_2} K_1^{n_3}}\right) + \left(\frac{n_3 - n_2}{n_1 n_3 \varepsilon}\right) V_{T1} \tag{8}$$

The threshold voltage has an approximately linear negative dependence on temperature that can be expressed as [24]

$$V_T(T) = V_T(T_0) - \alpha_T(T - T_0) \tag{9}$$

where $V_T(T_0)$ is the threshold voltage at room temperature and α_T is the first derivative of the threshold voltage with respect to temperature.

Replacing (9) in (8) and setting $\frac{\partial V_{\mathrm{REF1}}}{\partial T} = 0$, the optimal ratio between aspect rations S_3 and S_2 of M_3 and M_2, respectively, can be expressed as

$$\left(\frac{S_3^{n_3}}{S_2^{n_2}}\right)_{\mathrm{OPT}} = \frac{K_1^{n_3} I_{SQ2}^{n_2}}{I_{SQ3}^{n_3}(K_1+K_2)^{n_2} I_{S1}^{n_2-n_3}} \times \exp\left[\frac{q}{k}\left(\frac{n_1(\alpha_{T2} - \alpha_{T3}) - (n_2 - n_3)\alpha_{T1}}{n_1}\right)\right] \tag{10}$$

From expressions (8)-(10) the temperature compensated voltage reference is given by

$$V_{\mathrm{REF1}} = \frac{V_{T2}(T_0) - V_{T3}(T_0)}{n_3\varepsilon} + \left(\frac{n_3 - n_2}{n_1 n_3 \varepsilon}\right) V_{T1}(T_0) + T_0\left(\frac{n_1(\alpha_{T2} - \alpha_{T3}) - (n_2 - n_3)\alpha_{T1}}{n_1 n_3 \varepsilon}\right) \tag{11}$$

As shown by (11) the proposed SBSCM provides at its output a reference that is mainly defined by the difference between threshold of the 3.3 V and the 1.8 V transistors, since the α_T term is negligible at room temperature.

C. Self-Biased NMOS Load Voltage Reference - SBNMOS

With the expression of the SBSCM at hand, the analysis of the SBNMOS output (V_{REF2}) can be simplified. As Fig. 1(b) shows, the NMOS load voltage V_{REF2} is simply voltage V_{G2}, which is

$$V_{\mathrm{REF2}} = V_{T2} + n_2\phi_t \ln\left(\frac{I_{D2}}{2eI_{S2}}\right) \tag{12}$$

The temperature behavior of (12) can be compensated since its first term is CTAT and its second, PTAT.

Fig. 2(b) presents the complete circuit where all transistor operate in WI. Besides, M_1, which is a 3.3 V transistor, defines the bias current, M_4 acts as a cascode to shield M_1 from supply voltage variations, and transistors M_5 and M_6 act as a current mirror thus defining $K_1 = S_6/S_5$. The necessity of using the cascode transistor M_4 arises from the fact that the LS of V_{REF2} is directly dependent on the LS of the current source.

From the circuit of Fig. 2(b), through expressions (4)-(12), considering $V_{D2} = V_{\mathrm{REF1}}$ with $K_2 = 0$, and knowing that $I_{D2} = K_1 I_{D1}$, $V_{G2} = V_{G3} = V_{\mathrm{REF2}}$, $\beta = \frac{n_2}{n_1 n_3}$ and $\gamma = n_2 + \beta(n_2 - n_3)$, the resulting output voltage is given by

$$V_{\mathrm{REF2}} = V_{T2}(\beta+1) - \beta(V_{T3} + n_3\varepsilon V_{T1}) + \phi_t \ln\left(\frac{K_1^{\gamma} I_{S1}^{\gamma} {I_{S3}}^{\frac{n_2}{n_1}}}{{I_{S2}}^{n_2(\beta+1)}}\right) \tag{13}$$

Considering the linear approximation of V_T presented by (9) and replacing it into (13), and again setting $\frac{\partial V_{\mathrm{REF2}}}{\partial T} = 0$,

the optimal S_2 ratio for temperature compensation can be expressed by

$$S_{2\mathrm{OPT}} = \frac{(K_1 I_{S1})^{\frac{\gamma}{n_2(\beta+1)}} I_{S3}^{\frac{1}{n_1(\beta+1)}}}{I_{SQ2}} \times \exp\left(\frac{q}{k}\left[\frac{\alpha_{T2}(\beta+1)-\beta(\alpha_{T3}+n_3\varepsilon\alpha_{T1})}{n_2(\beta+1)}\right]\right)^{-1} \quad (14)$$

Thus, by satisfying (14), the temperature compensated V_{REF2} is now expressed as

$$V_{\mathrm{REF2}} = V_{T2}(T_0)(\beta+1) - \beta\left[V_{T3}(T_0) + n_3\varepsilon V_{T1}(T_0)\right] + T_0\left[\alpha_2(\beta+1) + \beta(\alpha_3 + n_3\varepsilon\alpha_1)\right] \quad (15)$$

Since the generated current (I_{D1}) also depends on M_2, the output reference voltage is expected to depend to depend on its threshold voltage V_{T2} by a factor higher than 1 (i.e. $\beta+1$), as represented in the first term of (15). Thus, the proposed circuit provides a reference voltage that depends on threshold voltages of M_1, M_2 and M_3, being V_{T2} the major contributor.

It is important to notice that, for expressions (10) and (14), if $\mu_1 \approx \mu_2 \approx \mu_3 \approx \mu$ is assumed, temperature dependent terms $\left(\mu\frac{\phi_t^2}{2}\right)$ of the specific currents (I_{SQ}) cancel each other. For this reason, the I_{SQ} temperature dependency is not considered in this analysis.

III. Design Considerations

A. Current Consumption Minimization

As depicted in Fig. 2(a) the total current consumed by the SBSCM circuit is given by

$$I_{\mathrm{DD1}} = I_{D1}(1 + K_1 + K_2) \quad (16)$$

Since the ratios S_3 and S_2 set a fixed temperature compensated reference voltage, and its value is applied to the gate of M_1, the generated current will be defined only by the ratio S_1. Therefore, the current consumption can be minimized by setting S_1 to the smallest possible ratio ($\mathrm{W_{MIN}/L_{MAX}}$), at the cost of temperature coefficient degradation, and also by reducing K_1 and K_2 current gains. To further reduce I_{D1} the third branch can be eliminated ($K_2 = 0$) and thus temperature compensation can be made by increasing S_3/S_2. In this case, the trade-off between power consumption and $\mathrm{M}_{2,3}$ area will depend on the threshold voltage temperature slope (α_T).

The total current consumption of the SBNMOS circuit (Fig. 2(b)) is simply (16) with $K_2 = 0$. It is straightforward that the decrease of the bias current I_{D1} depends on the reduction of both S_1 and V_{D2}, which can be reduced by increasing S_2 while reducing S_3. Yet this strategy is not practical since the S_2 ratio for optimal temperature compensation defined by (14) implies that S_2 must also be reduced for a $S_{1,3}$ reduction. Thus, for a small S_1 ratio, S_3 ratio must increase to reduce the current consumption while keeping a reasonable temperature coefficient.

B. Minimum Supply Voltage

Proper operation of the proposed circuits under the assumptions made in the previous sections requires the definition of a minimum supply voltage. This value is set to the minimum voltage needed to make both circuits as independent as possible of V_{DD} variations. In order to satisfy this condition, the saturation condition must be guaranteed. In the subthreshold region, the current of a MOS saturates when its drain-to-source voltage is greater than 3 to 4 times the thermal voltage, i.e., $V_{DS} \geq 3 \sim 4\phi_t$. Hence, in SBSCM without M_c, we have

$$V_{DD1\mathrm{MIN}} = \max\{\overbrace{V_{DS5} + V_{DS3} + V_{\mathrm{REF1}}}^{8\phi_t + 250\ \mathrm{mV}}, \overbrace{V_{DS6} + V_{\mathrm{REF1}}}^{4\phi_t + 250\ \mathrm{mV}}\} \quad (17)$$

Considering that the drain-to-source voltage (V_{DS}) of all transistors must be at least $4\phi_t$ and that from (8) the roughly expected voltage reference value is around 250 mV, the resulting minimum supply voltage will be around 450 mV according to (17). This value can be further reduced by using devices M_2 and M_3 with closer V_T values, thus reducing V_{REF1}.

From (13), the expected value for the SBNMOS voltage reference is around 390 mV. Estimating the minimum V_{DD} supply as done previously, the minimum for the SBNMOS would be simply $V_{\mathrm{REF2}} + 4\phi_t$. From measurement results, the observed minimum supply voltage was 0.6 V. This is because V_{REF2} depends directly on the minimum supply voltage to drive V_{D2} high enough to create the bias current I_{D1}. Therefore, the minimum supply voltage for the SBNMOS will have an additional of $4\phi_t$ to the value expected by only considering the voltage drop paths.

C. Supply Voltage Sensitivity

The sensitivity of a reference voltage with respect to supply voltage variations is commonly evaluated through the line sensitivity (LS) parameter. The LS is defined as

$$\mathrm{LS} = \frac{\Delta V_{\mathrm{REF}}}{\Delta V_{DD} \times V_{\mathrm{REF}\mu}} \times 100\% \quad (18)$$

in which ΔV_{DD} is the V_{DD} range of operation, ΔV_{REF} ($V_{\mathrm{REFMAX}} - V_{\mathrm{REFMIN}}$) is the absolute difference of the reference voltage in the V_{DD} range considered and $V_{\mathrm{REF}\mu}$ is the mean value of the voltage reference for the ΔV_{DD} range. The optimization of the LS lies on the minimization of ΔV_{REF}. Therefore, for both circuits of Fig. 2 this can be done by reducing currents gains K_1 and K_2 (the last one only for the SBSCM).

The line sensitivity of SBSCM can be substantially reduced (around 10× or more) by adding the transistor M_c at the cost of increasing the minimum supply voltage from 0.45 V to 0.6 V. M_c acts as a cascode device with an output impedance much larger than that of M_1. Accordingly, M_c shields M_1 from supply voltage variations, thus improving the LS. The simulation results of the TC sensitivity with respect to V_{DD} for the SBSCM with and without M_c are shown in Fig. 3. Typical simulations of the SBSCM without M_c present a TC of 7 ppm/°C at minimum supply voltage (0.45 V) while the

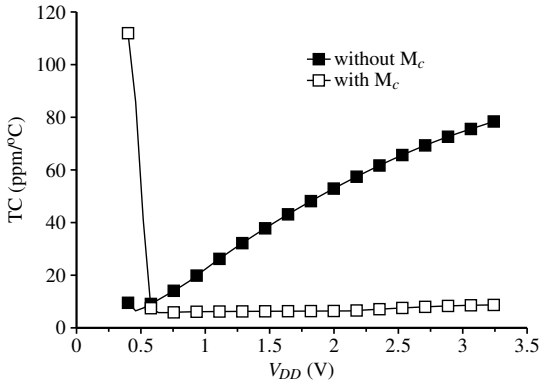


Fig. 3. Comparison of the simulated TC supply voltage dependence with and without M_c transistor.

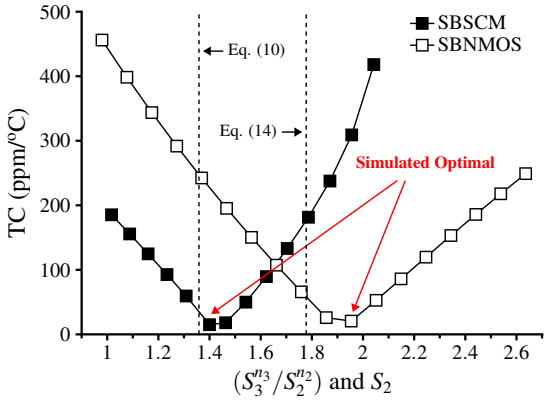


Fig. 4. Simulated transistors sizing for optimal TC.

maximum TC is less than 70 ppm/°C at 3.3 V. The addition of M_c results in a TC lower than 10 ppm/°C for all voltage supply range at the cost of increasing the minimum V_{DD} to 0.6 V.

The channel length modulation was neglected in this circuit design since this effect is not relevant for MOS transistors operating in subthreshold, where drain output impedance depends mainly on drain-induced barrier lowering effect (DIBL). DIBL is significantly reduced by increasing the channel length, therefore the high impedance transistors (SBSCM: M_1, M_5 and M_6; SBNMOS: M_1, M_4 and M_6) were designed with large L to minimize the LS of the proposed circuits.

D. Sizing for Optimal Temperature Compensation

Fig. 4 represents the simulated TC as function of transistor ratios for both SBSCM and SBNMOS. The simulation was performed by properly sizing all other transistors besides M_2 and varying its W/L ratio.

The calculated optimum ratios of (S_3^{n3}/S_2^{n2}) (for SBSCM) and S_2 (for SBNMOS) are 1.34 and 1.78 respectively, as predicted by (10) and (14). As can be seen in Fig. 4 the simulated optimal ratios of the same parameters are 1.4 and 1.92 respectively. The proximity between calculated and simulated values validates the proposed approach. Taking into account the previous considerations as well as layout regularity, the proposed circuits were sized as presented in Table I.

TABLE I
TRANSISTORS SIZING FOR SBSCM AND SBNMOS.

Transistor	Size (W/L)	
	SBSCM	SBNMOS
M_1	1/10	4×4/10
M_2	2×8/10	2×9.6/10
M_3	2×11/10	4/2
M_4	2×6/10	2×4/10
M_5	2×6/10	2×5/10
M_6	4×6/10	2×5/10

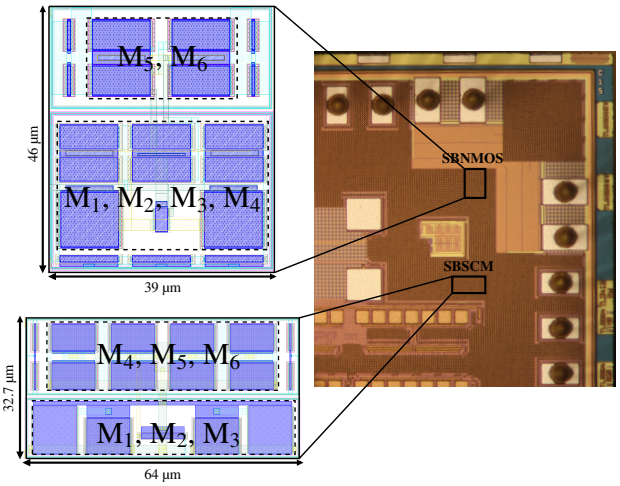


Fig. 5. Chip photo of the proposed voltage references and their layouts.

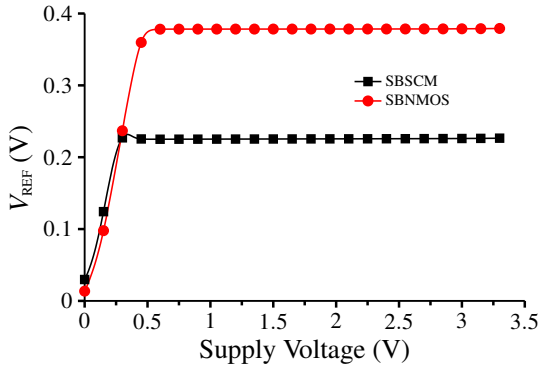
IV. MEASUREMENT RESULTS

The proposed CMOS voltage references were fabricated in a standard 0.18-µm CMOS process. The chip photo and the layout of the proposed circuits are shown in Fig. 5. The total occupied areas are 0.0020 mm^2 and 0.0017 mm^2 for the SBSCM and SBNMOS, respectively. Measurements were performed using a Keysight 4156C Semiconductor Parameter Analyzer for DC biasing and voltage/current measurement. A thermal chamber was used for temperature control. Power Supply Rejection (PSR) was measured using a Keysight B2961A Low Noise Power Source and a Keysight MSO9104A scope. A total of 24 chips from the same batch were packaged in ceramic [25] and measured.

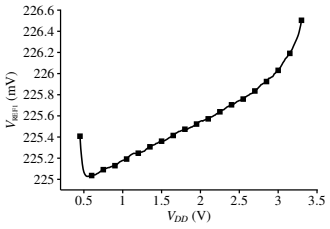
Fig. 6(a) shows the measured results of the supply voltage dependence for average samples of both proposed circuits at 20 °C. As reported, the SBSCM starts to operate at 0.45 V supply, while the SBNMOS at 0.6 V supply. The average measured line sensitivity (LS) from $V_{DD\text{MIN}}$ to 3.3 V was 0.15 %/V (SBSCM - Fig. 6(b)) and 0.11 %/V (SBNMOS - Fig. 6(c)).

The spread of V_{REF} across the 24 measured samples of both circuits at 20 °C and minimum supply voltage are presented in Fig. 7. The V_{REF} mean reference voltages for the SBSCM and SBNMOS are 225.3 mV and 378 mV, respectively, and the V_{REF} variation coefficient (σ/μ - where σ and μ are the standard deviation and mean value) are 0.63 % and 0.8 %, respectively.

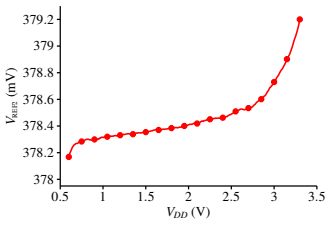
The simulated and measured temperature sensitivity from 0 °C to 120 °C for both circuits are shown in Fig. 8. The



(a) $V_{\mathrm{REF}} \times V_{DD}$

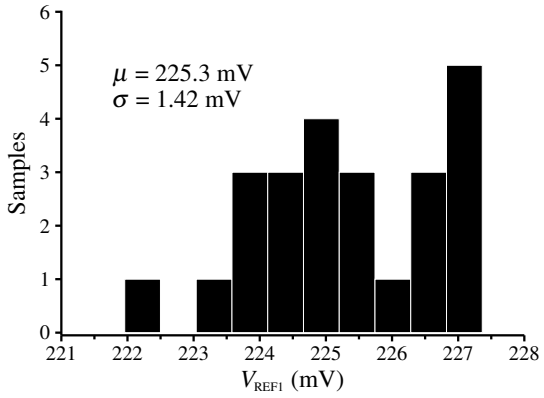


(b) V_{SBSCM} [0.45-3.3 V]

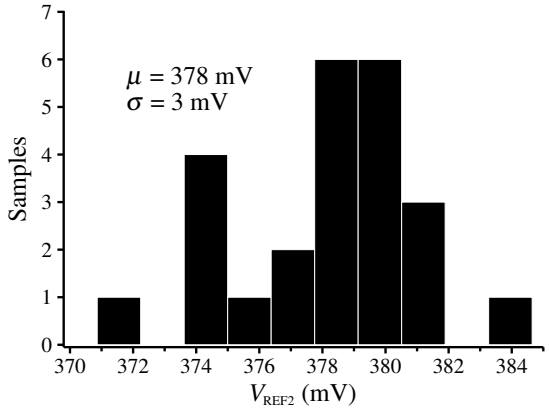


(c) V_{SBNMOS} [0.6-3.3 V]

Fig. 6. Measured V_{REF} supply voltage dependence.



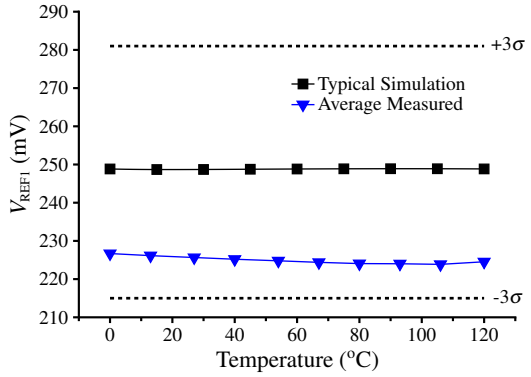
(a) SBSCM



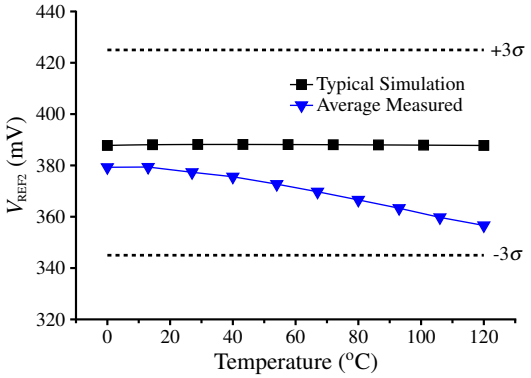
(b) SBNMOS

Fig. 7. Distribution of V_{REF} of the 24 samples @ 20 °C and V_{DDMIN}.

temperature coefficient (TC) is evaluated using the following



(a) SBSCM



(b) SBNMOS

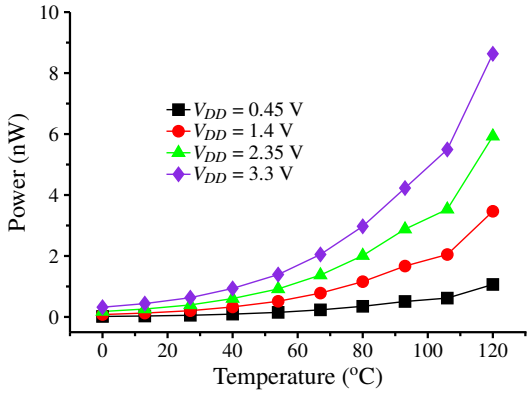
Fig. 8. Average measured and typical simulated temperature behavior showing the ±3σ range.

expression:

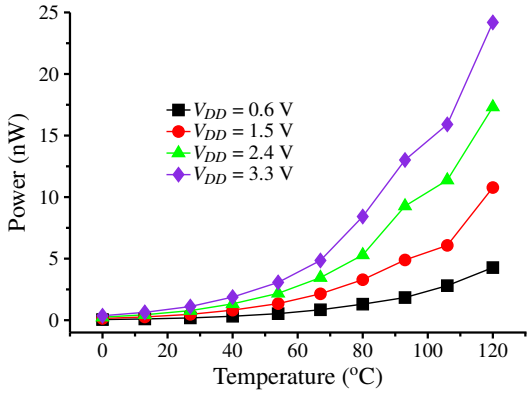
$$\mathrm{TC} = \frac{V_{\mathrm{REFMAX}} - V_{\mathrm{REFMIN}}}{(T_{\mathrm{MAX}} - T_{\mathrm{MIN}})V_{\mathrm{REF27\,^oC}}} \times 10^6 \qquad (19)$$

A TC between 68 ppm/°C and 150 ppm/°C, with a mean of 104 ppm/°C was measured from the 24 samples in the case of the SBSCM, as shown in Fig. 8(a), while for the SBNMOS the mean measured TC was 495 ppm/°C. The simulated worst case TCs at minimum supply voltage across all corners were 65 ppm/°C and 136 ppm/°C for the SBSCM and SBNMOS, respectively. The difference between simulated and measured behaviors may be partially caused by the inaccuracy of the BSIM3v3.2 model for the temperature behavior in deep weak inversion [26].

Fig. 9 shows the measured temperature behavior of the power consumption for different values of V_{DD} for both circuits. Since they are biased with the subthreshold current, the power consumption of the references increases exponentially with temperature. The SBSCM consumes typically 54.8 pW at 0.45 V and 27 °C and reaches a maximum of 8.6 nW at 3.3 V and 120 °C as shown in Fig. 9(a). The SBNMOS measured typical (0.6 V and 27 °C) and maximum (3.3 V and 120 °C) power consumption are 184 pW and 24.2 nW, respectively, as reported in Fig. 9(b). Simulated results of typical and maximum power consumption were 93 pW and 12.5 nW, respectively, for the SBSCM, while for the SBNMOS they were of 350 pW and 41.6 nW. Some dis-



(a) Power consumtion of SBSCM



(b) Power consumtion of SBNMOS

Fig. 9. Measured temperature dependence of the power consumption for different values of supply voltage.

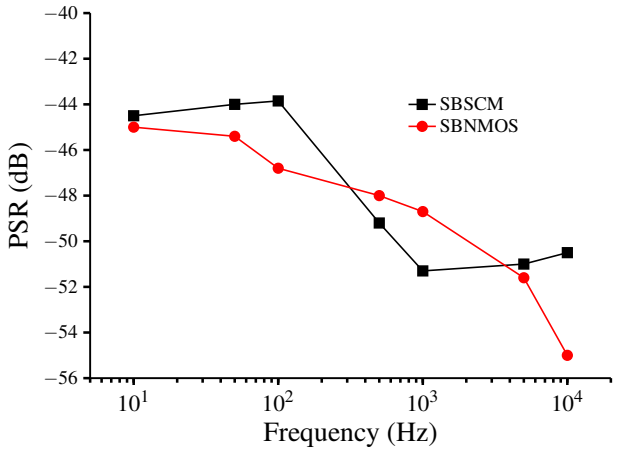


Fig. 10. Measured PSR for both proposed circuits @ $V_{DD\text{MIN}}$.

crepancy between measured and simulated power consumption is expected for both circuits. The SBSCM measured output voltage was around 25 mV less than that from simulation, which means that its consumption was also smaller than that predicted by simulations. The measured SBNMOS output voltage presented a CTAT behavior, indicating that the circuit is not biased with sufficient current to compensate the NMOS active load temperature dependence, thus reducing the power consumption.

Fig. 10 presents the measured PSR for both circuits at minimum supply voltage and 100 Hz resulting -44 dB for the SBSCM and -47 dB for the SBNMOS. Worst case PSR from 10 Hz to 10 kHz are -44.5 dB (SBSCM) and -45 dB (SBNMOS). PSR measurements were done with a high input impedance buffer presenting a total input capacitance of about 4 pF.

Measured start-up time for V_{DD} from 0 V to 3.3 V was 92 ms and 32 ms, for the SBSCM and SBNMOS, respectively. This time increases by 10× when the voltage supply goes from 0 V to $V_{DD\text{MIN}}$.

V. Trimming Analysis

It is well known that sensitivity to process variations of circuits with transistors in subthreshold increases dramatically. Due to the exponential I-V characteristics of MOS transistor in weak inversion, any small variation in threshold voltage causes an exponential change in drain current. Voltage references operating at such region are very much process dependent and present a large spread of both output reference voltage and TC [7], [11], [12]. These variations can be compensated through trimming techniques. From expressions (8) and (13), process variations of the generated reference voltages can be compensated by either increasing or decreasing the current gains K_1 and K_2 through a digital control.

From the corner simulations presented in Fig. 12, the SBSCM and SBNMOS are expected to have a ΔV_{REF} at room temperature of approximately ±6% and ±8%, respectively. As presented in [27], the number of bits of the trimming circuit is determined by the following expression

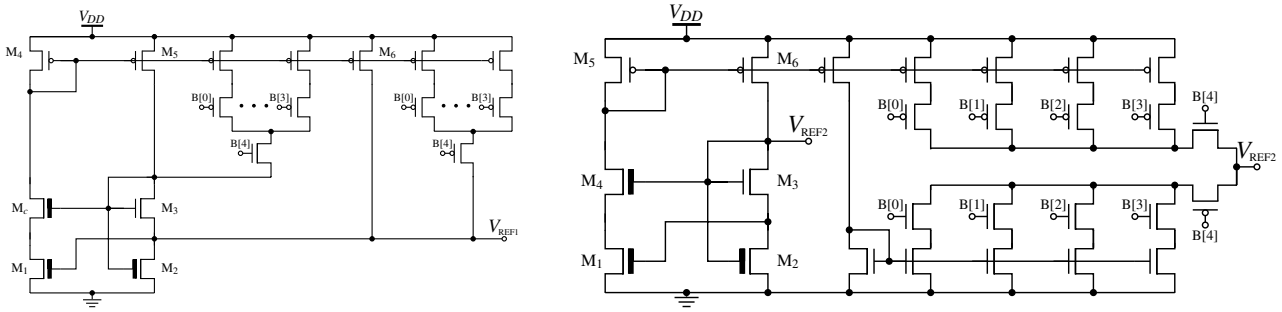
$$\text{BITS} \geq \frac{\ln\left(\frac{V_{FS}}{V_{LSB}}+1\right)}{\ln(2)} \tag{20}$$

where V_{LSB} is the least significant bit voltage and V_{FS} is the full-scale voltage.

The trimming circuit must be designed to cover the entire output voltage variation range while a reasonable V_{LSB} must be chosen in order to reduce the spread of V_{REF}, compensating the output voltage for a target TC [12]. Therefore, the trimming circuit is designed to cover the maximum range at room temperature while having a small V_{LSB} for fine TC compensation. Thus, for SBSCM, choosing $V_{FS} = 6\%V_{\text{REF1}}$ and $V_{LSB} = 0.25\%V_{\text{REF1}}$ lead to a 5-bit trimming circuit.

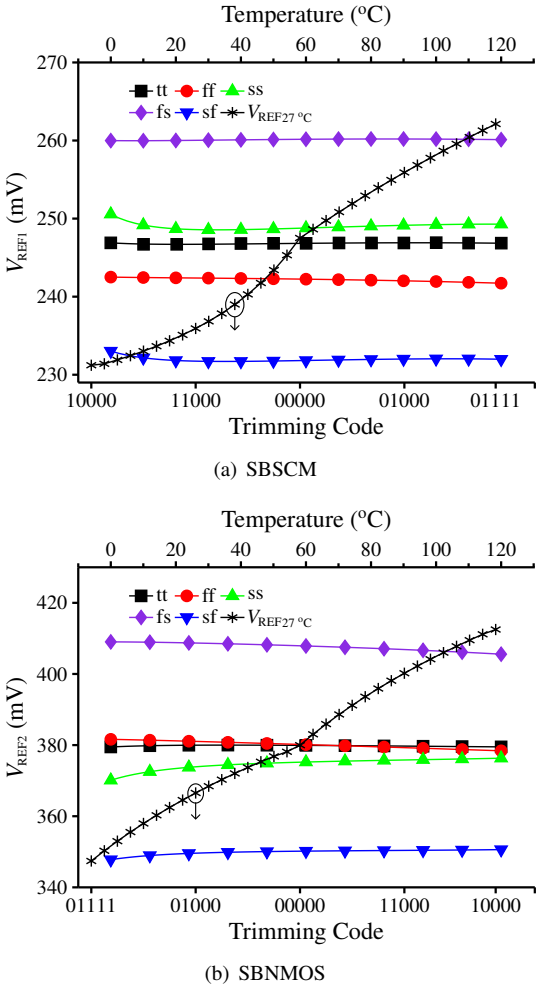
The SBNMOS can be adjusted by increasing or decreasing the current gain K_1, which is equivalent to adding or sinking current at the reference voltage node. This can be achieved by using a current-trimming technique [15], where the trimming circuit can cover all the variation of the output voltage at room temperature. Defining $V_{FS} = 8\%V_{\text{REF2}}$ and using the same 5 bits as for the SBSCM, lead to $V_{LSB} = 0.3\%V_{\text{REF2}}$. The schematic of the 5-bit trimming circuit of the proposed voltage references is shown in Fig. 11.

The simulation of the trimming circuit, as well as the variation of the output voltage with process corners, is shown in Fig. 12. For both circuits, the increase/decrease of the current gain is defined by the control bits B[4:0], where B[4] is a sign



(a) SBSCM (b) SBNMOS

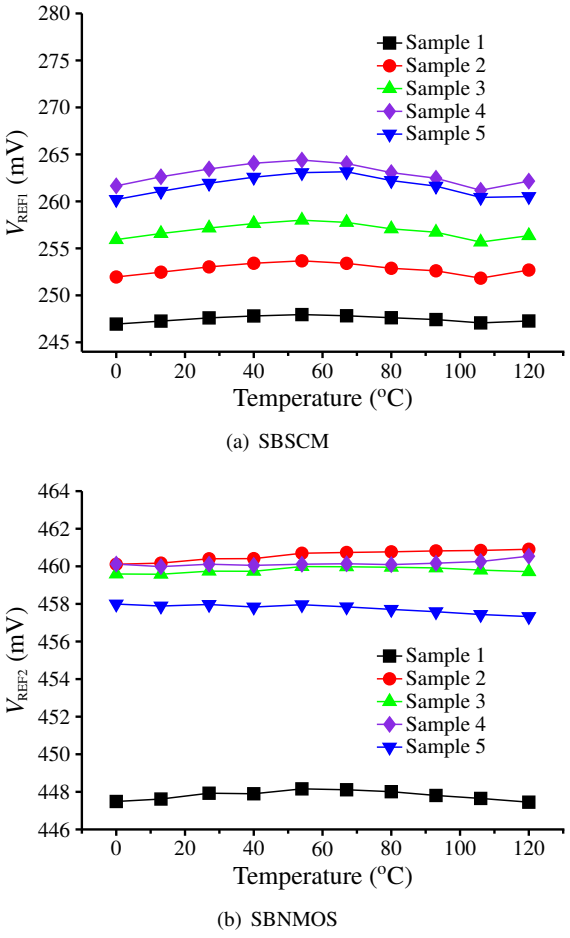
Fig. 11. 5-bit trimming scheme for the proposed circuits.



(a) SBSCM

(b) SBNMOS

Fig. 12. Simulated 5-bit trimming range for the proposed circuits.



(a) SBSCM

(b) SBNMOS

Fig. 13. Measured temperature dependence of V_{REF} for five samples after trimming emulation.

bit that determines the direction of the resulting trim to the output voltage, and B[3:0] are the binary codes proportionally controlling the current mirror gains [16]. As clearly shown by Figures 12(a) and 12(b), the proposed trimming circuits can cover all process variations.

Even though the trimming circuits were not fabricated due to silicon access restrictions, they can be emulated with the assistance of the measurement equipment, since each DC channel of Keysight-4156 can perform a precision programmable current source at the same time it measures the node V_{REF}. This emulation can be made by increasing or decreasing the current at the voltage reference node through the following process: 1) By processing the measured data of a given sample through a mathematical software, an optimal temperature-compensated V_{REFOPT} is obtained; 2) Experimentally, at 27 °C a current (I_T) is sunk or applied to the reference node of the processed sample in order to achieve the same value as V_{REFOPT} in this temperature; 3) The generated currents of the proposed circuits increase exponentially with temperature, hence the

TABLE II
COMPARISON WITH PUBLISHED LOW POWER CMOS VOLTAGE REFERENCES

Specification	[9]	[10]	[11]	[12][a]	[13]	[14]	[15][a]	[17][a]	[18][a]	This Work			
										SBSCM		SBNMOS	
Technology (µm)	0.35	0.35	0.18	0.13	0.18	0.18	0.18	0.35	0.18	**0.18**			
V_{DD} (V)	0.9-4	1.1-4	0.45-2	0.5-3	0.15-1.8	1.2-2.2	0.45-1.8	0.9-3	1.4-3.6	**0.45-3.3**		**0.6-3.3**	
V_{REF} (mV)	670	96.6	263.5	176	17.69	986.2	118.41	713	1250	**225.3**	**256.6**[a]	**378**	**457.1**[a]
Temp. Range (°C)	0-80	-20-80	0-120	-20-80	0-120	-40-85	-40-85	-20-80	0-100	**0-120**			
TC (ppm/°C)	10	11.4	142	29	1462	124	59.4	26	31	**104**	**72.4**[a]	**495**	**11.6**[a]
LS (%/V)	0.27	0.09	0.44	0.036	2.03	0.38	0.033	0.3	0.31	**0.15**		**0.11**	
PSR @ 100Hz (dB)	-47	-60	-45	-51	-64	-42	-50.3	-	-41	**-43.9**		**-46.8**	
Power (pW)	36,000	22,000	2,600	29.5	26.1	114	15,600	2,970	35	**54.8**	**147**[a]	**184**	**664**[a]
Area (mm^2)	0.045	0.0189	0.045	0.0093	0.0012	0.0048	0.0132	0.054	0.0025	**0.002**		**0.0017**	
FoM[b] (°C^3/W×mm^2)	0.0004	0.002	0.0009	1.25	0.315	0.23	0.0013	0.0025	3.68	**1.26**		**1.1**	

[a]After trimming; [b]10^{21};

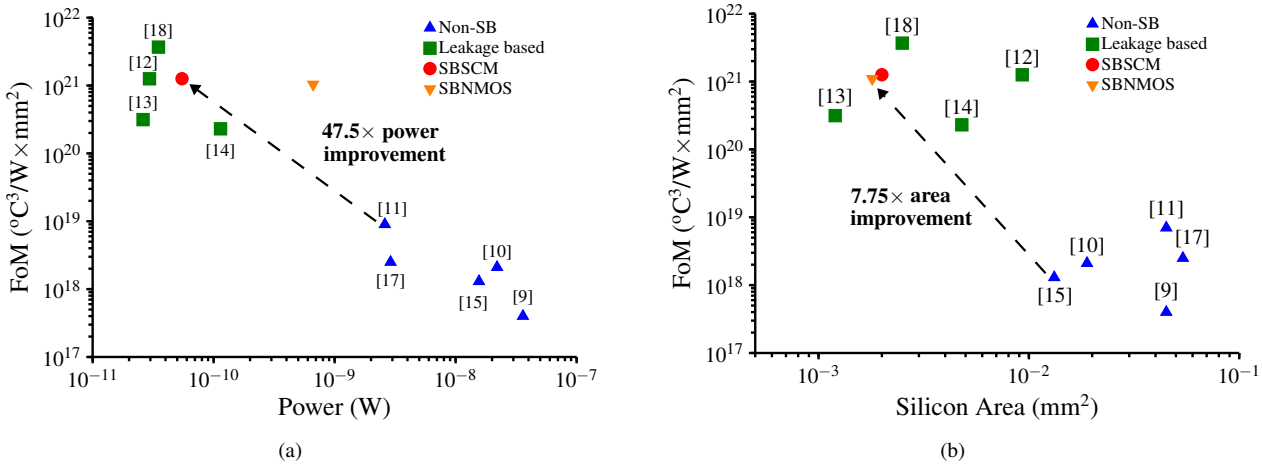


Fig. 14. FoM comparison between the proposed circuits and prior works with respect to (a) power and (b) silicon area.

applied/sunk I_T trimming current must follow this behavior. Using the obtained I_T from the previous step as starting point, the current that must be applied to the other temperature points is achieved by approximating it with a function that increases exponentially.

The measured results after the trimming emulation, as explained before, for five randomly selected samples at minimum supply voltage are shown in Fig. 13. The measured TCs with trimming emulation for the 5 samples of the SBSCM were 34, 60.7, 75.4, 100 and 93 ppm/°C, while for the SBNMOS they were 13.2, 16, 7.25, 9 and 12.7 ppm/°C. The TCs for the SBNMOS were expected to be lower when comparing to those from the SBSCM since the latter circuit presented a more defined CTAT behavior. The TC and power consumption were 72.4 ppm/°C and 147 pW for the SBSCM, and 11.6 ppm/°C and 664 pW for the SBNMOS. Since the trimming circuits were not included in the fabricated references due to silicon access restrictions, the presented emulation approach can help validate the process compensation trimming scheme that was proposed.

VI. COMPARISON WITH PUBLISHED WORKS

The performance of a voltage reference circuit is quantified by many specification parameters as presented in the previous sections, meaning that the performance comparison among different circuit designs and approaches is a complex task. For this reason a Figure of Merit (FoM) can be defined to provide a comparative number that represents the overall performance of a given design.

A FoM that considers the main performance parameters of a voltage reference, such as temperature range, TC, power, and silicon area, can be expressed as [28]

$$\text{FoM} = \frac{(T_{\text{MAX}} - T_{\text{MIN}})^2}{\text{TC} \times \text{Power} \times \text{Area}} \tag{21}$$

First-order compensated voltage references usually present a parabola-like curve across temperature, meaning that as the temperature goes far from the reference point, typically room temperature, the output reference voltage temperature sensitivity increases. Therefore, the temperature range $(T_{\text{MAX}} - T_{\text{MIN}})$ is squared in the FoM expression proposed, benefit designs where a wider temperature range is covered. The product between TC, power at room temperature and silicon area must be as low as possible, meaning that resistorless solutions are benefited since integrated resistors tend to occupy large areas when designed for low currents.

Table II and Fig. 14 summarize the performance of the SBSCM and the SBNMOS in comparison with published low power CMOS voltage references. When compared with the non-self-biased works (Non-SB), the proposed circuits presented a 47.5× and 7.75× of power and area improvement, respectively, while having the best FoM performance. As

Fig. 14 explicitly shows, besides presenting better FoM than Non-SB, the leakage based solutions have the smallest area and power consumption. The performance of both circuits proposed concerning power, area, and FoM are among the best in literature. Although [18] presents a higher FoM, its minimum supply voltage is 1.4 V, which is not suitable for low voltage applications. The SBSCM 0.45 V operation is in the range of ultra-low voltage applications.

VII. Conclusion

Low power and low voltage self-biased subthreshold CMOS voltage references were herein presented. The voltage references are generated with the usage of NMOS devices with different threshold voltages. The power consumption is remarkably reduced by combining subthreshold operation with a self-biased scheme. By employing this approach, two variants of this design were presented: the SBSCM and the SBNMOS. A trimming scheme for both circuits was proposed and analyzed. The proposed circuits were fabricated in a standard 0.18-µm CMOS process. The measurement results from 24 samples show that both circuits can operate at 0.45/0.6 V minimum supply voltage, consuming 55/184 pW at room temperature. The calculated FoM reveals that both circuits are among the best in recent literature. The performance of the proposed circuits makes them suitable for extreme power-constrained applications such as battery voltage supervisors for IoT systems.

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