Analog Curve Tracer

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Contents

1 Abstract

In order to preemptively replace the aging curve tracers in the 6.101 lab, we decided to design a replacement for our final project.

A replacement device should be able to replace the Tektronix 575 in the context of 6.101. This means that it has to be able to generate characteristic curves for BJTs and diodes. Users should be able to easily adjust testing parameters to fit the device being tested, and it should be easy to view and capture the generated curves.

Our design can automatically identify whether the device under test (DUT) is a bipolar junction transistor or a two-terminal device, like a resistor or a diode. If the device is a BJT, it also detects the type (NPN or PNP), as well as its orientation. Based off of this information, it sets up the test and applies the test currents in the appropriate directions. The BJT testing only works if the middle pin is the base, but that is usually the case, so it shouldn't be a problem. Users can adjust various testing parameters through 3 rotary switches.

The output of the curve tracer can be read off of two test points and an oscilloscope in X-Y mode can be used to display the curves generated. This allows for the easy export of the characteristic curves through the oscilloscope's USB port.

2 Project Overview

Our project's circuit can be split into three main parts - the device identification circuit, the control voltage generation circuit, and the two voltage controlled current sources used to test the DUT.

The device identification circuit determines how the testing setup for the DUT should be setup, and includes an array of analog switches in order to connect the device in the way required for testing. The device identification circuit also provides the control voltage generation circuit with two voltages representing the directions of the base and collector currents.

The control voltage generation circuit uses these two voltages, as well as inputs given from the user through three rotary switches, to generate a staircase wave that controls the base current source, and a triangle wave that controls the collector current source. The commanded current is proportional to the voltage.

Finally, the two current sources reference the control voltages to test the DUT by pushing or pulling current through the device. Voltages representing the current through the device and the voltage across the device are available for the user to probe through test points.

3 Design

3.1 Overall System Design

The design involves a discrete sweep of the base current and a continuous sweep of the collector current which was accomplished with two voltage controlled current sources.

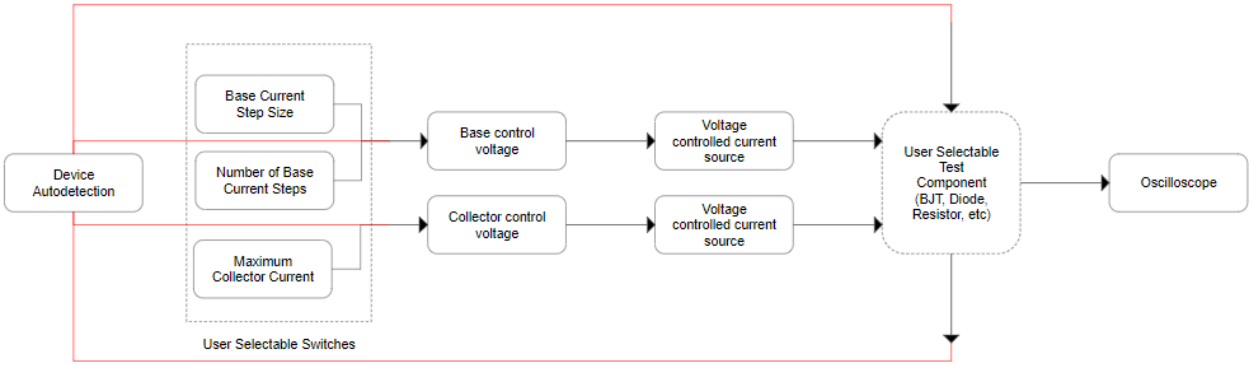

Figure 1: Overall Block Diagram

3.2 User Input

User input for setting the base current step size, number of base current steps, and the maximum collector current is taken through 10 position rotary switches. The switches for base current step size and maximum collector current change the gain of an amplification stage by changing the feedback resistor of an inverting amplifier. The switch for number of base current steps changes the value of a resistor in a voltage divider, changing a reference voltage.

3.3 Automatic Device Identification

3.3.1 Theory

This section of the circuit needs to determine if the DUT is a BJT or a two-terminal device, as well as determine the type and pin orientation for BJTs.

Because BJTs are constructed by sandwiching one semiconductor type between two layers of another, each has two junctions, and thus look like two diodes from the perspective of the base.

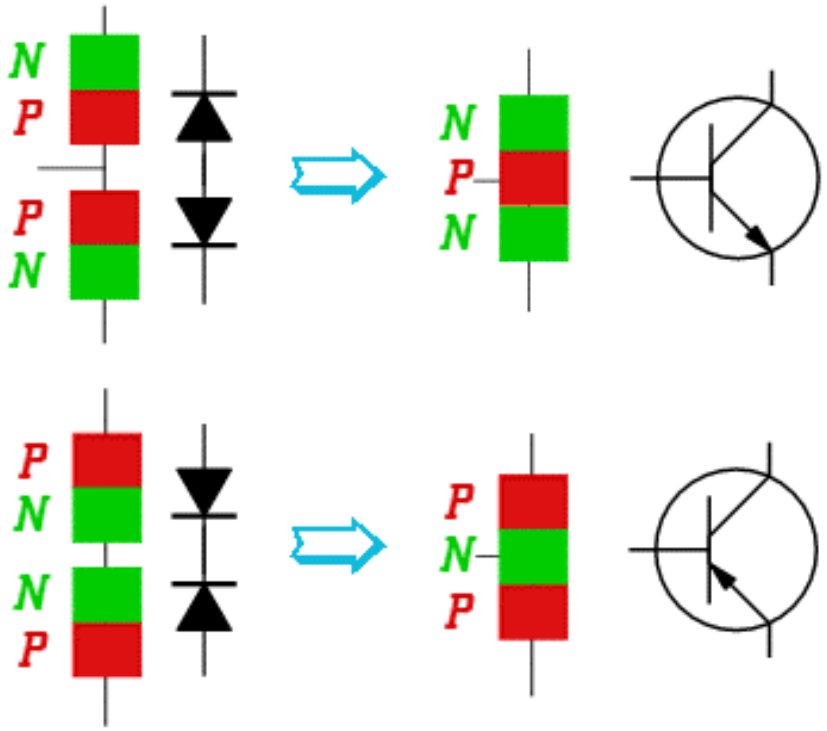

Figure 2: BJTs can be identified because they can look like two diodes from the perspective of the base. Source: http://fourier.eng.hmc.edu/e84/lectures/ch4/node3.html

A BJT can be identified by looking for these diode drops when the emitter and the collector are grounded through resistors, and a test voltage is applied to the base. For a PNP type BJT, the diode drops will appear when the test voltage is negative. For a NPN type BJT, the diode drops will appear when the test voltage is positive. When the test voltage is the wrong polarity for the type of device, the voltage drop will be the full test voltage. This allows for the identification of the type of device.

Because of differences in doping concentration (the emitter region is typically doped more heavily than the collector), the base-emitter diode drop is typically larger than the base-collector diode drop. This allows for the identification of these two pins.

Both of these methods require knowledge of which pin is the base of the device. Because this is the center pin for the BJT packages available in the lab, this was assumed to be known.

3.3.2 Implementation

The electronics that implement the device identification circuit consists of a sawtooth wave generator, window comparators, XOR gates, S/R latches, and opamp subtractors. The circuit controls an array of analog switches used to set up the testing conditions for the device.

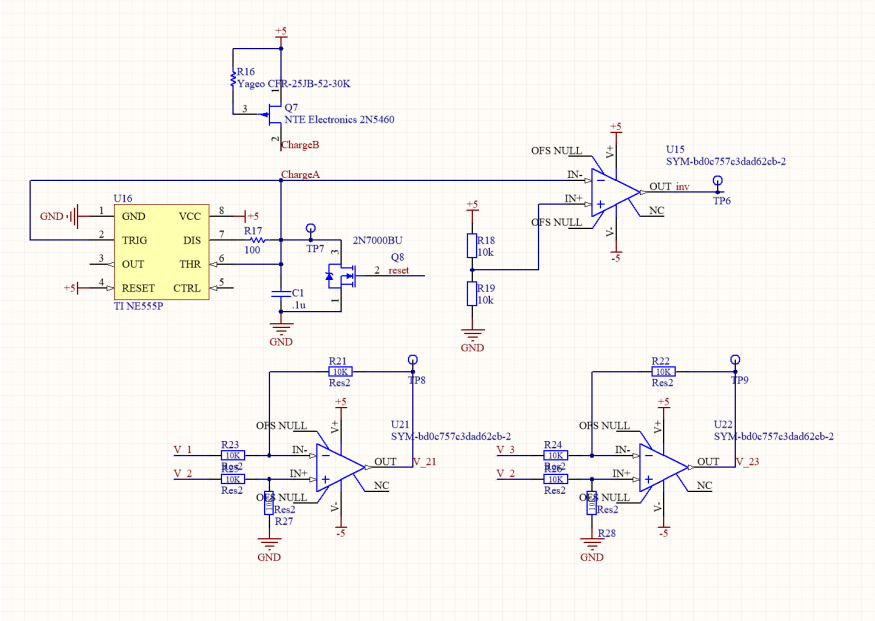

Figure 3: Sawtooth Generator, Subtractors, and Test Voltage Opamp

The sawtooth generator is implemented with a 555 timer set up in an astable configuration, with the timing capacitor driven by a JFET (2N54560) current source. The JFET current source is connected to the timing capacitor through an analog switch, which allows the circuit to hold the sawtooth voltage by disconnecting the current source. A NMOS (2N7000) connected in parallel with the timing capacitor allows the circuit to reset the sawtooth.

Each window comparator is made from two LM211s, which were chosen for their lower offset voltage when compared to the more common LM311. The reference voltages for the two comparators are set through a three tap resistor divider. By adjusting the values of the resistors in the divider, you can change the range of voltages in which the window comparator will output a logic high. As the output of the comparators are open-collector, they are pulled up to the positive supply rail through a resistor, and are tied together. The other comparators in the design are also LM211s.

Due to PCB size constraints, we opted to use integrated circuits to implement the XOR gates and S/R latches. For the XOR gates, the CD4043B was used, and for the S/R latch, the SN74LS86A was used. Both were chosen because they were not clocked, and were available in through hole packages. S/R latches were chosen instead of a sample-and-hold circuit because they were needed to reset the staircase wave used in the base control voltage, and many integrated circuits had multiple latches available. We can control when these latches sample the input by pulling the set pin to ground, and releasing it when we want to sample.

For the analog switches, we used the ADG441/ADG442 CMOS switches for all the switching where the resistance was not critical. These switches were used instead of MOSFETS because in a lot of the situations where switching is needed, the voltage at the source changes, which makes it hard to turn the MOSFET completely on. Using analog switches simplifies the

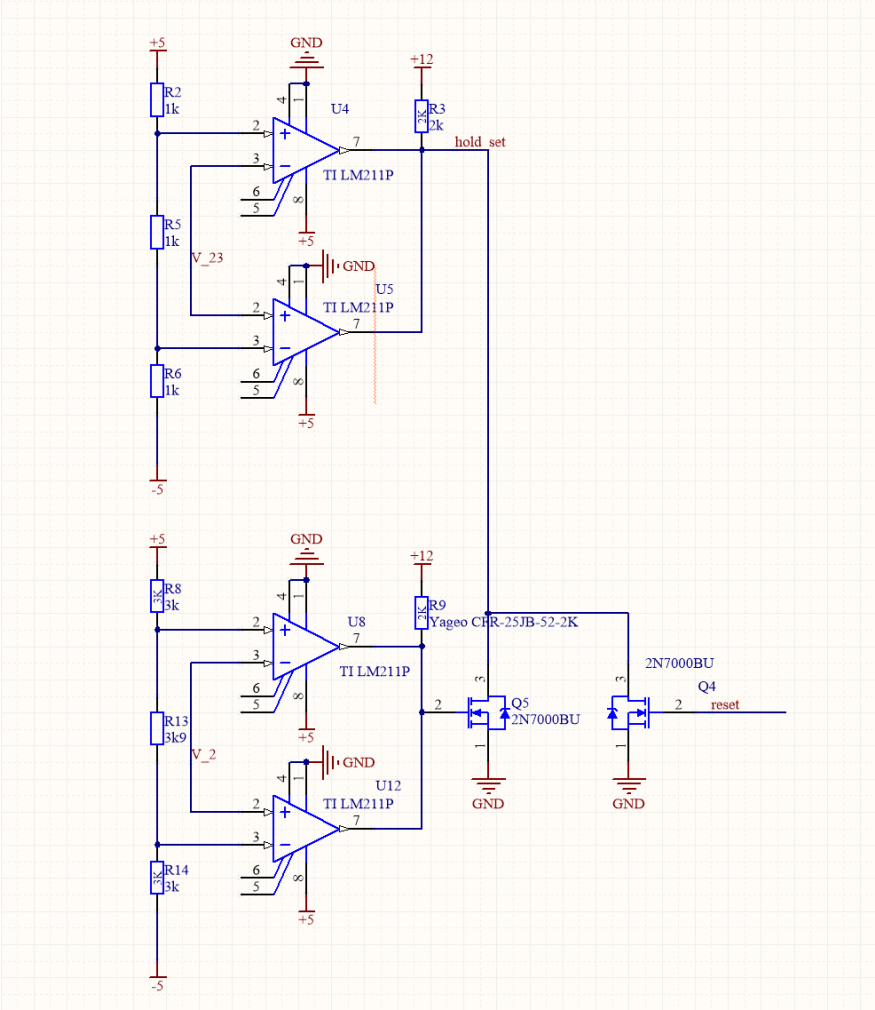

Figure 4: Window Comparator

design greatly, and allows us to switch both positive and negative voltages. To connect the DUT to our testing circuit, we used the MAX4663, which has a much lower on resistance (2.5 Ω), and guarantees break-before-make switching, allowing us to use them as multiplexers.

3.3.3 Operation

The sawtooth wave generator controls the entire device identification cycle, with different portions of the wave corresponding to different tests that the circuit performs. When the circuit has successfully identified a device, the circuit holds the sawtooth voltage constant while the device is being tested by disconnecting the JFET current source. Once testing is over, the sawtooth voltage is reset to 0 and the cycle restarts. Throughout the entire device identification cycle, the pins 1 and 3 are grounded through resistors. This is done through analog switches.

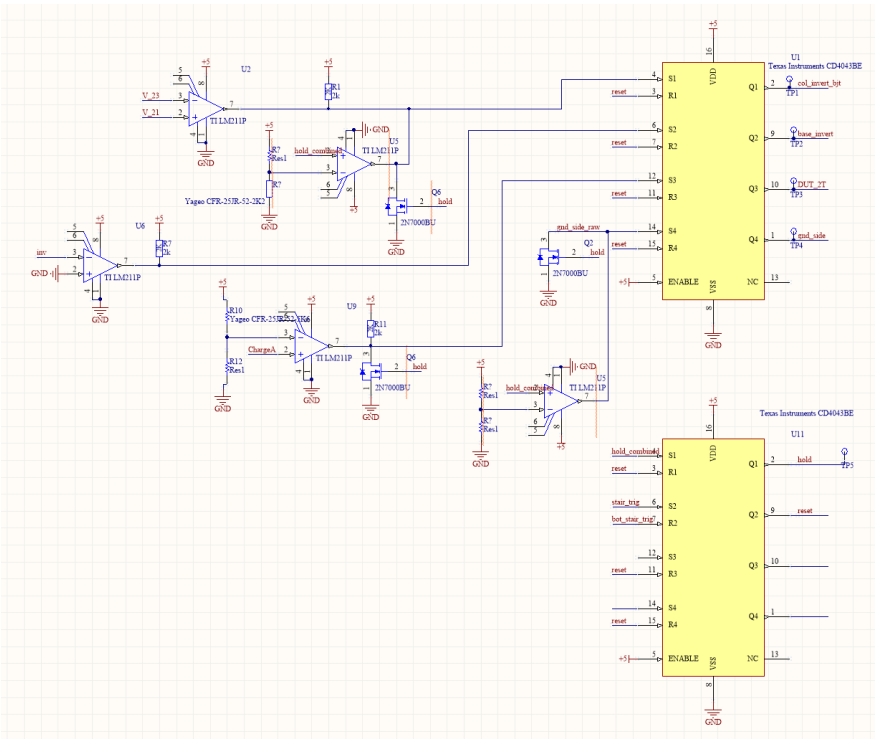

Figure 5: S/R Latches

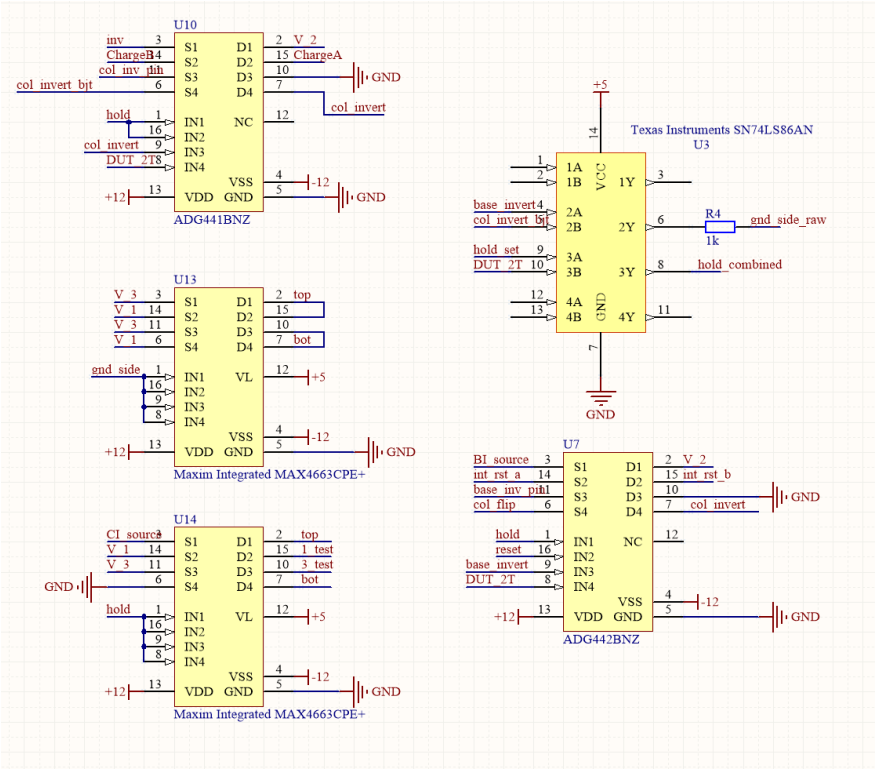

Figure 6: Analog Switches and XOR Gates

Throughout the entire testing period, the voltage drop between pins 2 and 3 ($V_{2,3}$), as well as the voltage drop between 2 and 1 ($V_{2,1}$) are measured. These two voltages are fed into a comparator that goes high when $V_{2,1} > V_{2,3}$. This result can be XORed with the output of a comparator representing the inverse of the test voltage (high if negative test voltage, low if positive voltage) to produce a voltage which pin is the emitter of the device, which should be grounded during the testing cycle (GND Side). The inverse of the test voltage represents whether current should be pushed or pulled out of the base, as well as whether current should be pushed or pulled out of the collector. These values sampled and held in S/R latches when the device identification cycle ends and the testing cycle begins. These two voltages are used as inputs to an array of analog switches that connect the DUT to the testing setup in the correct way, and determine if the base and collector control voltages are inverted or not.

These relations can be seen in Table 1.

Device Identification Truth Table			
$V_{2,1} > V_{2,3}$	$V_{test} < 0$	Collector and Base Current Direction	GND Side
1	1 (PNP)	1 (Pull)	0 (Pin 1)
1	0 (NPN)	0 (Push)	1 (Pin 3)
0	1 (PNP)	1 (Pull)	1 (Pin 3)
0	0 (NPN)	0 (Push)	0 (Pin 1)

Table 1: Truth Table relating measured values to testing parameters

For the first third of the sawtooth, the circuit checks to see if the DUT is a NPN BJT by applying 5V to pin 2. If $-1.66 < V_{2,3} < 1.66$, and ($V_{test} > 2$ or $V_{test} < 2$), the HOLD latch is set, the sawtooth voltage is held, and the device is tested using the parameters determined from the circuit. This ends the device identification cycle and starts the testing cycle.

For the middle third of the sawtooth, the circuit checks if the DUT is a PNP BJT by applying a negative voltage (-5V) to the base. $V_{2,3}$ and the test voltage are checked again, and if the device passes, the device is tested.

If both of these tests fail, the sawtooth is allowed to reach its peak. When this happens, the device identification circuit assumes that the DUT is a two-terminal device. This sets a latch corresponding to this specific device type, which in turn connects the output pin of the 555 used for the triangle generation to the control pin of the analog switch used to invert the triangle wave. This inverts the control voltage waveform halfway through the sweep, switching the test current from positive to negative, and allowing for the full testing of diodes and resistors. When testing these devices, the middle pin remains unconnected.

3.4 Control Voltage Generation

The control voltage generation is accomplished by two parallel circuits, one that makes triangle waves for the collector current source, and one that makes a staircase wave for the base current source. Both of these circuits are triggered by a pulse generator, which allows the collector current sweeps to be aligned with a base current step.

3.4.1 Pulse Generator

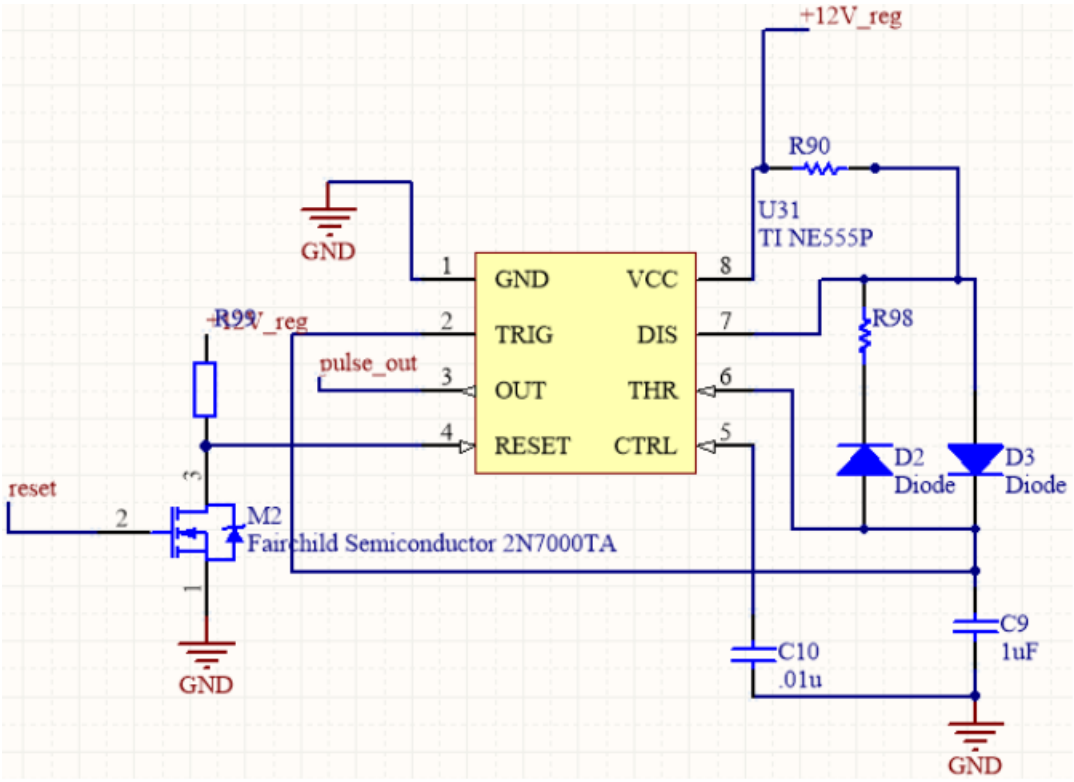

Figure 7: Pulse Generator Circuit

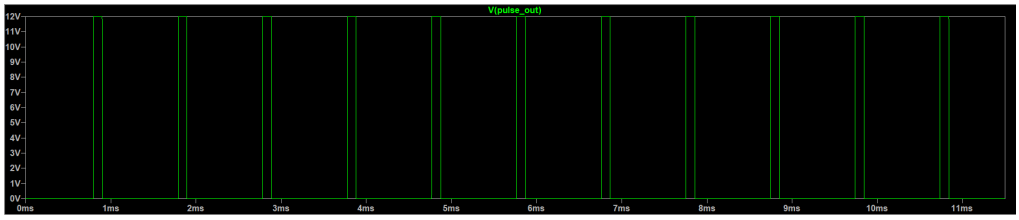

Figure 8: Pulse Generator Output Waveform

The pulse generator is implemented with an astable 555 timer circuit, with separate charging and discharging paths for the capacitor gated by diodes. This allows for a low duty cycle

and easy control of the on and off times. The reset pin is held high when HOLD is high, signaling a testing cycle and enabling the 555 timer.

3.4.2 Staircase Wave Generation

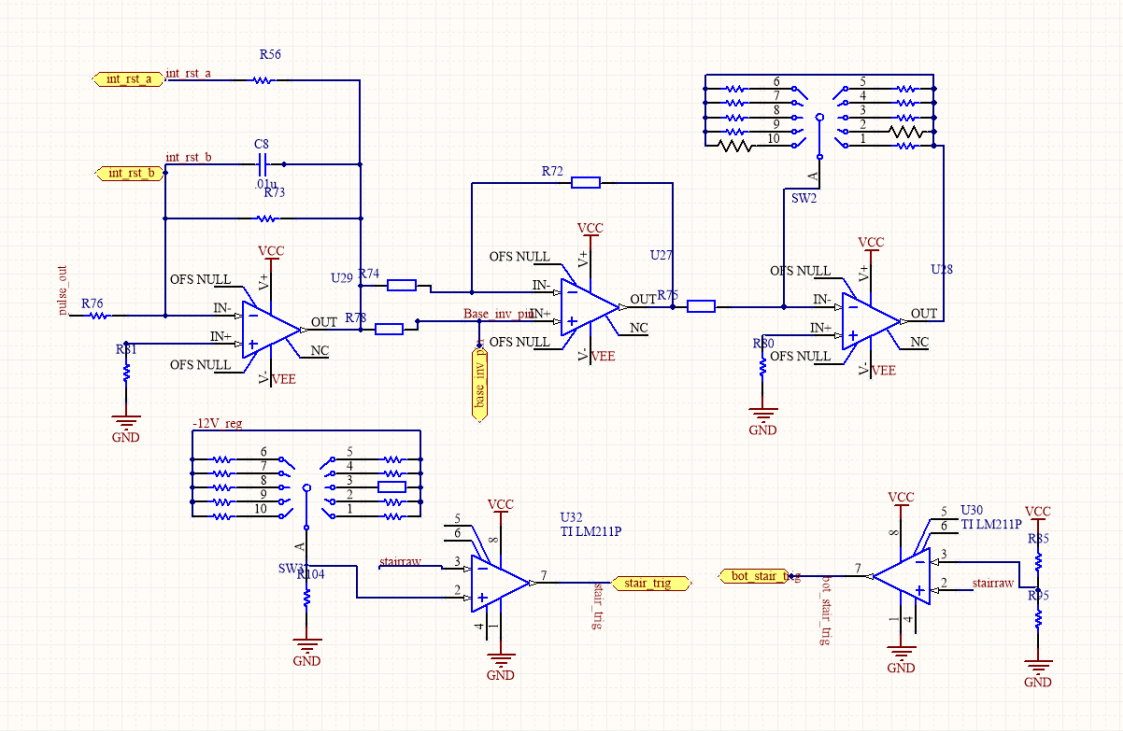

Figure 9: Staircase Wave Generator Circuit

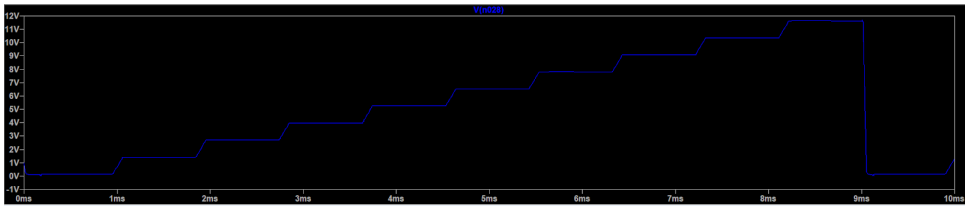

Figure 10: Example Staircase Waveform

The staircase wave is generated by integrating the pulses from the pulse generator using an opamp integrator. Once the staircase reaches a threshold voltage set by the user, the RESET S/R latch is set and the charge out of the integrating capacitor is drained out through an analog switch. When the voltage across the capacitor is close to 0V, the latch gets reset and the integrator is re-enabled. This allows the user to set the number of steps in the base current sweep.

Following the integrator, the wave goes through a unity-gain inverting/non-inverting opamp stage, where the wave can be inverted by pulling the non-inverting terminal of the opamp to ground. This stage is controlled by the device identification circuit through an analog switch. After this stage, the staircase goes through an inverting amplifier, where the gain is set by the user. This allows the user to control the size of the base current steps. The resulting waveform is fed to the base current source.

3.4.3 Triangle Wave Generation

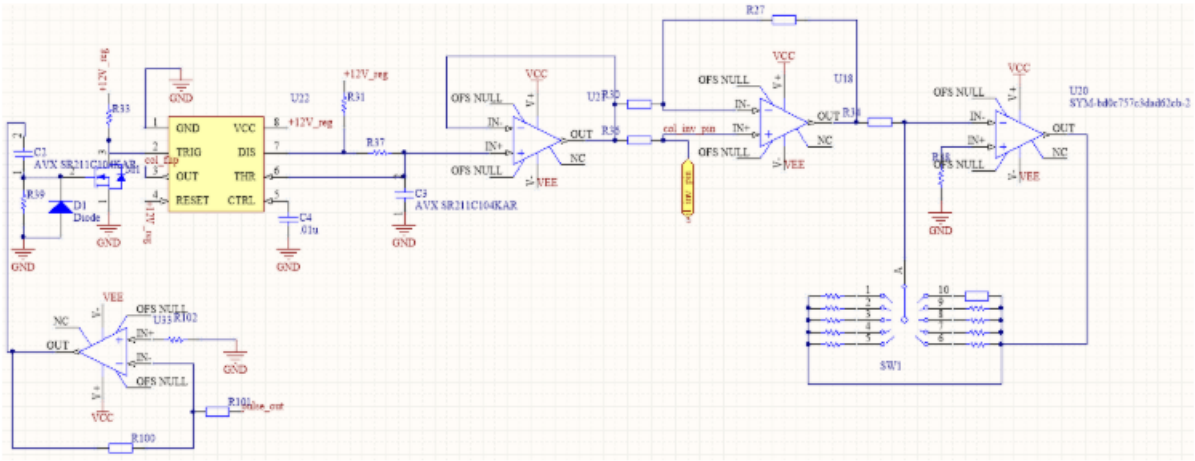

Figure 11: Triangle Wave Generator Circuit

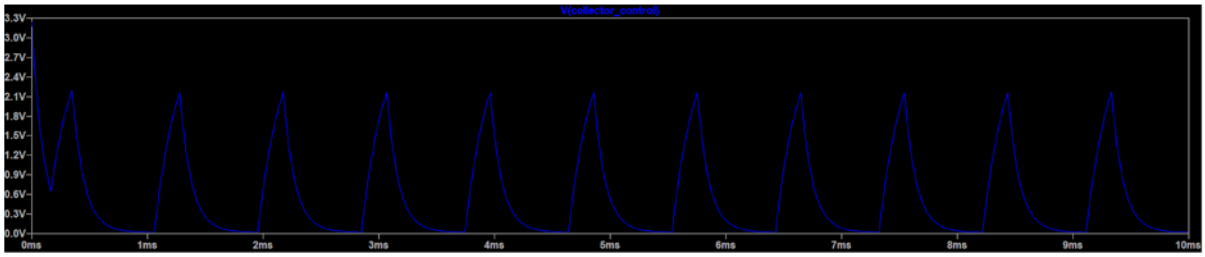

Figure 12: Example Triangle Wave

The triangle wave is generated using a monostable 555 timer circuit, with roughly equal charging and discharging times. One charge-discharge cycle of the timing capacitor happens in the period between pulses from the pulse generator. The pulses from the pulse generator are inverted and differentiated using an passive RC differentiator to act as the trigger for the circuit. This triggers the circuit on the falling edge of the pulse, which allows the base current to stabilize before the collector current sweep starts. The shape of this wave is not critical, and so a constant current source was not needed to charge the capacitor.

The output is taken across the timing capacitor, buffered and then sent through an identical set of processing stages. For the triangle wave, adjusting the gain of the inverting stage allows users to change the maximum current sent through the device.

3.5 Voltage Controlled Current Sources

The voltage controlled current sources consist of two circuits. One is connected to the pin 2 of the DUT and is controlled by the staircase wave generator. The other is connected to the collector of a BJT DUT or a pin on a two-terminal DUT and is controlled by the triangle wave generator.

3.5.1 Base Current Source

The base current source should discretely input different currents into pin 2 of the DUT. The step size and number of steps are set by the user input rotary switches.

The input from the Staircase Wave Generator will go into a Howland Current Pump which can sink or source up to 1.1mA of current depending on the input voltage.

Since the resistors in the Howland Current Pump have to be well matched, .1 percent tolerance resistors were chosen and spots for potentiometers in line with the resistors were added so the resistance could be precisely matched if the .1 percent tolerance was not tight enough.

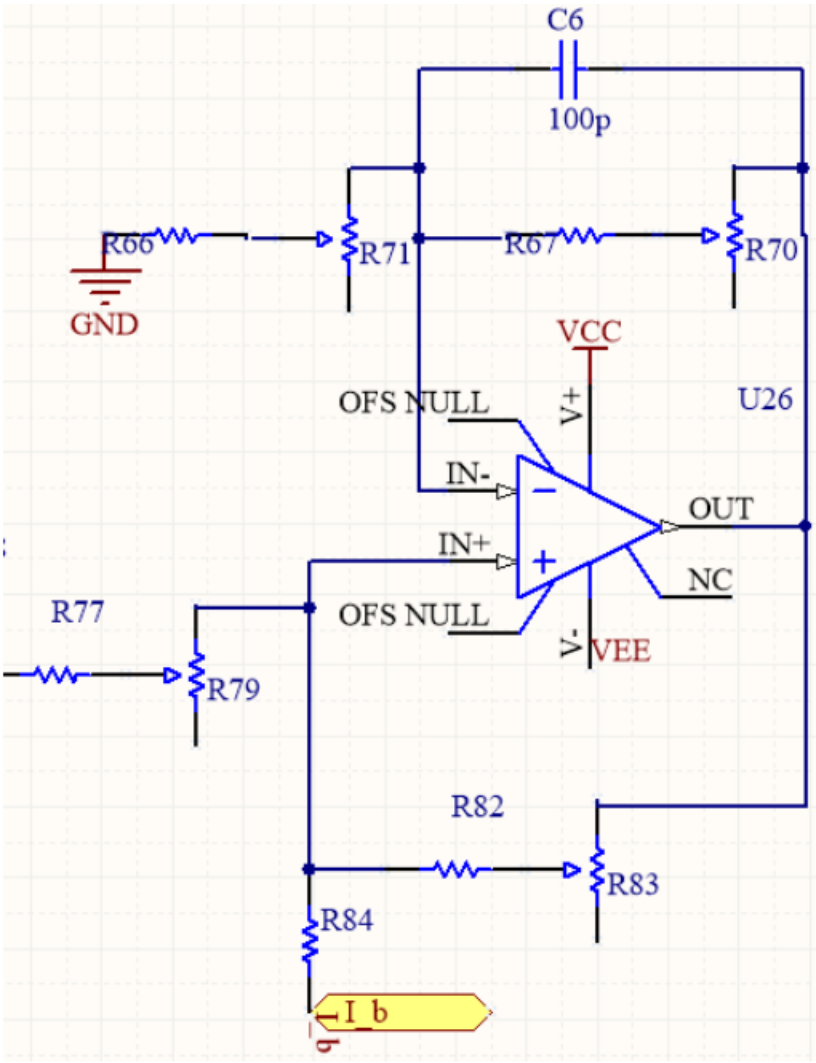

Figure 13: Howland Current Pump

The current flowing out of R84 is the current flowing into pin 2 of the DUT. That current is the combination of the current flowing through R79 and R82. The Howland Current Pump adjusts the currents through R79 and R82 to keep the output current constant for each reference voltage input.

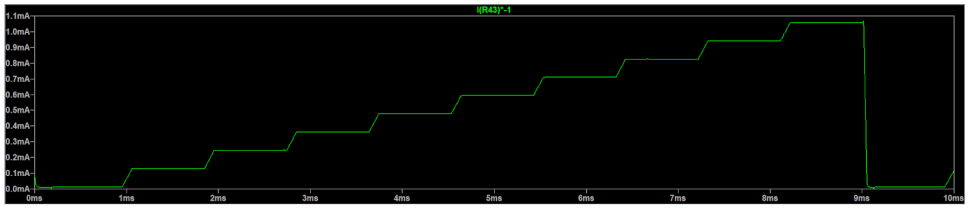

Figure 14: Example Base Current Staircase Wave

3.5.2 Collector Current Source

The collector current source should do a continuous sweep of different currents into the collector terminal of a BJT DUT. The max collector current is set by the user input rotary switches.

The input from the Triangle Wave Generator will go through an opamp into a pair of PNP and NPN BJTs in a push-pull configuration. The opamp will get feedback from an instrument amp measuring across a shunt resistor in the current path. This current source is able to source or sink up to 100mA of current depending on the input voltage.

The instrument amp is unity-gain. The original version of this system had some noise that was also getting amplified, so to reduce this the instrument amp gain was reduced, the OP27 was used because of its low noise characteristics, C5 and C7 were added to create a low pass filter, and a small R35 (30 ohms) was added to increase the damping ratio of the system.

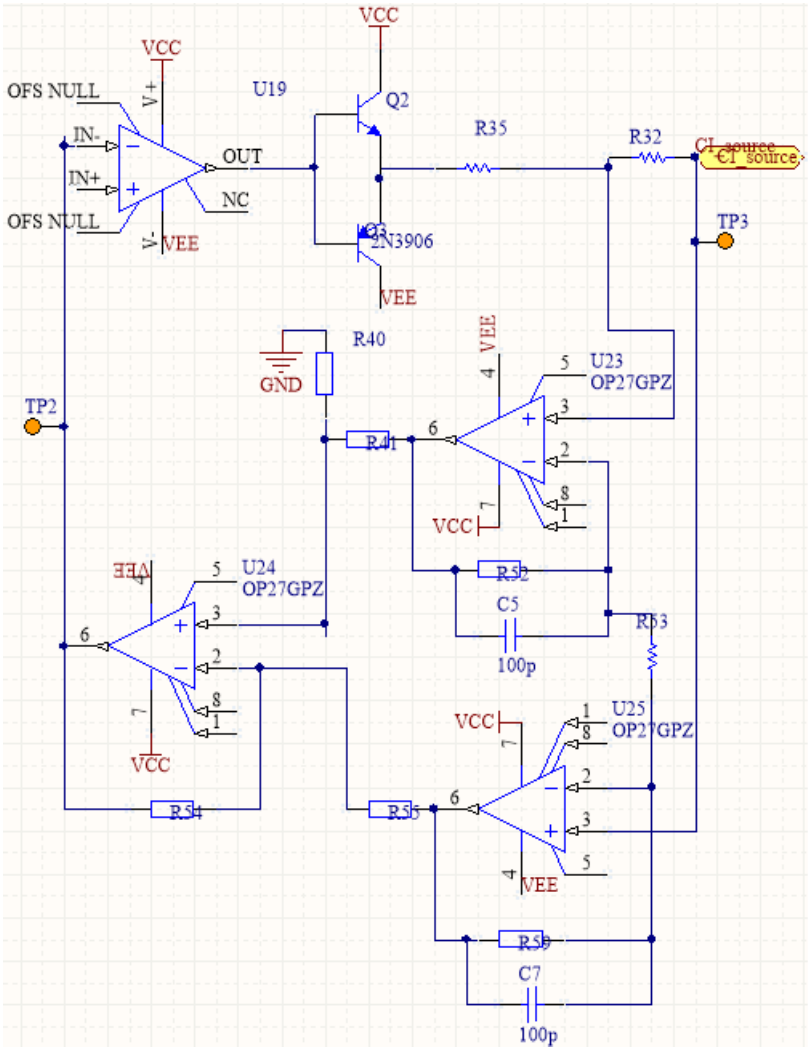

Figure 15: Push-Pull Current Source

The negative feedback across the R32 which is the output resistor helps to ensure that the voltage across the resistor is the same as the triangle wave input voltage on the positive input pin of the op amp.

The voltage between pins 1 and 3 will be measured by measuring the collector voltage of the current source (Test Point 3) since the other pin is grounded. The current will be measured on the output of the instrument amp providing feedback to the collector current source (Test Point 2) using another oscilloscope probe.

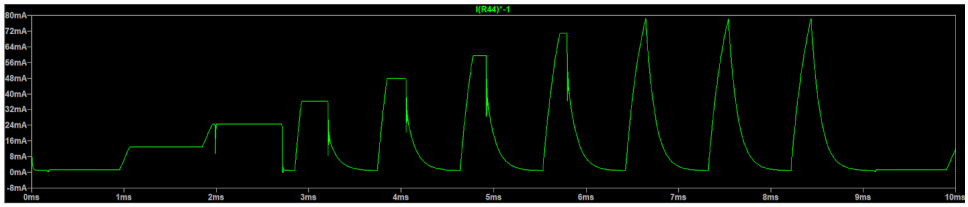

Figure 16: Esample Collector Current Sweeps

Notice that it doesn't always reach its peak. That is because it is limited by the ±15V rails.

4 PCB Layout

Because the maximum size for cheaply manufacturable PCBs is 10cm x 10cm, our entire design was unable to fit on one board. Instead, the design was split into two stacked PCBs, connected with a 16 pin header. Even though the design was spread over 2 PCBs, the top PCB is still completely filled with components, and the bottom PCB had to use SMD parts (1206) for the resistors used in the user input circuit in order for everything to fit on the bottom PCB.

The top PCB has the ±15V inputs, and linear regulators to make the ±5V and ±12V rails. It also contains the socket for the DUT, and the device identification circuit. This board has a cutout that the rotary switches can be accessed through.

The bottom PCB has the control voltage generators and the current sources, as well as the switches used for user inputs. There are test points acting as outputs for the oscilloscope at the back of the board.

4.1 Top PCB

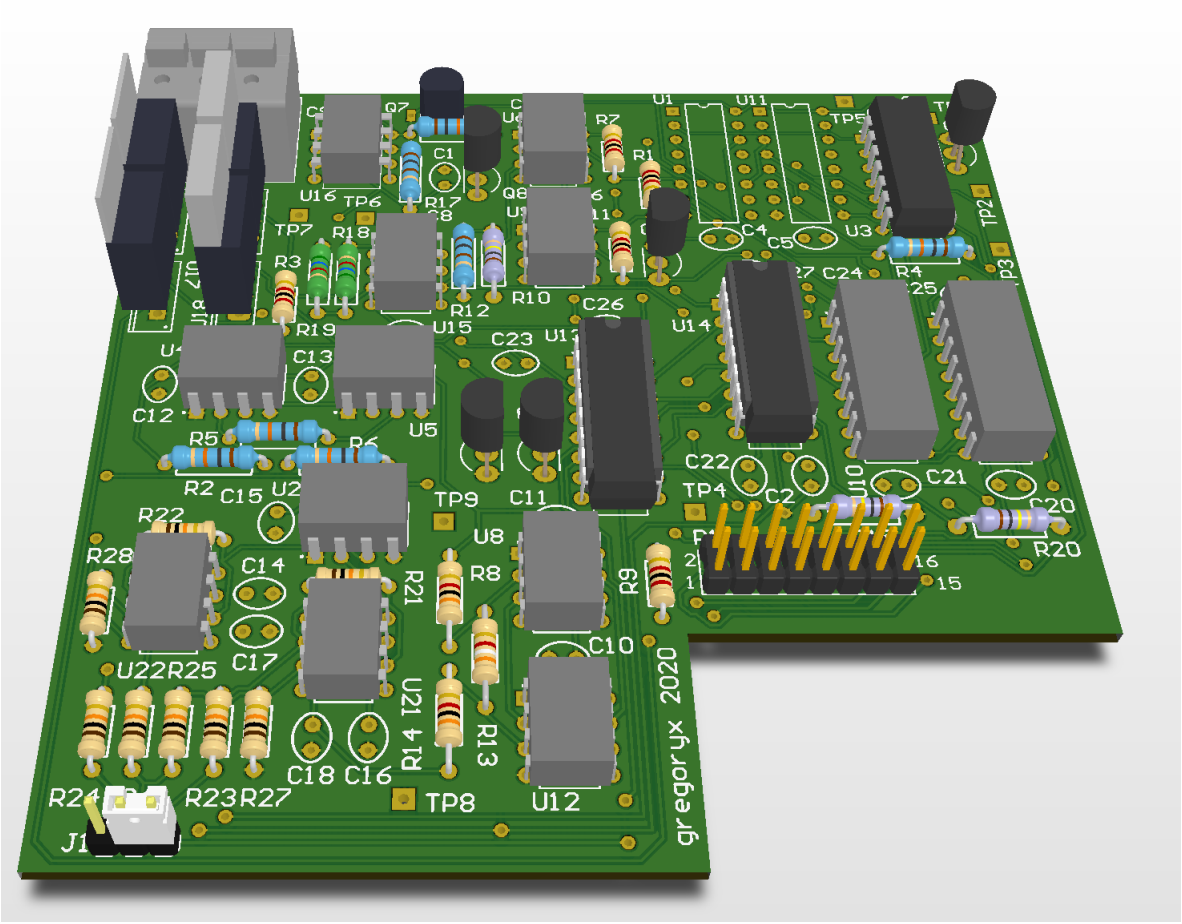

Figure 17: Top PCB 3D View

While laying out and routing this board, care was taken to put the subtractors that made $V_{2,3}$ and $V_{2,1}$ as well as the comparator comparing these two values close to the DUT. For some devices, the difference between these two voltages can be only a couple of mV.

The 16 pin header would be soldered onto the board such that the pins were facing down to interface with the bottom PCB.

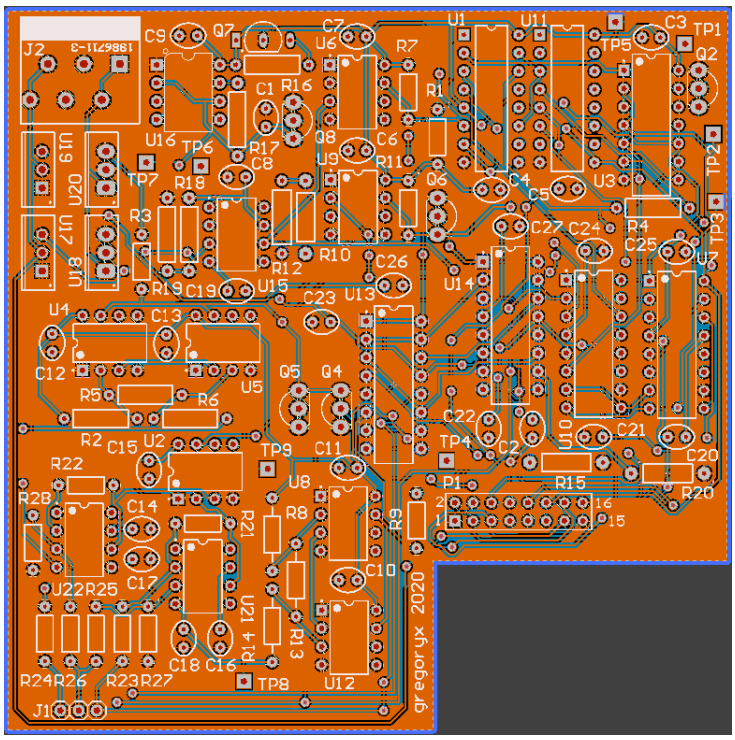

Figure 18: Top PCB Top Layer

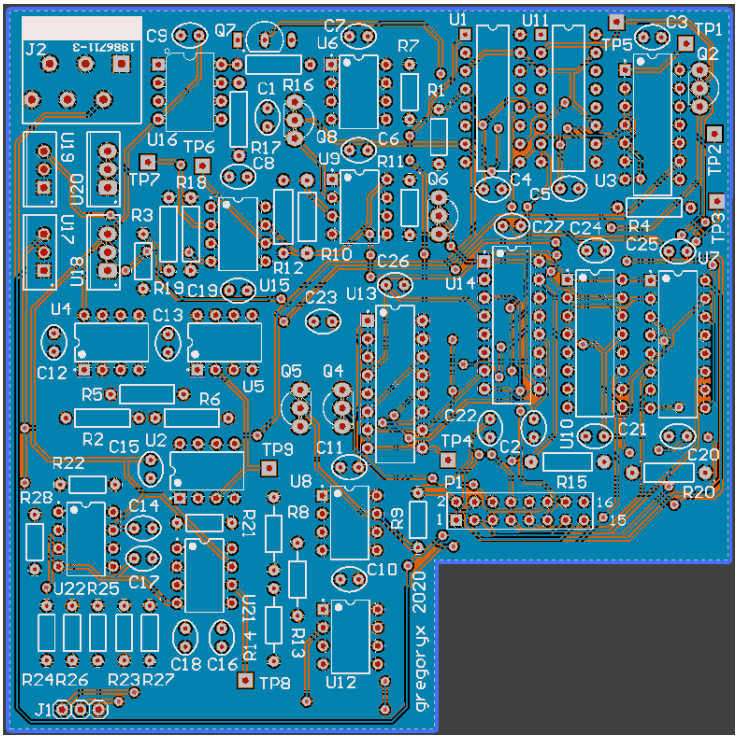

Figure 19: Top PCB Bottom Layer

4.2 Bottom PCB

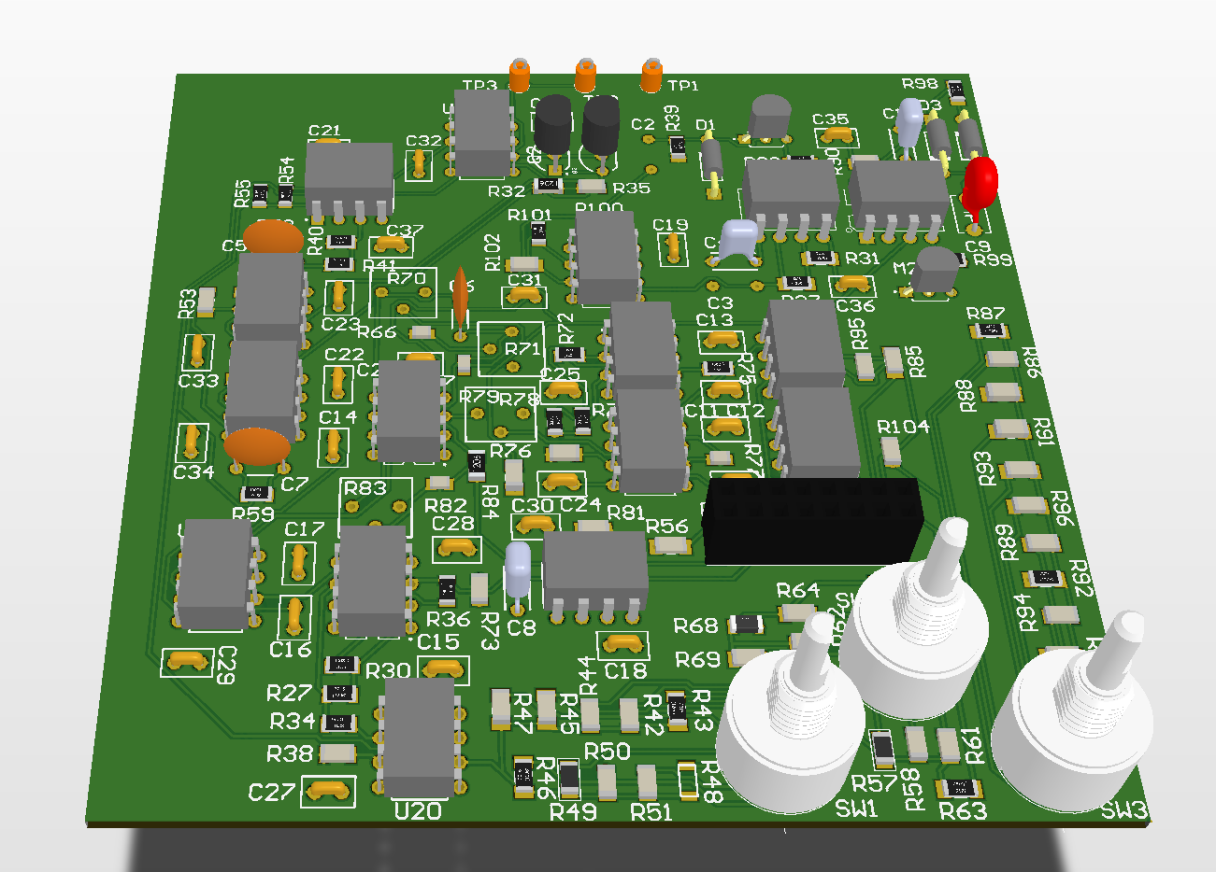

Figure 20: Bottom PCB 3D View

The test points would likely be rotated 90 degrees from how they are shown in this CAD model for ease of connection. Test Point 1 is a ground.

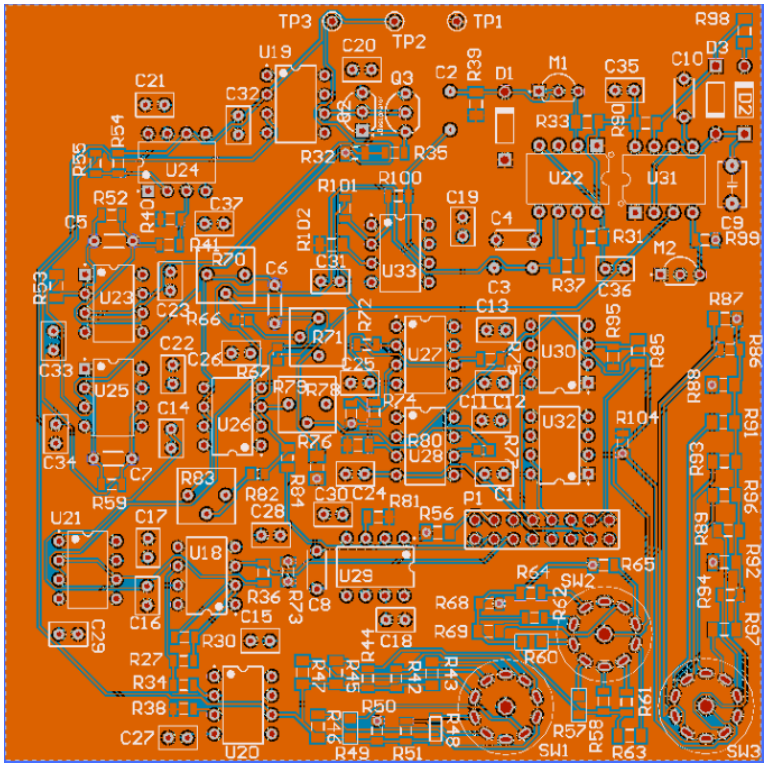

Figure 21: Bottom PCB Top Layer

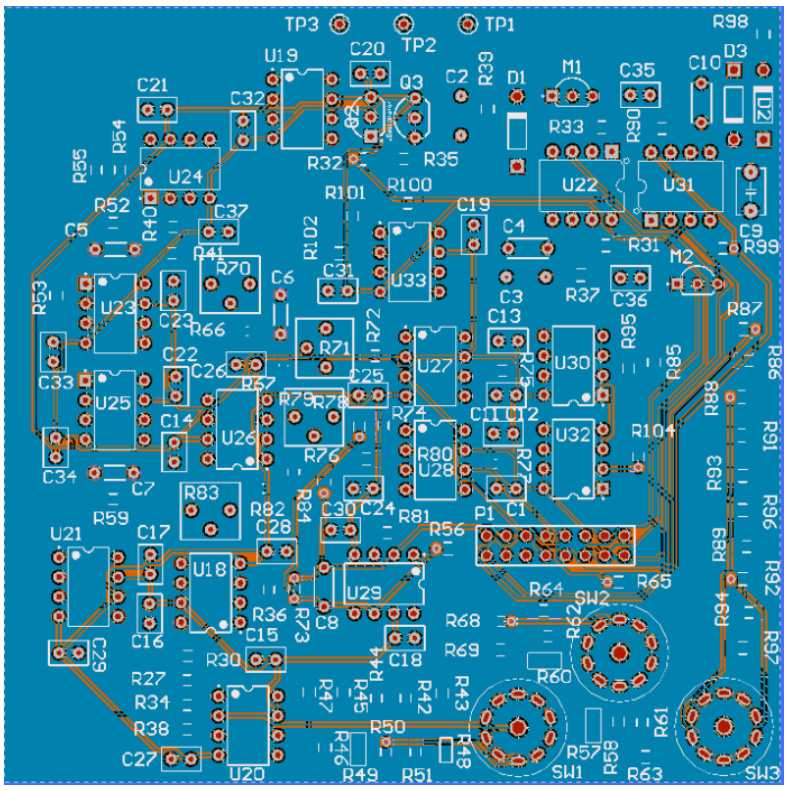

Figure 22: Bottom PCB Bottom Layer

5 Conclusion

As is, the project works as expected in simulation. The generated characteristic curves are readable, with some small artifacts.

5.1 Challenges

1. LTSpice can be tempermental and can also take a lot of time to simulate, so some design and component choices were made because they caused the simulation to run the fastest and most consistently. This was especially important for the final project this year because our entire design had to work in simulation.

2. Integrating automatic device detection with the rest of the circuit was difficult, as the test device has to switch between being connected to the detection circuit, and the testing circuit. This caused lots of problems with the simulation.

5.2 Improvements

In simulation, our design works as is, but there are some improvements that would have been implemented if there was more time and board space.

1. Add a boost power supply to increase the voltage rails.

   In our current design, the highest voltage that can be applied to a device is 15V. By implementing a boost power supply, the curve tracer would be able to apply higher voltages to the DUT, allowing larger current sweeps.

2. Add potentiometers to trim the base control voltage generator.

   Currently, there is no way for the user to adjust the values of the passive components used in the control voltage generation circuit without replacing the components outright. This does not matter much for the collector control voltage, but can influence the size of the base current control voltage steps. When calculating the β of a device, this can introduce error.

3. Bus capacitors for the collector current source.

   The amount of current that the collector current source provides changes at around 1 KHz, and can introduce noise into the power rails. By adding bus capacitors close to the current source, they act as local energy sources, reducing the voltage fluctuations on the power rails.

5.3 Simulation Results

Many of the characteristic curves have artifacts from the connection and disconnection of the current sources from the DUT.

5.3.1 2N3904

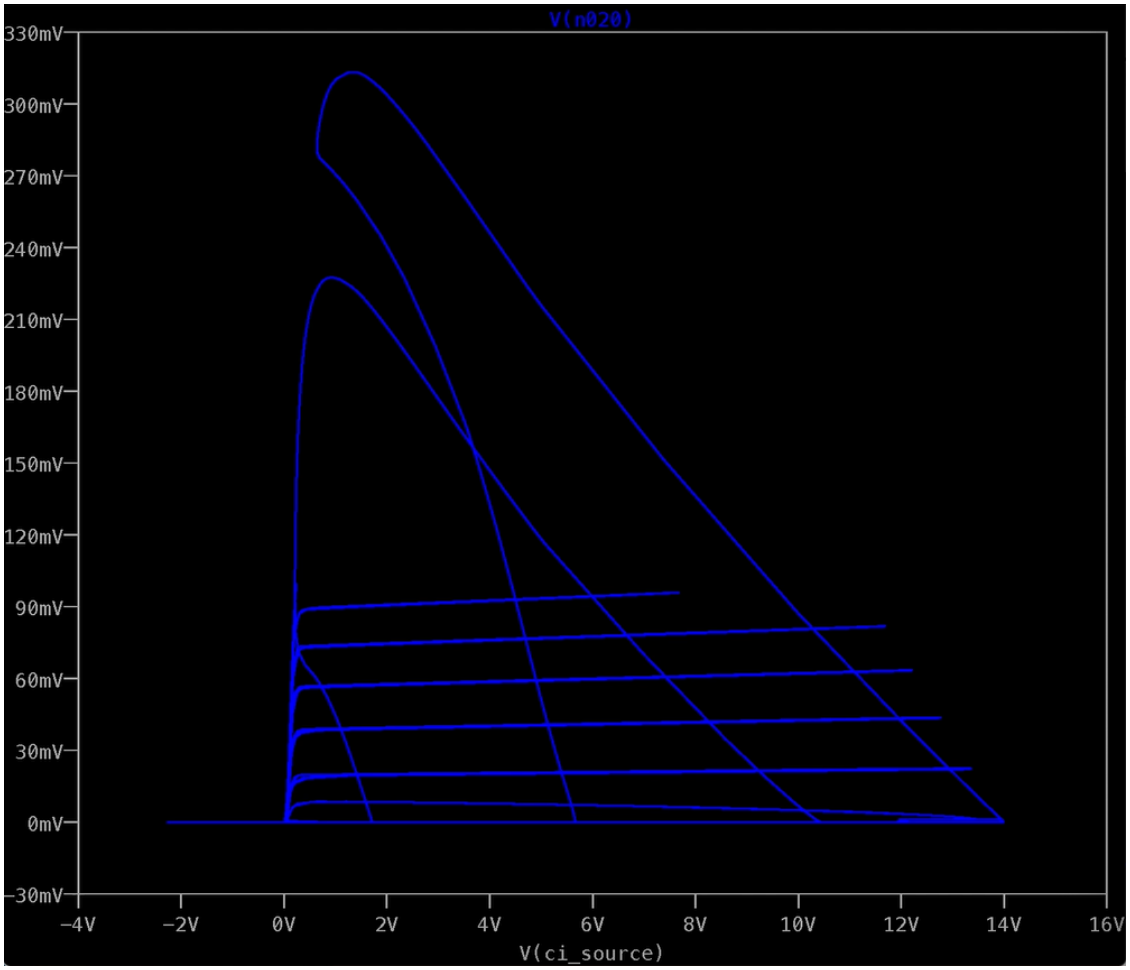

Figure 23: 2N3904 Characteristic Curves

5.3.2 2N3906

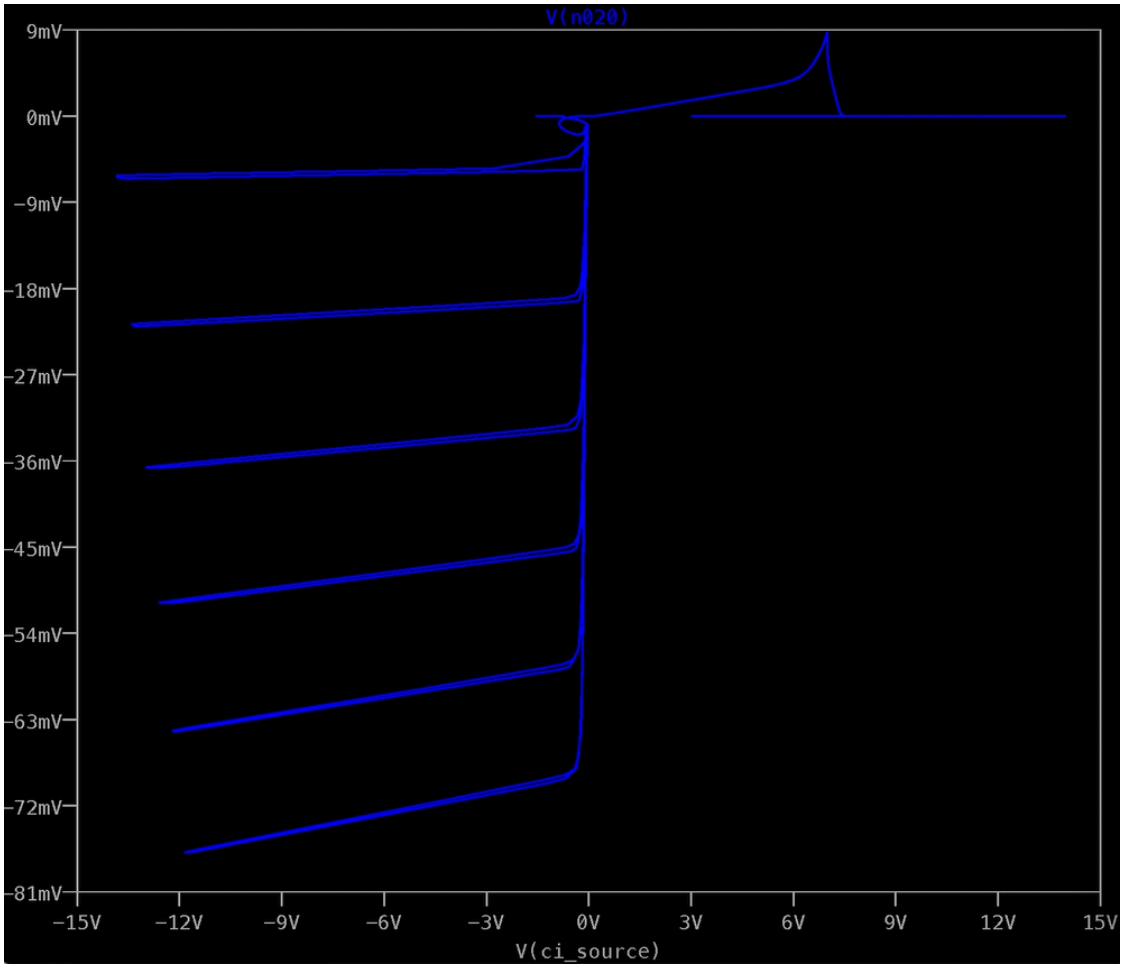

Figure 24: 2N3906 Characteristic Curves

5.3.3 1N914

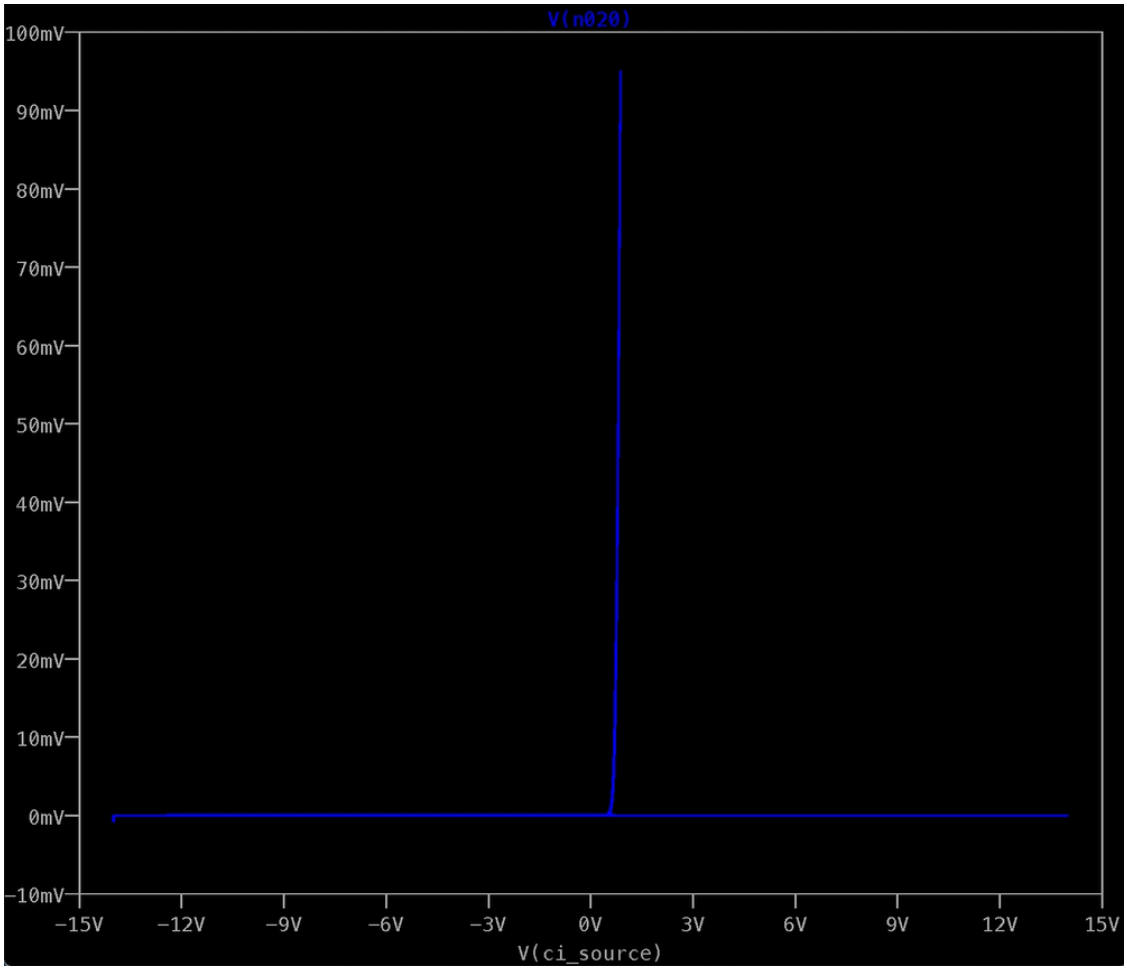

Figure 25: 1N914 Characteristic Curve

5.3.4 10 Ohm Resistor

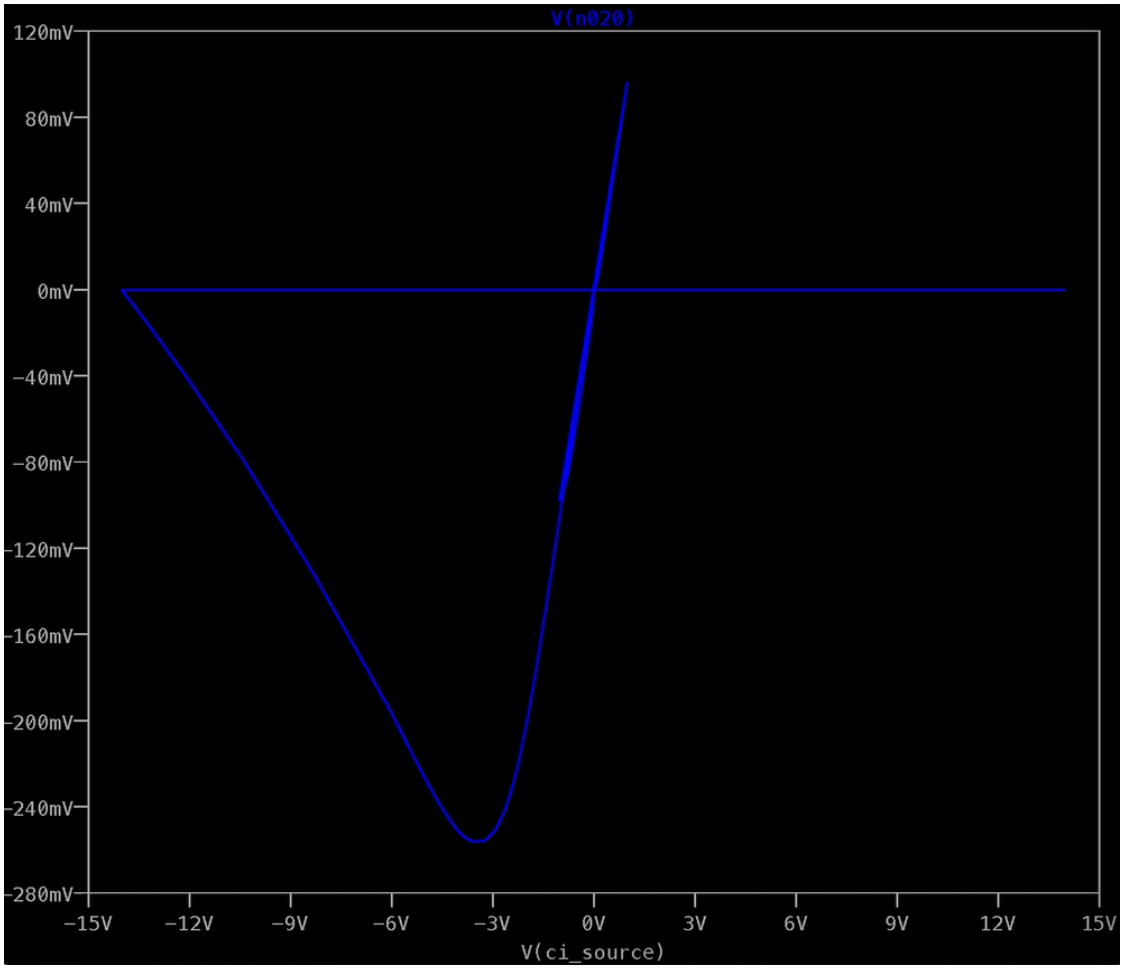

Figure 26: 10 Ohm Resistor Characteristic Curve

5.3.5 Link To Testing Video

Full:

http://dropbox.com/6.101FinalProjectTesting

8 Times Speed:

http://dropbox.com/6.101FinalProjectTesting8x