M A S S A C H U S E T T S I N S T I T U T E O F T E C H N O L O G Y
DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

6.111 Introductory Digital Systems Laboratory
Fall 2019
Lecture PSet #4 of 8

Due: Upload as PDF by 14:30 - Tue, 09/24/2019
Note: Please type your solutions; no credit for hand written solutions

Optional docx available for submission

Problem 1 [6 points. In many digital systems, exact values are not required especially when humans are involved. One example is the refresh rate on a hex display. As long as the refresh rate is greater than 60Hz, the eye will not be able detect the difference. (Gamers, however, will argue that higher better.) Other situations such as control systems may require exact values where even a single bit error will result in failure. This problem will test your understanding in calculating values.]

In lab 2 and lab 3, different Verilog modules were provided to drive the 8 seven segment display. As with many digital designs, both appear to the human eye to work but not necessarily to specification. Assume the system clock is exactly 100MHz.

1. What is the refresh rate for the digits in the seven segment display with lab 2 implementation? [For many designs, approximate or back of the envelope calculations are fine. For this exercise, give the exact frequency to one decimal place with truncation.]

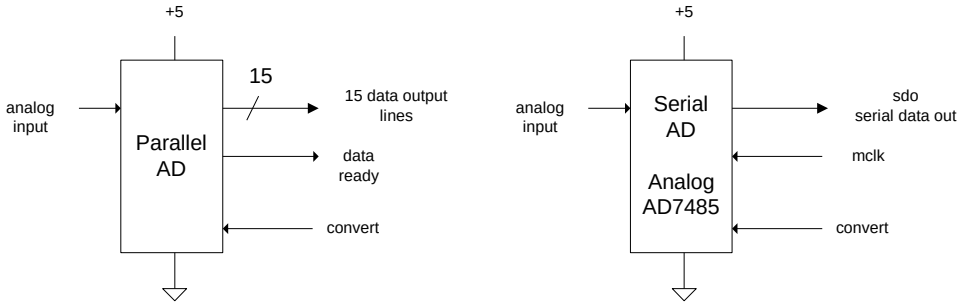
2. What is the refresh rate for the digits in the seven segment display with lab 3 implementation? [For this exercise, give the exact frequency to one decimal place with truncation. You will find that in this case, back of the envelope calculation gave the wrong answer!]

3. The recommended refresh rate is 60Hz to 1KHz Provide one explanation why (in terms of electronics) in this case a faster refresh rate is not better.

4. Modify the Verilog in lab 3 to provide an approximate 500Hz < refresh rate <1000Hz. In your Verilog, include only those line(s) that changed.

A note: The approach to refresh rate in lab 2 results is easier to follow and more useful for someone trying to follow the design. The approach is lab 3 when implemented with discrete IC's results in fewer wires and in Verilog fewer lines of code.

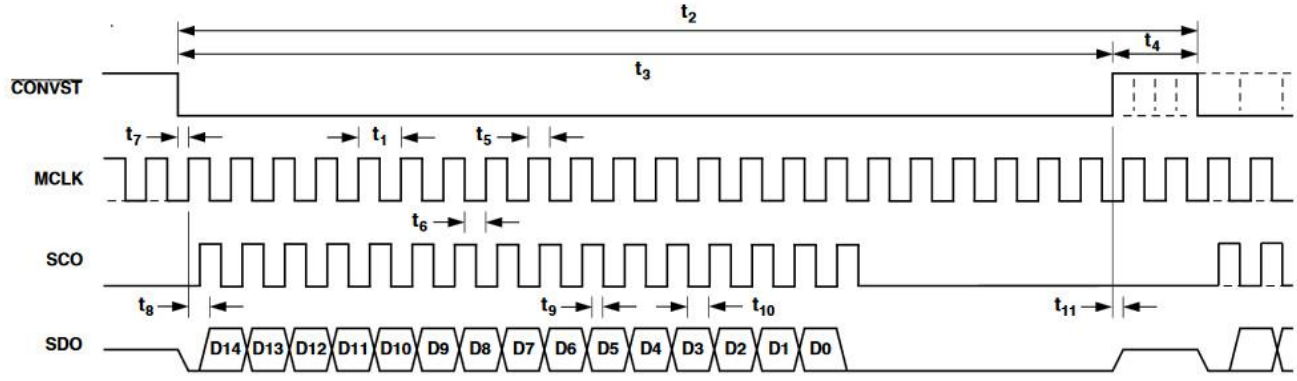
Problem 2. [4 points. This problem is another example you might face as an engineer or in your final project. *In many cases, critical information is in the timing diagram.]* Analog to digital converters (ADCs) are used to provide data input to digital systems for processing. The analog signal is sampled at fixed intervals or on command and converted to binary data with resolution ranging from 8 to 24 plus bits. ADCs are available with parallel or serial digital outputs. The advantage of serial output is fewer wires and interconnects but requires the added complexity of a serial to parallel conversion on the digital side. This is something to consider at project time should your project require an ADC: wires vs Verilog! One performance metric for ADCs is samples per second. (For the ADC, a sample is when all 14 bits of the value are available.) Parallel output ADCs are faster - i.e. more samples per second. The following is a simplified diagram of each type of ADC.



An example of a serial ADC is the Analog Devices AD7485, a 14 bit AD converter with serial output. The AD7485 uses a system clock, MCLK, provided by the user. To start the AD conversion, assert CONVST_bar (bar = line above CONVST, an active low signal) low. SCO is system clock out which you can ignore for this exercise.

SDO, serial data out, consists of 15 bits of data. The over range bit (D14) is latched out first, then 14 bits of data (MSB first) followed by a trailing zero.

AD7485



(see other side)

All timing parameters are provided in terms of t_1.

For the AD7485, $40ns < t_1 < 100{,}000ns$

$t_{2\ (min)} = t_1 \times 24$

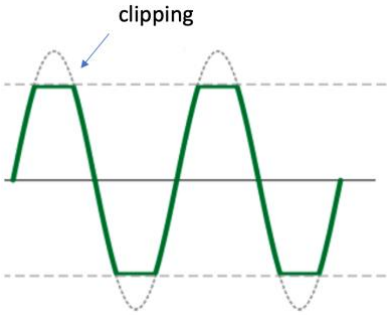
$t_{3\ (min)} = t_1 \times 22$

$t_{4\ (min)} = 10ns$

All other timing parameters can be ignored for this problem.

(a) [2 points]What is the maximum number of samples per second for this device assuming the system clock is at maximum frequency? Since this will be used for marketing, show the answer with 2 decimal places with rounding:

(b) [2 points: 0 or 2 only] Because of uncertainty of the incoming data when the analog input is over range (d[14] high), you want to set the data bits to the highest value when this occurs. For analog voltages this is referred as clipping as shown in the waveform.



Write the Verilog for this module. Ignore the clipping for negative voltages. We will address this when we discuss signed numbers. [Verilog must be syntactically correct for full credit.]

```
module range_check(input [14:0] data_in,          // result from ADC
                   output logic [13:0] data_out,
                   output out_of_range);

// your Verilog

endmodule
```

[Analog Devices was founded by Ray Stata, the major contributor to the Stata Center. Analog Devices provides free samples of their products for use in 6.111 final projects.]