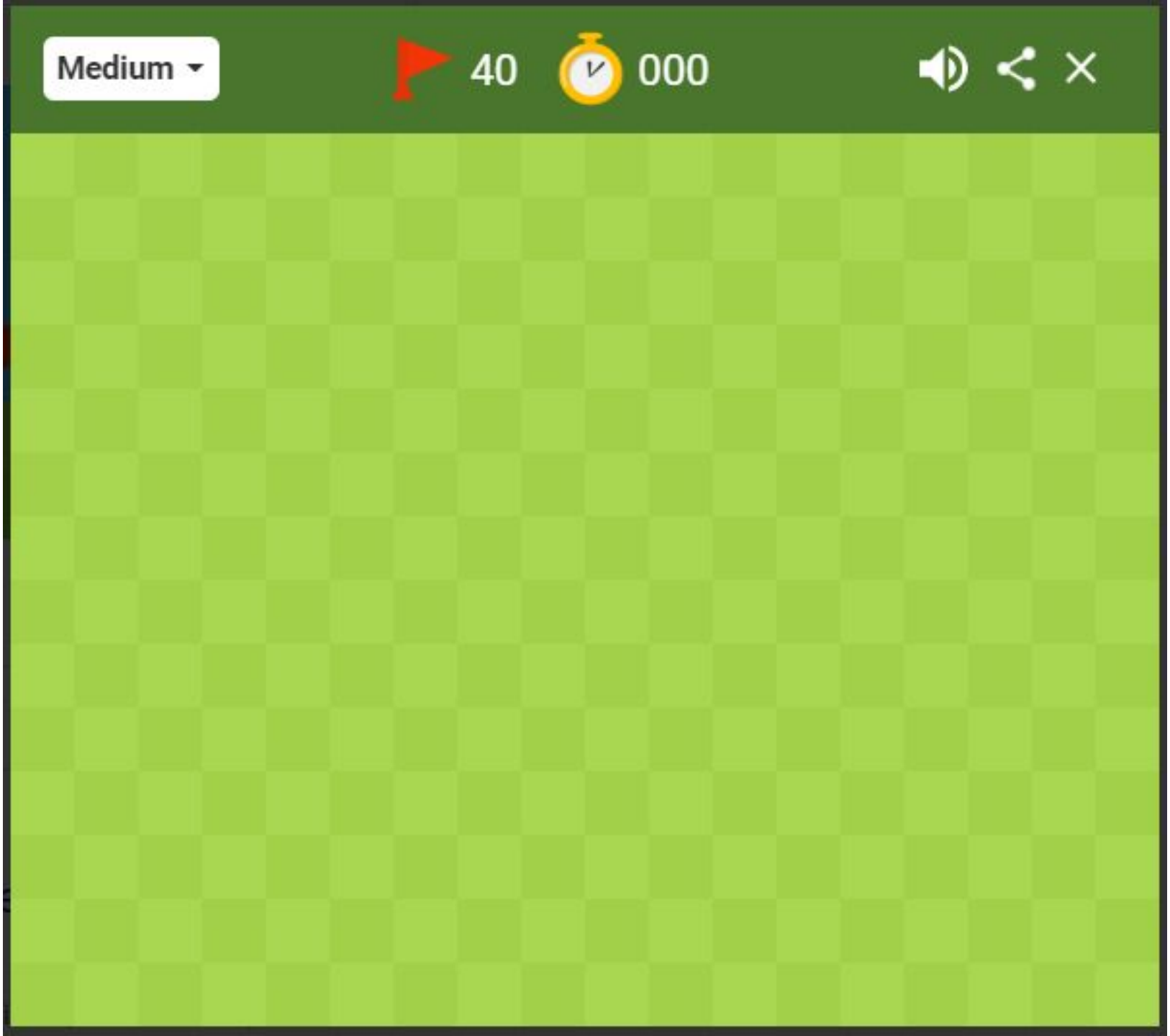
Minesweeper

Rod Bayliss III and Brandon John

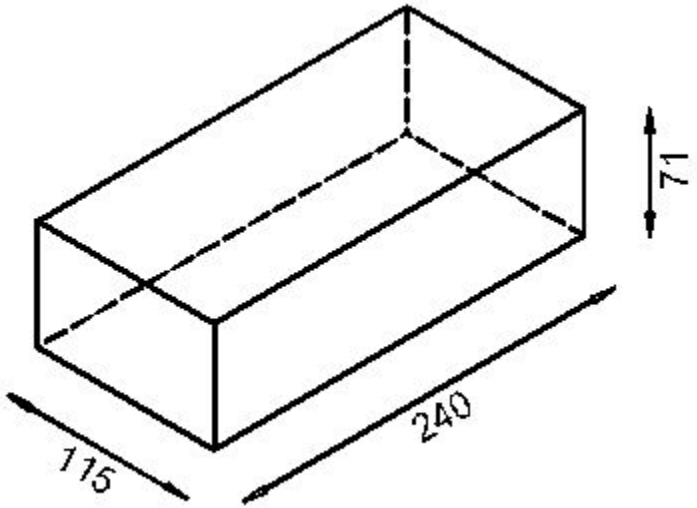

Medium
40
000

Medium
40
005
1 1
1 1 2
1 1 1 2 4
2 1 1 2
1 1 3
1 1 1 2
1 1
2 1 1 1 2 1
2 1 2
1 2
1 1
2 2 2 1

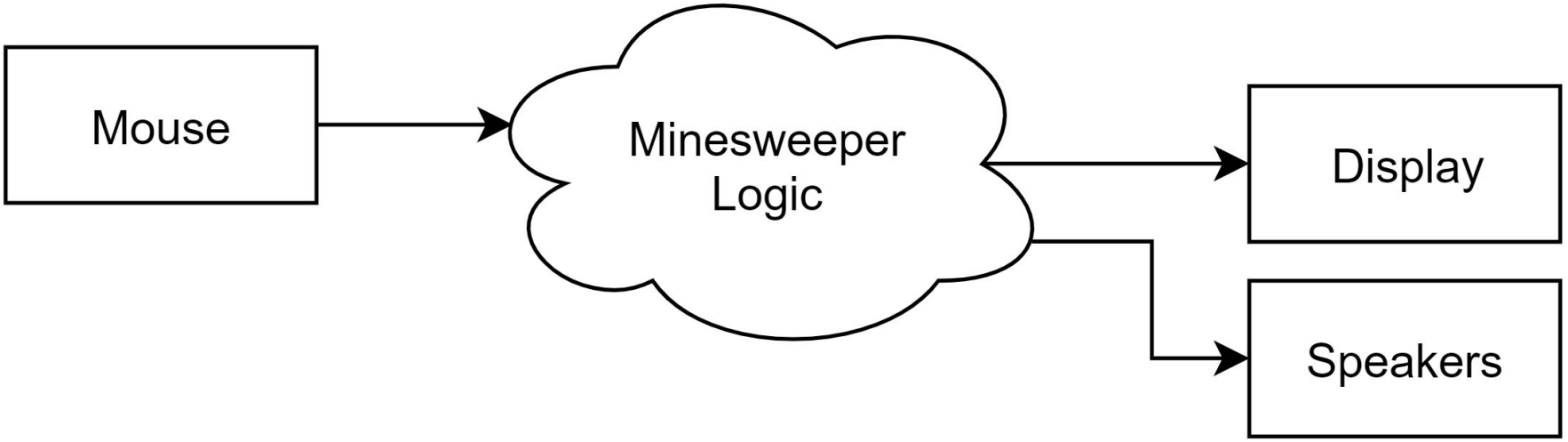
Medium
20
071

Medium
0
187

Block Diagram

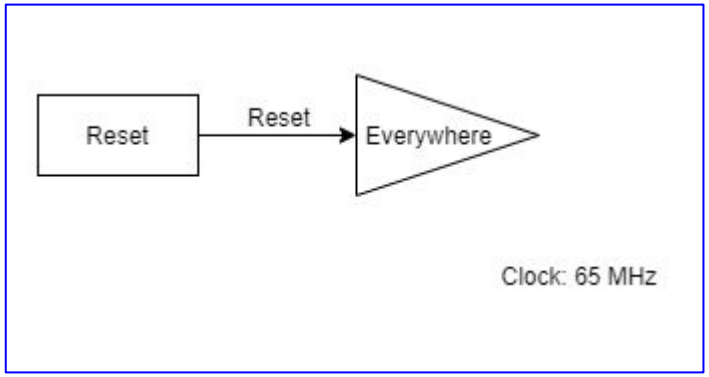


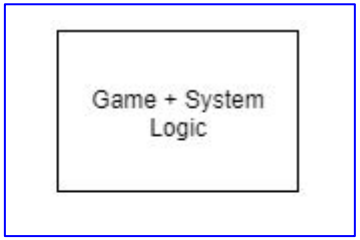
Block Diagram

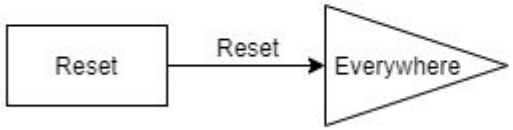


Ultra High Level

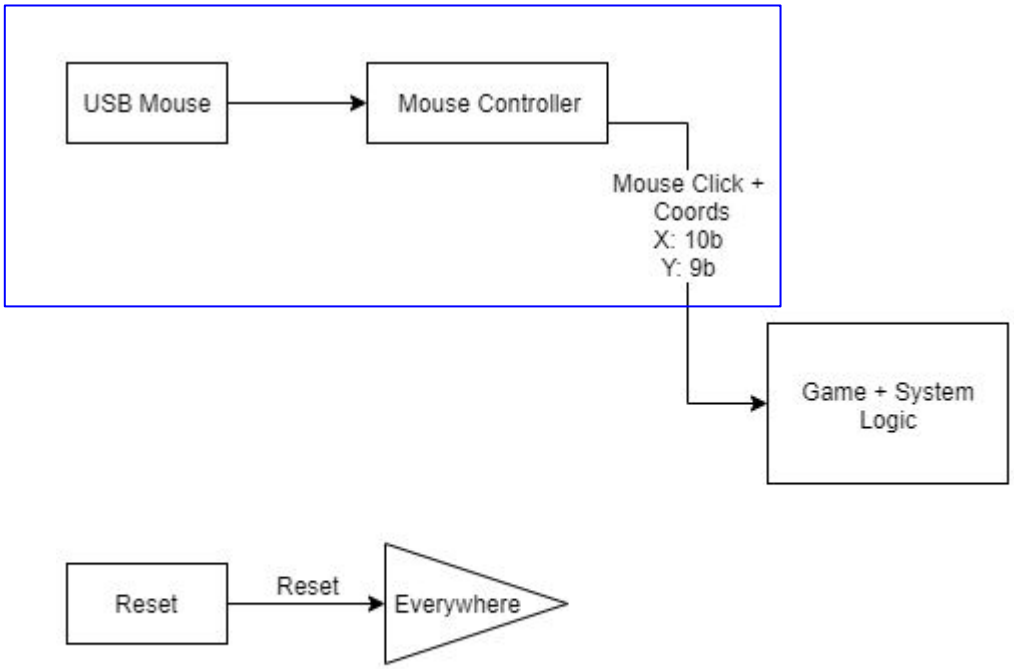
Block Diagram



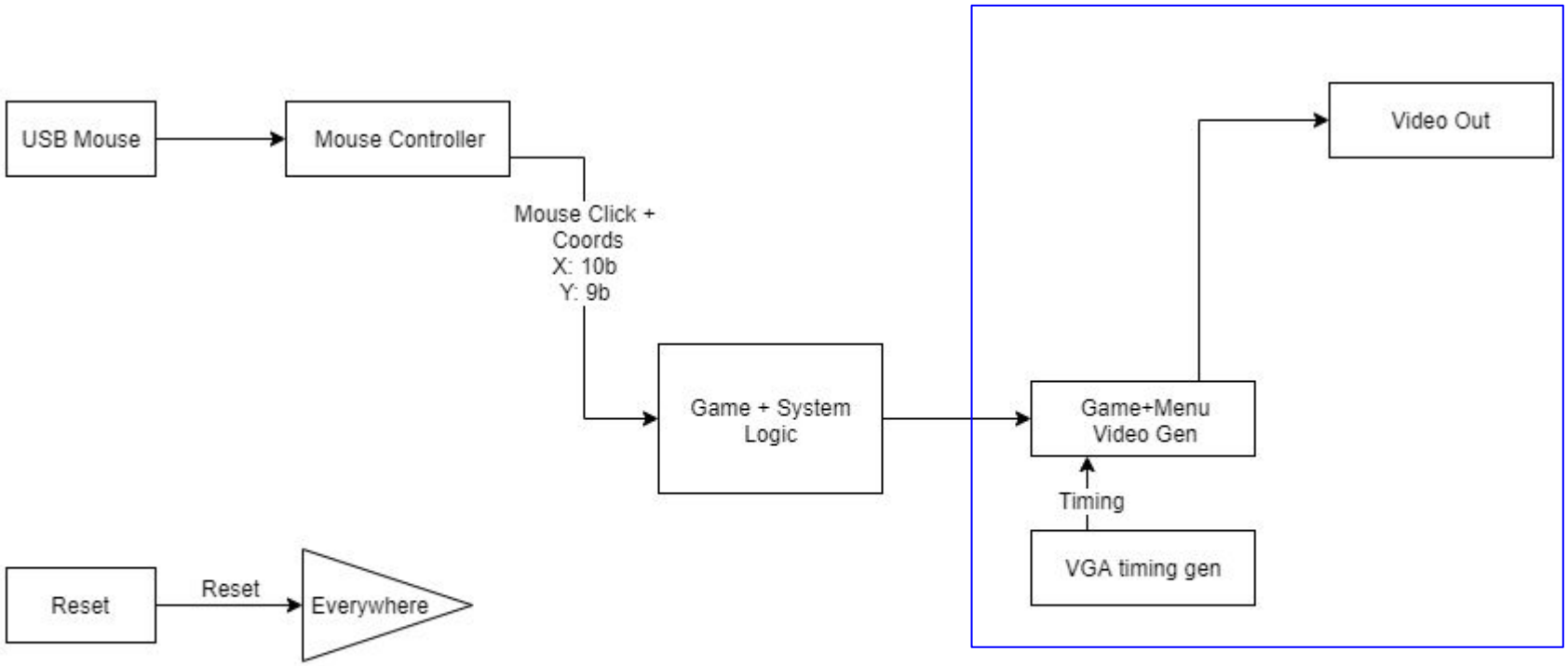




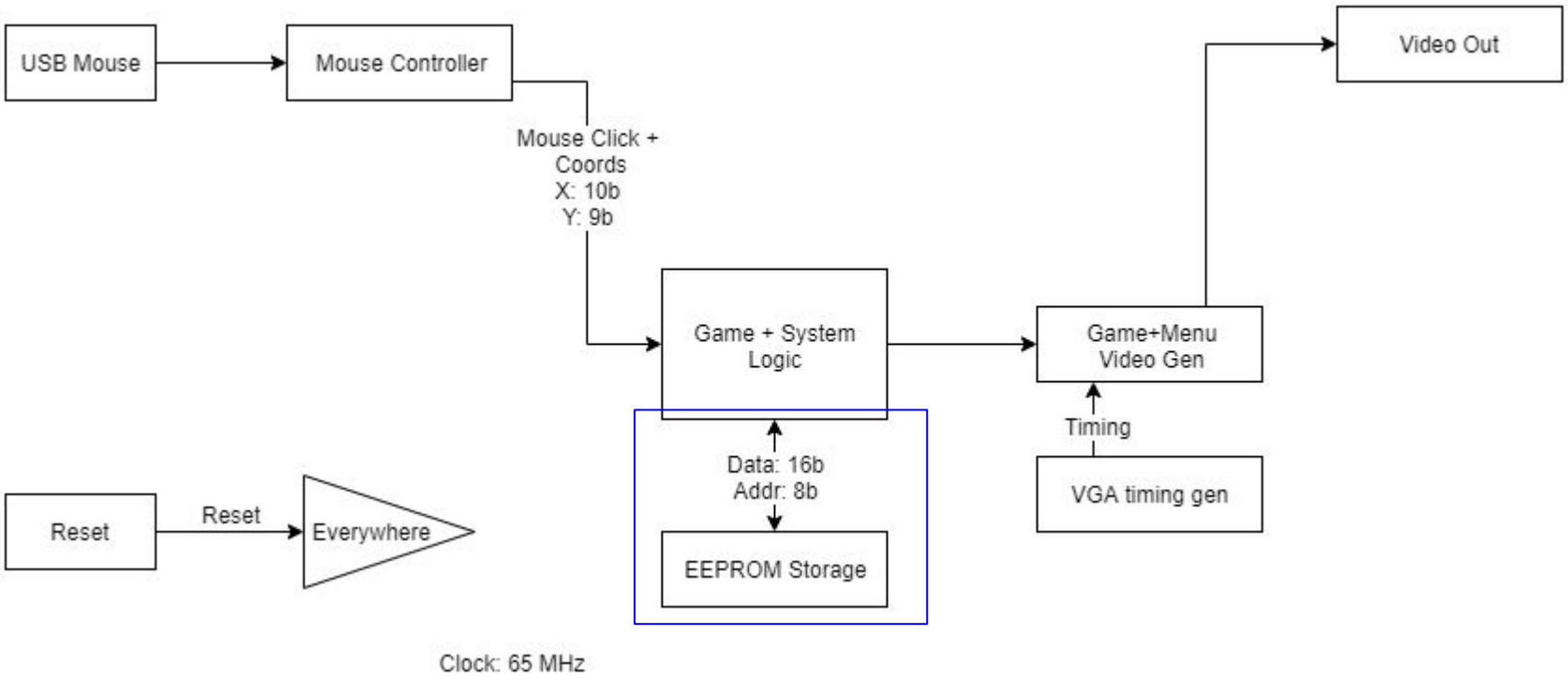
Clock: 65 MHz

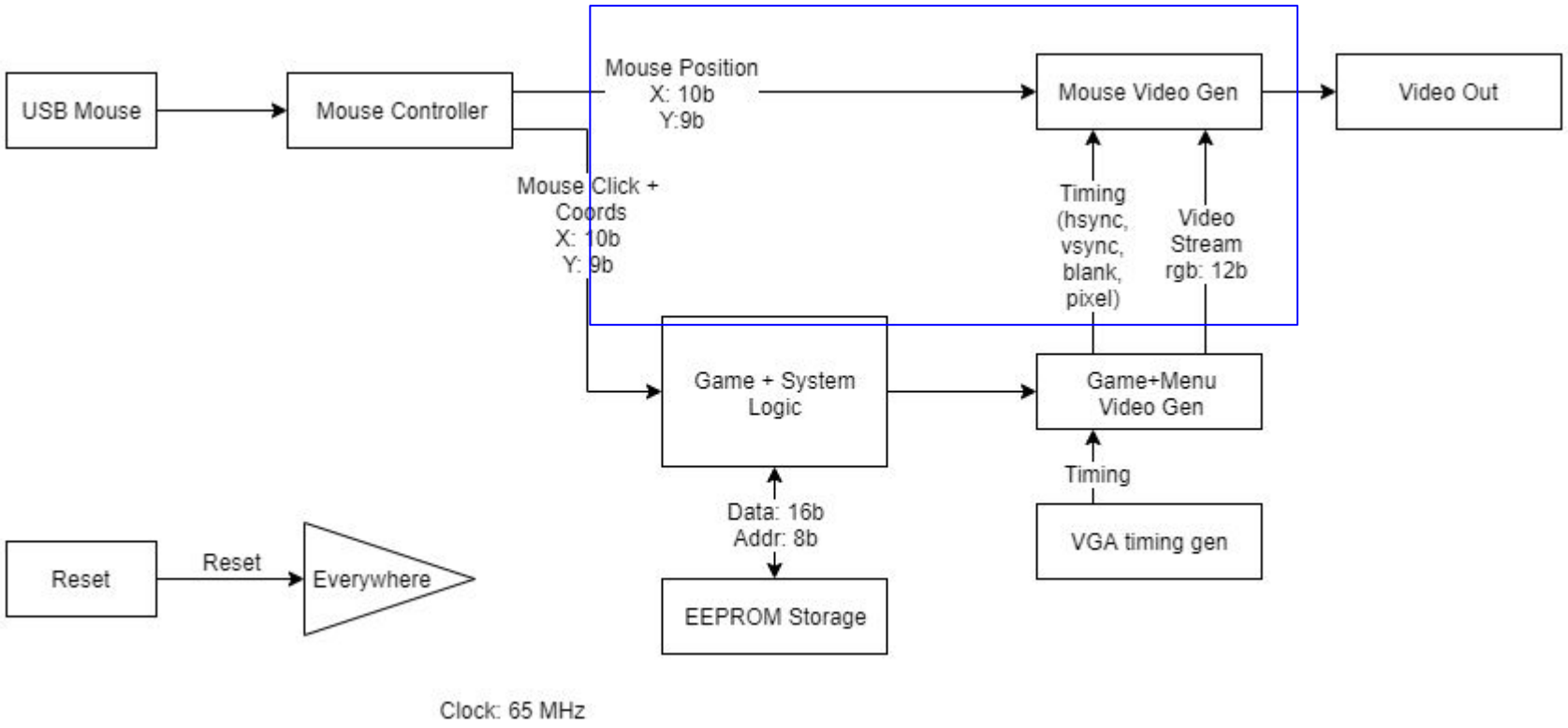

USB Mouse
Mouse Controller
Mouse Click +
Coords
X: 10b
Y: 9b
Game + System
Logic
Reset
Reset
Everywhere

Clock: 65 MHz

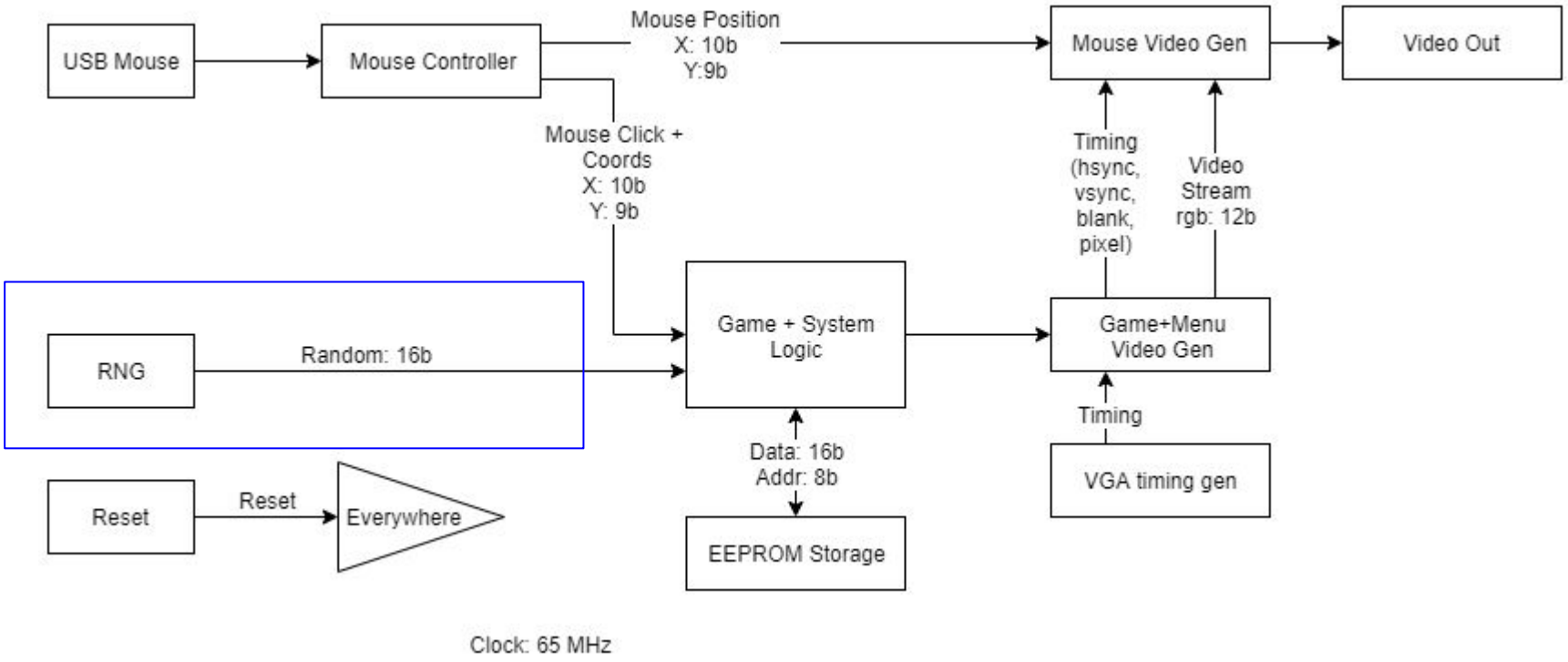

USB Mouse
Mouse Controller
Mouse Click +
Coords
X: 10b
Y: 9b
Game + System
Logic
Video Out
Game+Menu
Video Gen
Timing
VGA timing gen
Reset
Reset
Everywhere

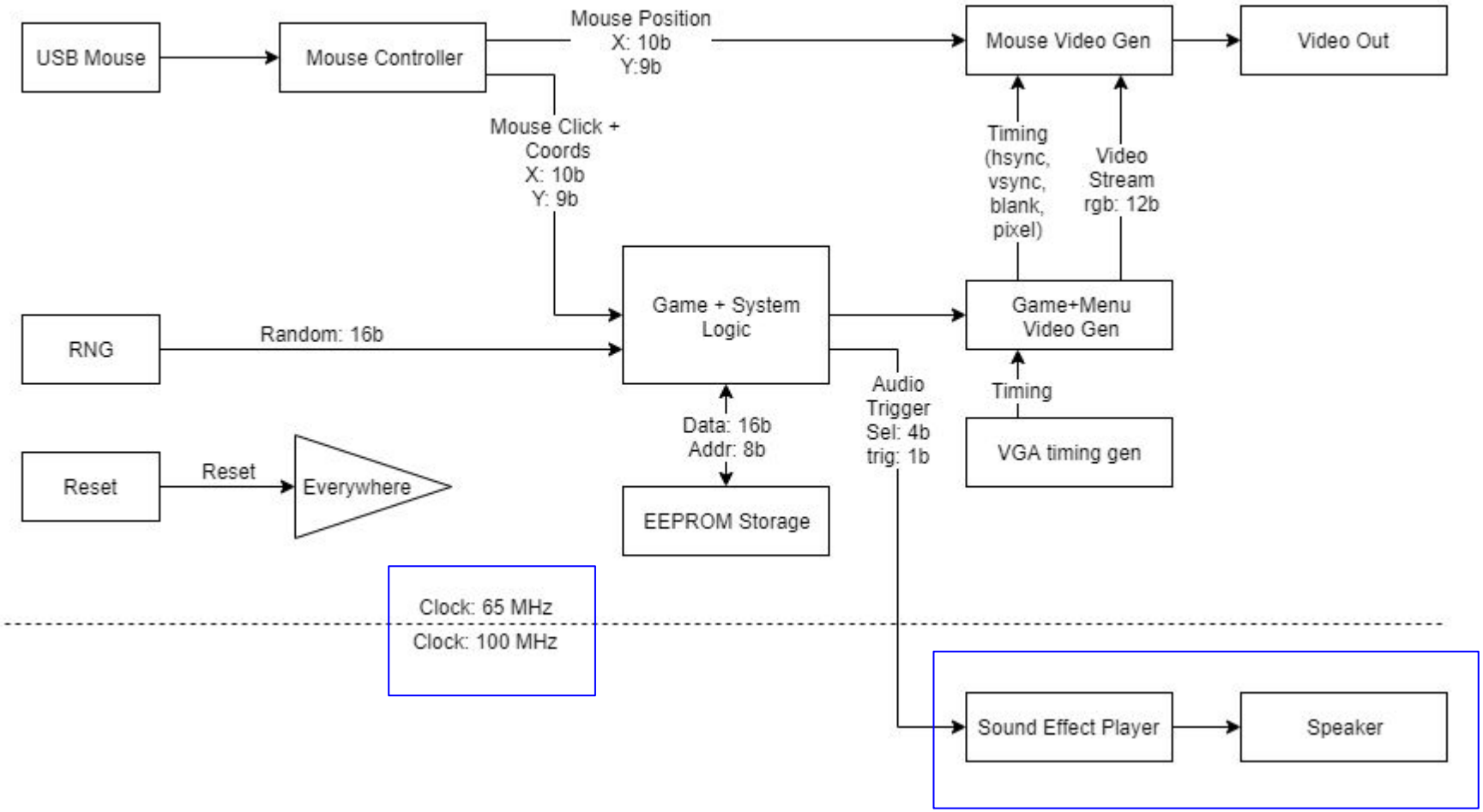
Clock: 65 MHz

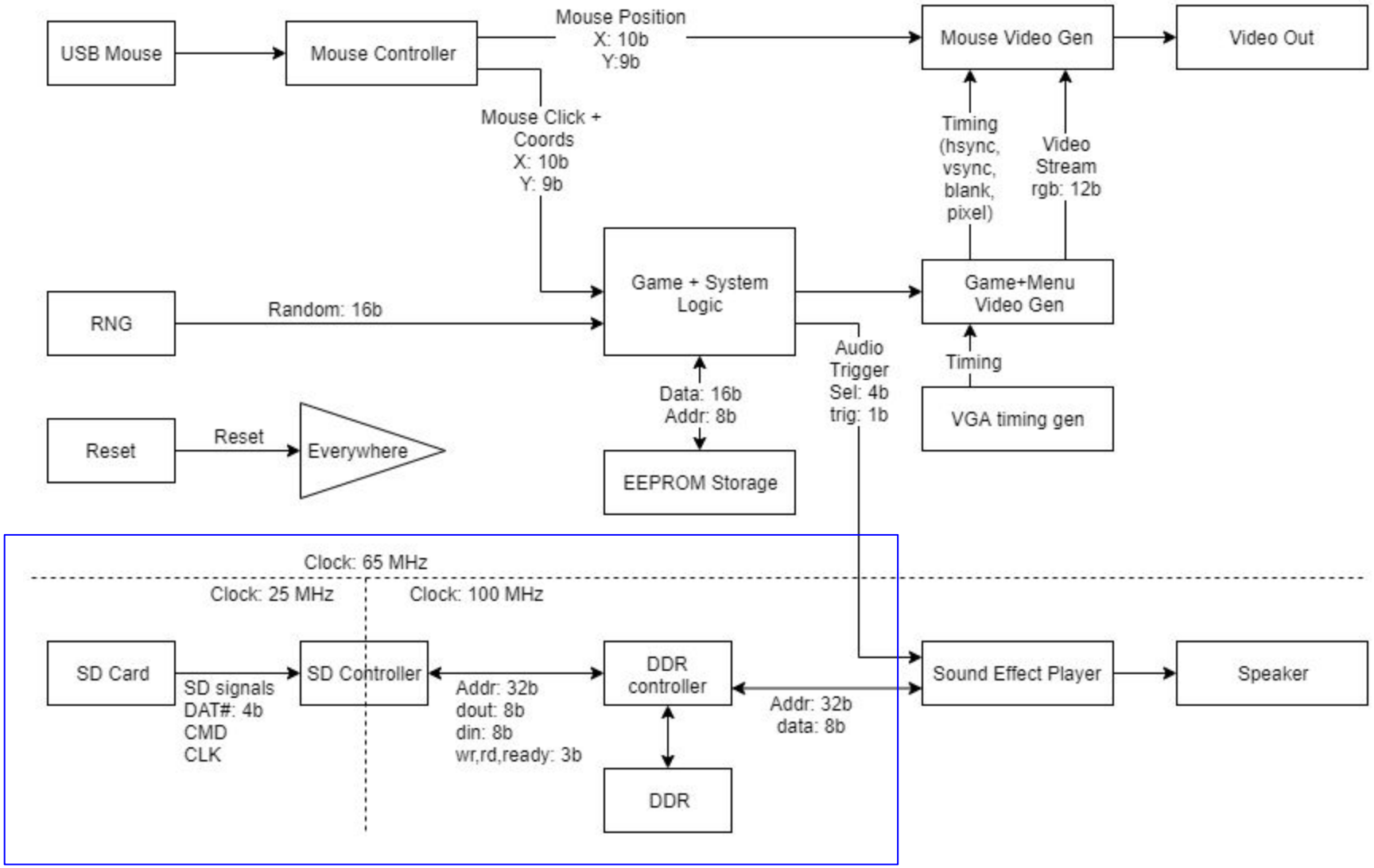

USB Mouse
Mouse Controller
Mouse Click +
Coords
X: 10b
Y: 9b
Video Out
Game + System
Logic
Game+Menu
Video Gen
Timing
VGA timing gen
Data: 16b
Addr: 8b
EEPROM Storage
Reset
Reset
Everywhere
Clock: 65 MHz


USB Mouse
Mouse Controller
Mouse Position
X: 10b
Y:9b
Mouse Video Gen
Video Out
Mouse Click +
Coords
X: 10b
Y: 9b
Timing
(hsync,
vsync,
blank,
pixel)
Video
Stream
rgb: 12b
Game + System
Logic
Game+Menu
Video Gen
Timing
Data: 16b
Addr: 8b
VGA timing gen
Reset
Reset
Everywhere
EEPROM Storage

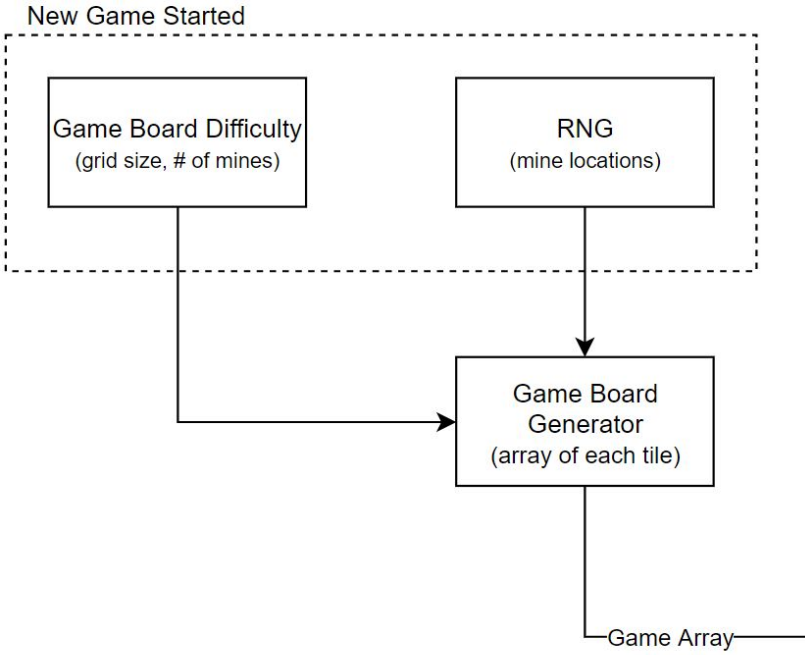
Clock: 65 MHz


USB Mouse
Mouse Controller
Mouse Position
X: 10b
Y:9b
Mouse Video Gen
Video Out
Mouse Click +
Coords
X: 10b
Y: 9b
Timing
(hsync,
vsync,
blank,
pixel)
Video
Stream
rgb: 12b
RNG
Random: 16b
Game + System
Logic
Game+Menu
Video Gen
Timing
Data: 16b
Addr: 8b
VGA timing gen
Reset
Reset
Everywhere
EEPROM Storage
Clock: 65 MHz

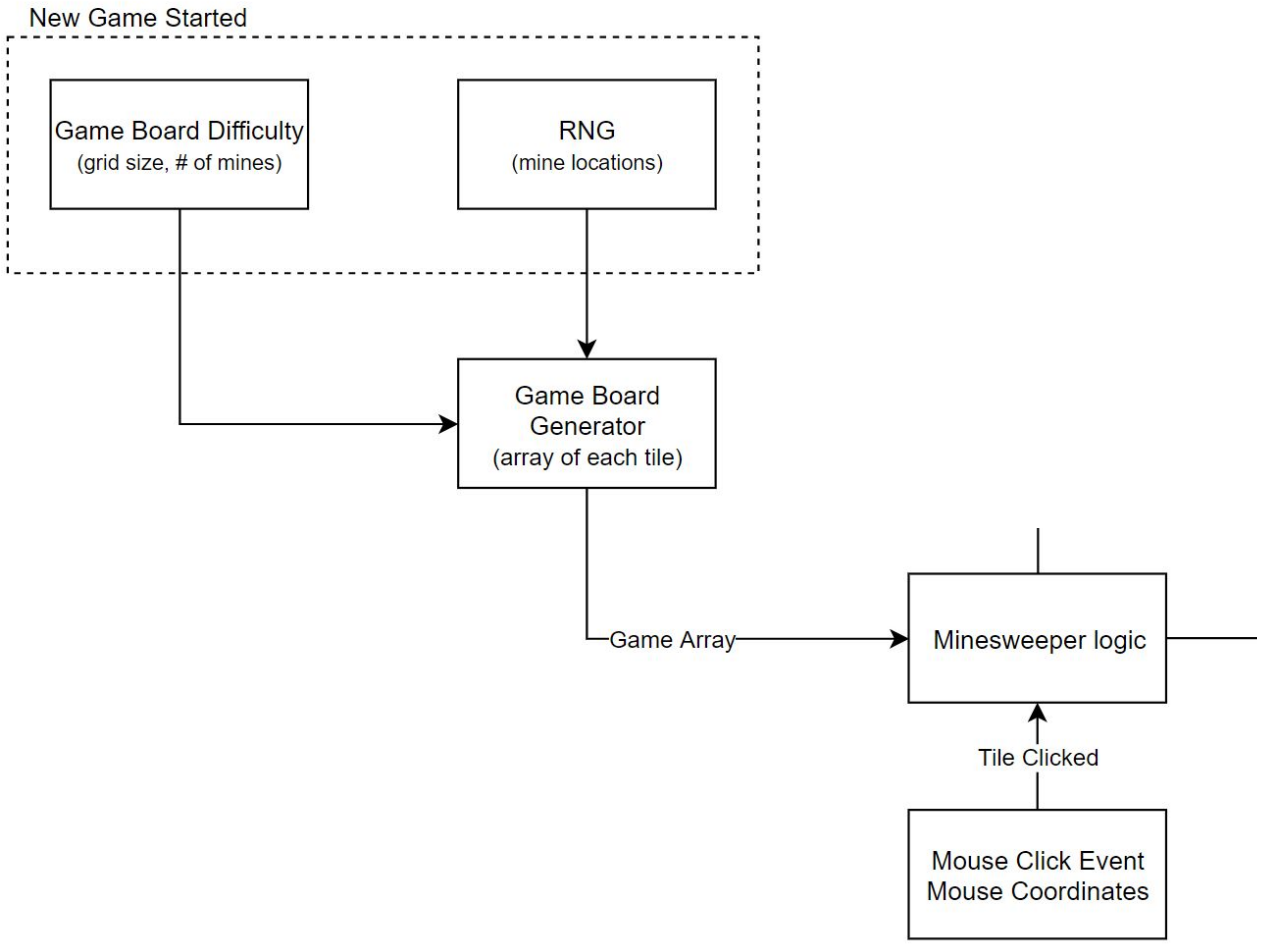

USB Mouse
Mouse Controller
Mouse Position
X: 10b
Y:9b
Mouse Video Gen
Video Out
Mouse Click +
Coords
X: 10b
Y: 9b
Timing
(hsync,
vsync,
blank,
pixel)
Video
Stream
rgb: 12b
RNG
Random: 16b
Game + System
Logic
Game+Menu
Video Gen
Audio
Trigger
Sel: 4b
trig: 1b
Timing
VGA timing gen
Data: 16b
Addr: 8b
Reset
Reset
Everywhere
EEPROM Storage
Clock: 65 MHz
Clock: 100 MHz
Sound Effect Player
Speaker


USB Mouse
Mouse Controller
Mouse Position
X: 10b
Y:9b
Mouse Video Gen
Video Out
Mouse Click +
Coords
X: 10b
Y: 9b
Timing
(hsync,
vsync,
blank,
pixel)
Video
Stream
rgb: 12b
Game + System
Logic
Game+Menu
Video Gen
RNG
Random: 16b
Audio
Trigger
Sel: 4b
trig: 1b
Timing
Data: 16b
Addr: 8b
VGA timing gen
Reset
Reset
Everywhere
EEPROM Storage
Clock: 65 MHz
Clock: 25 MHz
Clock: 100 MHz
SD Card
SD signals
DAT#: 4b
CMD
CLK
SD Controller
Addr: 32b
dout: 8b
din: 8b
wr,rd,ready: 3b
DDR
controller
DDR
Addr: 32b
data: 8b
Sound Effect Player
Speaker

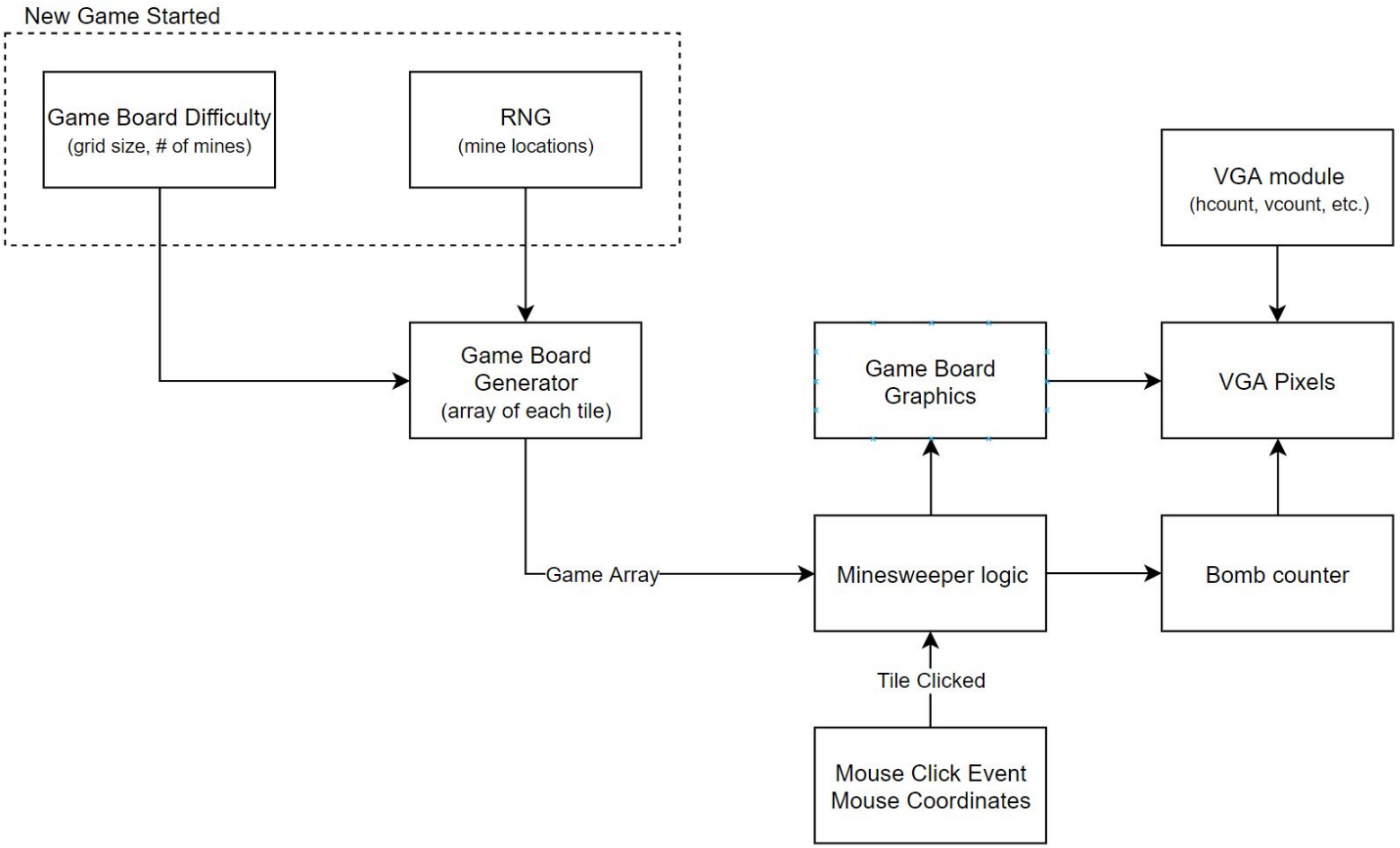
Logic Block Diagram



Logic Block Diagram



Logic Block Diagram



Timeline

11/8: Module interfaces written in verilog, high-level test benches created.

11/15: Game logic working for single difficulty. USB-HID (mouse) module working

11/22: Game logic + video gen, USB-HID, VGA fully working at single difficulty

11/27: Multiple game difficulties, SD-Card working, audio finishing up, leaderboard and end-game sequence finishing up

12/6: Project completed. Additional features potentially implemented such as multiplayer, snowflakes on screen, etc.

Questions?