Picture in Picture

6.111 Final Project

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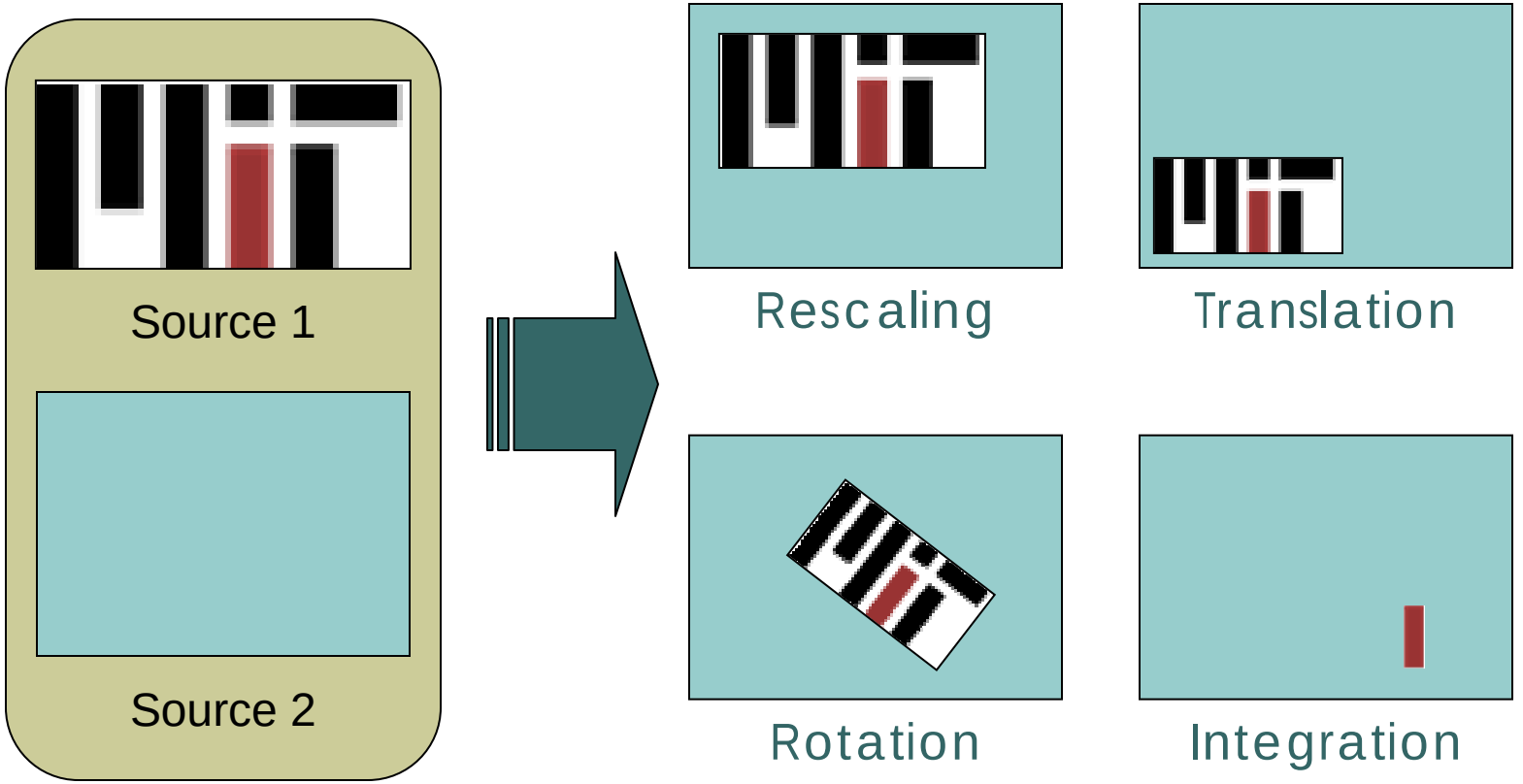
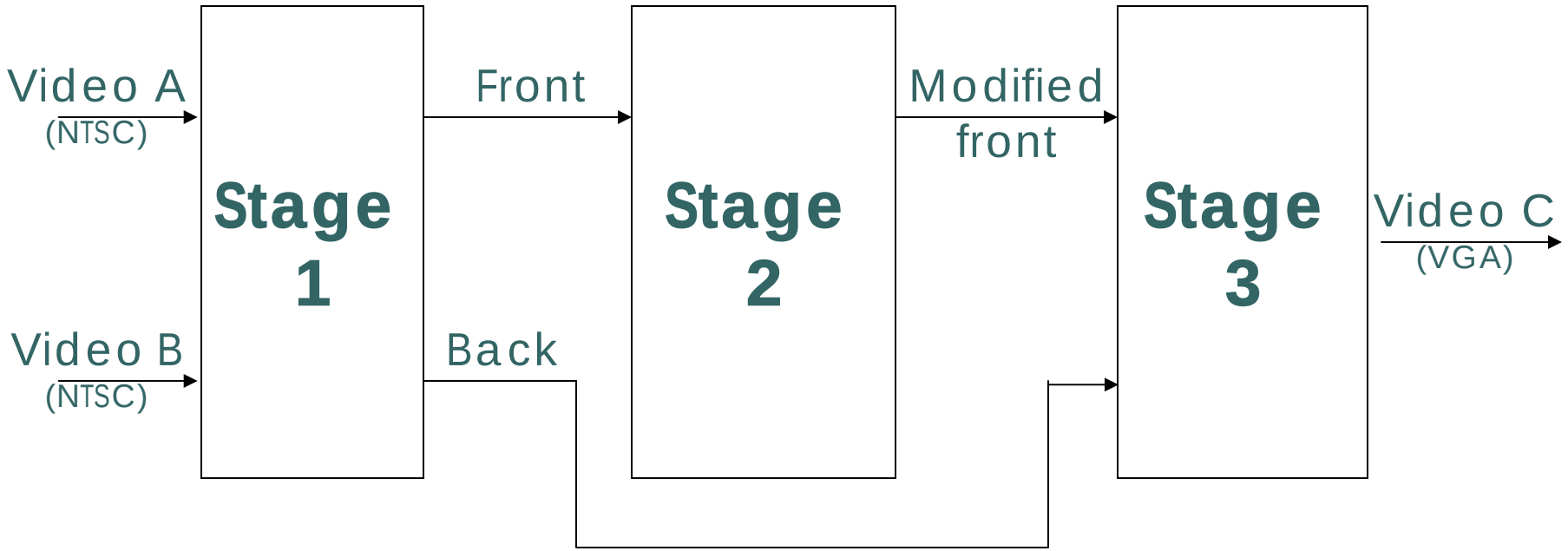
Project Overview

- Display two live video feeds on the screen at the same time.
- Perform some manipulation of one of the feeds.
- Converting from NTSC to VGA
- Using lots of RAM and needs way to manage communication

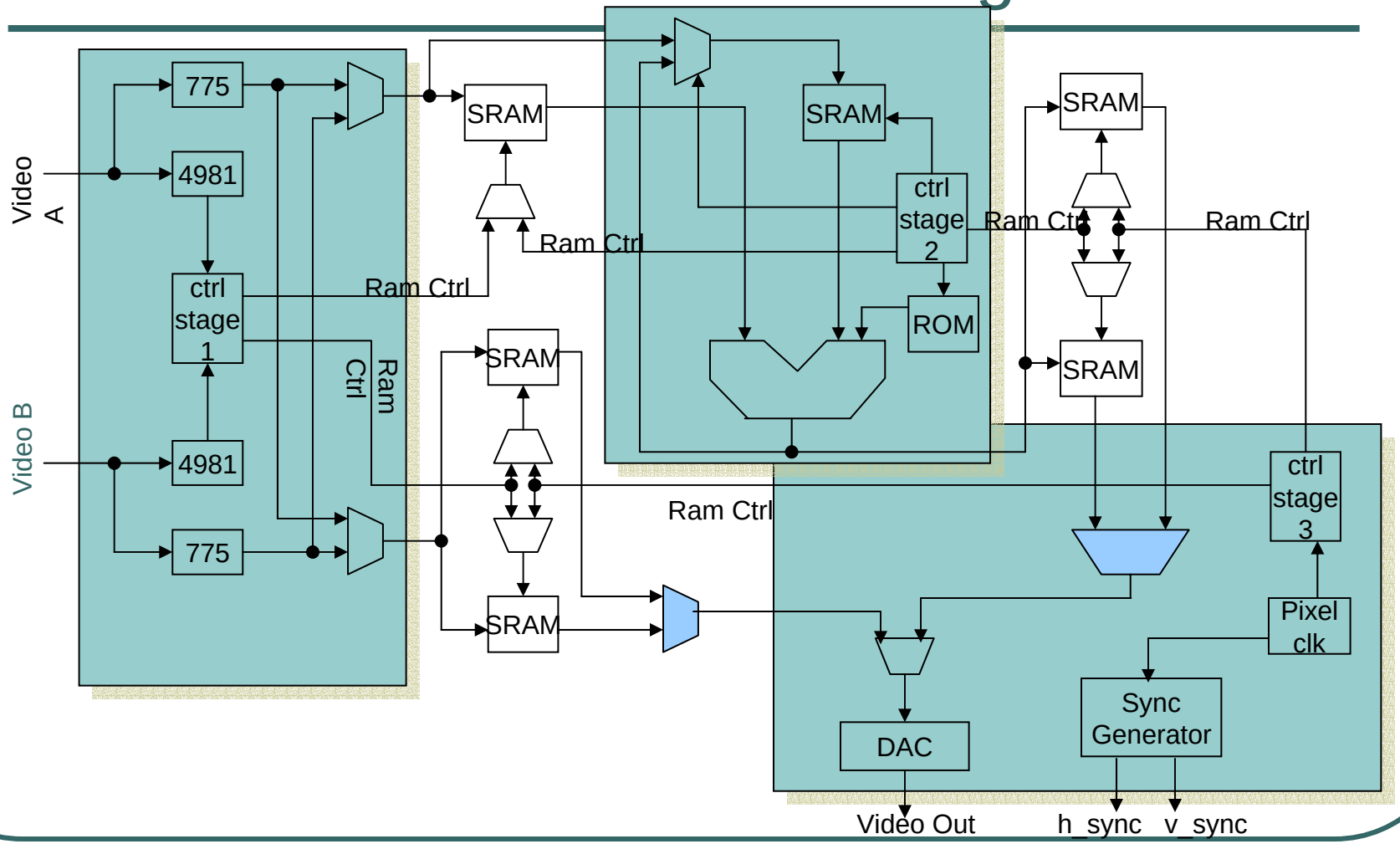
Project Overview (continued)



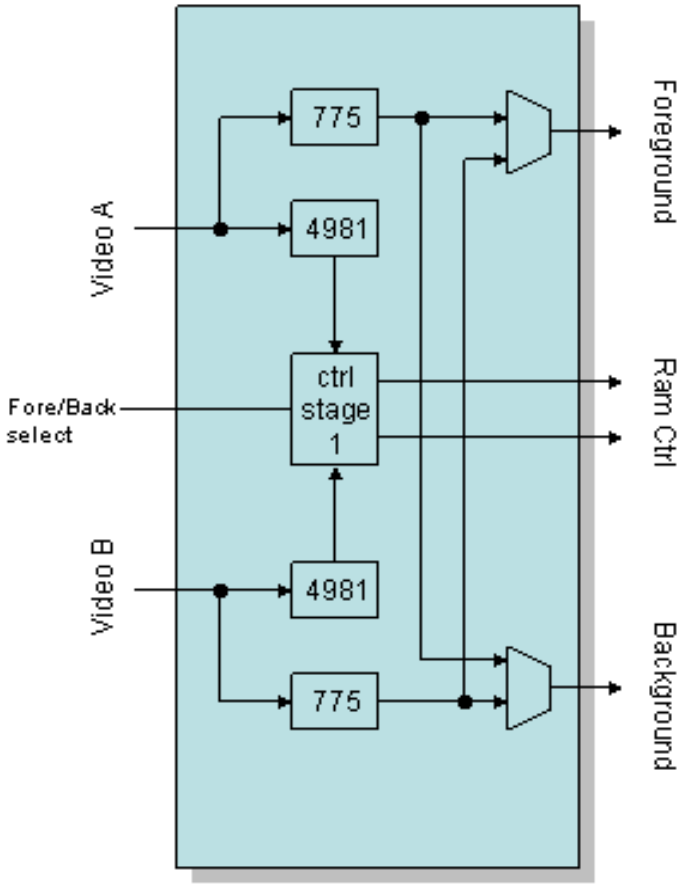
Basic Block Diagram



More detailed block diagram



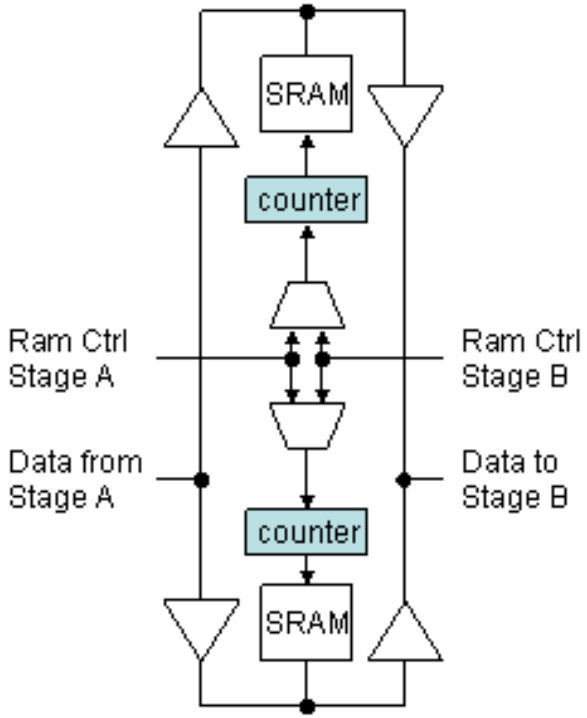
Stage 1: Digitizing Video



- User controls choice of front and back signals
- Frame size is 320x240 = 6MHz
- Sync signals from GS4981 indicates sample start point

Stage 1: RAM management

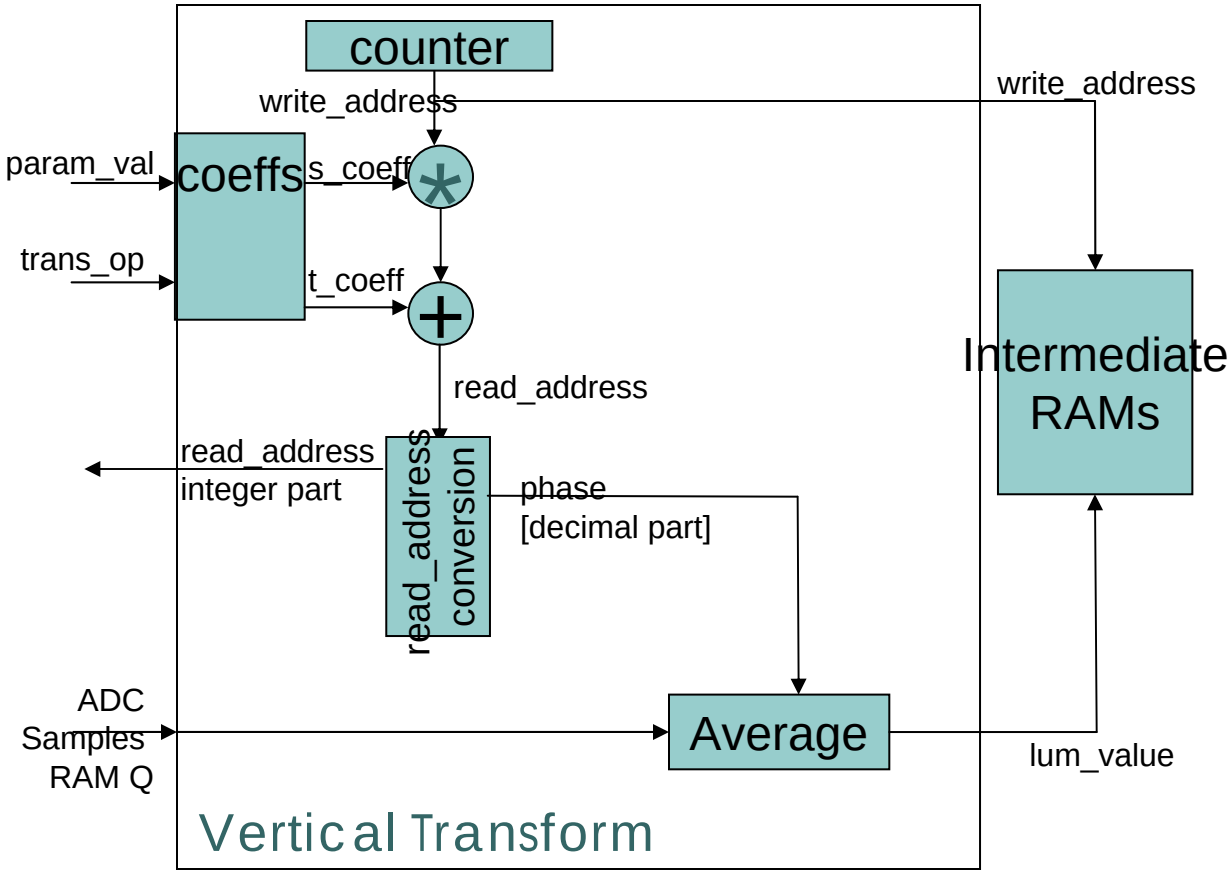
- Passing frames (RAM) between stages
- Parallel processing leads to 28 RAMs
- Limited output pins on FPGA
- Need to manage handoffs transparent to the other stages



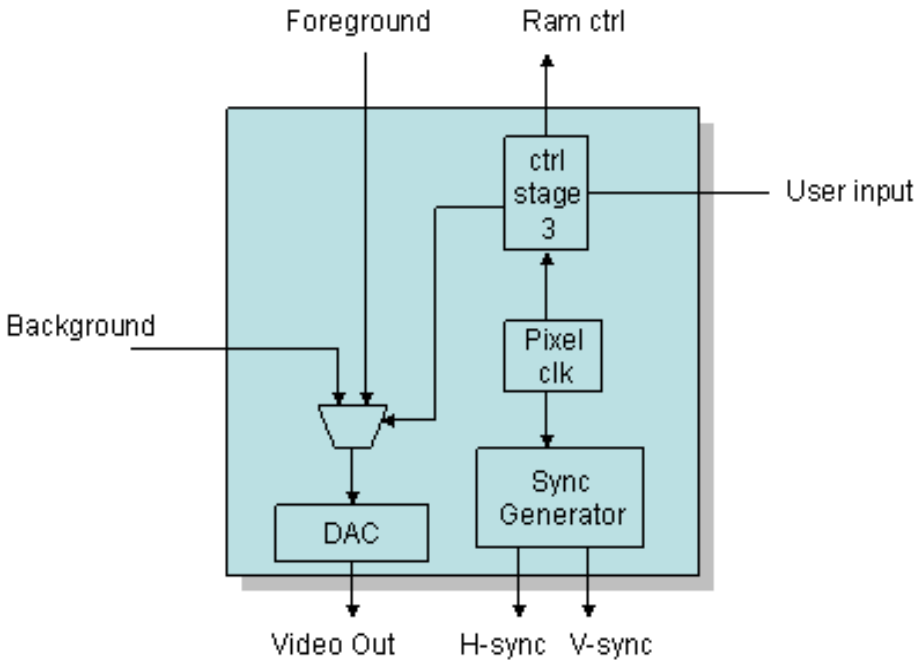
Stage 2: Digital Processing

- Read pixels from sample storage RAM
- CG Transforms can be split up into two 1-D problems
  - Perform a Vertical Transform on the frame columns (scaling, translation offset)
  - Store result in an intermediate RAM
  - Perform a Horizontal Transform on the frame rows
  - Store result in an final output RAM

Stage 2: Digital Processing



Stage 3: Output to VGA



- Combine two video feeds into one video stream
- Search foreground for blanking signal
- Generate sync signals for VGA monitor

Stage 3: Handling User Input

- User can control foreground image by pushing buttons and toggling switches
  - Scale
  - Angle
  - Movement
- Appropriate response for holding of button