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# Line Field Decoder

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## Summary

The video standard ITU-R.656 uses the sample definition defined in ITU-R BT.601 and SMPTE 125M. The standards describe how video field and line timing are embedded in the bit-parallel data through the use of reserved data words known as timing reference signals (TRS)[1] [2]. The MicroBlaze™ and Multimedia development board uses and decodes this information to regain the timing of the incoming video stream. This timing is then passed to other algorithms inside the device.

The reference design available with this application note decodes TRS information and supplies timing control signals to the rest of the video algorithms. The design is a modification of design files associated with **XAPP248: Digital Video Test Pattern Generators**.


## Component Video Voltages

### The Associated Digital Video Data Values in Each Video Line

The MicroBlaze and Multimedia development board uses an Analog Device decoder, ADV7185, to sample (up to four times over-sampling) incoming analog video and convert it to digital values. Figure 1 shows how the voltages relate to the digital values sent to the Virtex™-II or Spartan™-II device. Notice the 8-bit data values of `FFh` (decimal 256) and `00h` (decimal 0) in Figure 1 do not occur in the normal stream of video. Therefore, `FFh` or `00h` can be inserted in non-picture parts of a line to mark timing information. These inserted symbols are the timing reference signals (TRS),

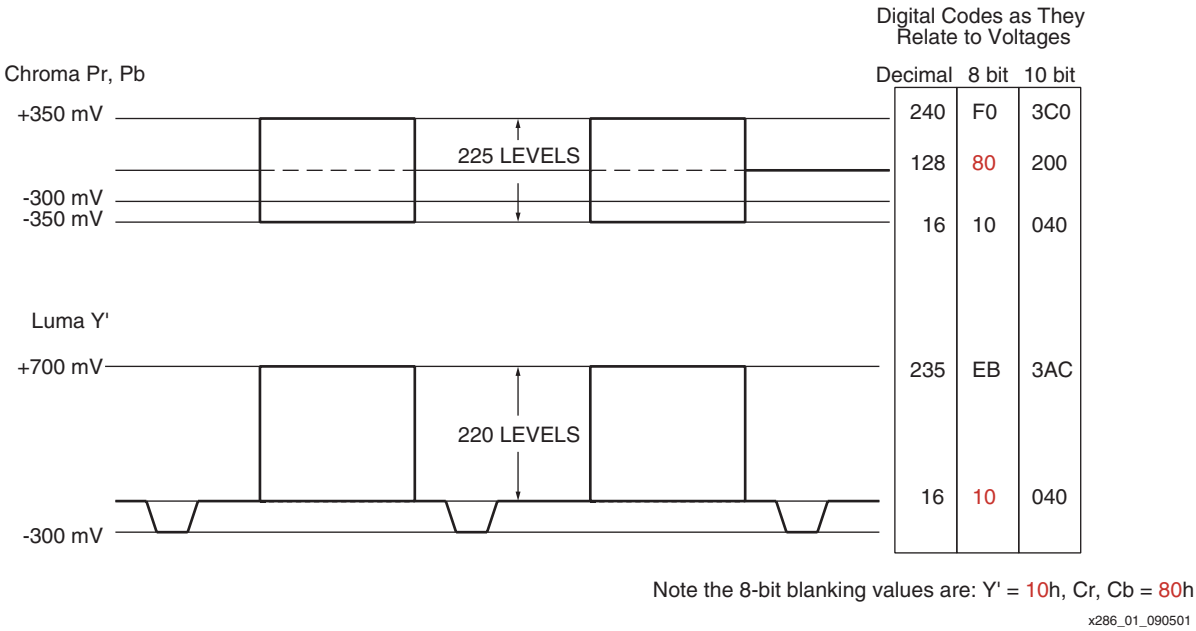


*Figure 1:* **Analog Component Video Voltage Levels and Associated Digital Values**

The MicroBlaze and Multimedia development board supports 10-bit video data coming from the decoder device. Notice in Figure 1 how this compares to 8-bit data values. The two extra bits beyond the normal 8-bit data are appended to the rightmost part of the 8-bit data and are assumed to be fractional. When the fractional parts are zero, the specifications just "leave them off".

For example, the bit pattern `10010001` would be expressed as `145d` or `91h`, whereas the pattern `1001000101` is expressed as `145.25d` or `91.4h`. In fact, the data paths on the development board and inside the Virtex-II device were designed specifically for future MPEG investigation and are 12-bits wide. The extra two data bits beyond the10-bit data are appended to the MSBs, leaving more "headroom" for calculations.

Figure 2 and Figure 3 summarize the embedded timing format described fully in the video standard ITU-R BT.656. The significant components of a single horizontal line are shown; "front porch", "horizontal sync", "back porch", and "active video". The number of samples allocated to each horizontal line for the NTSC and PAL standards are also shown.

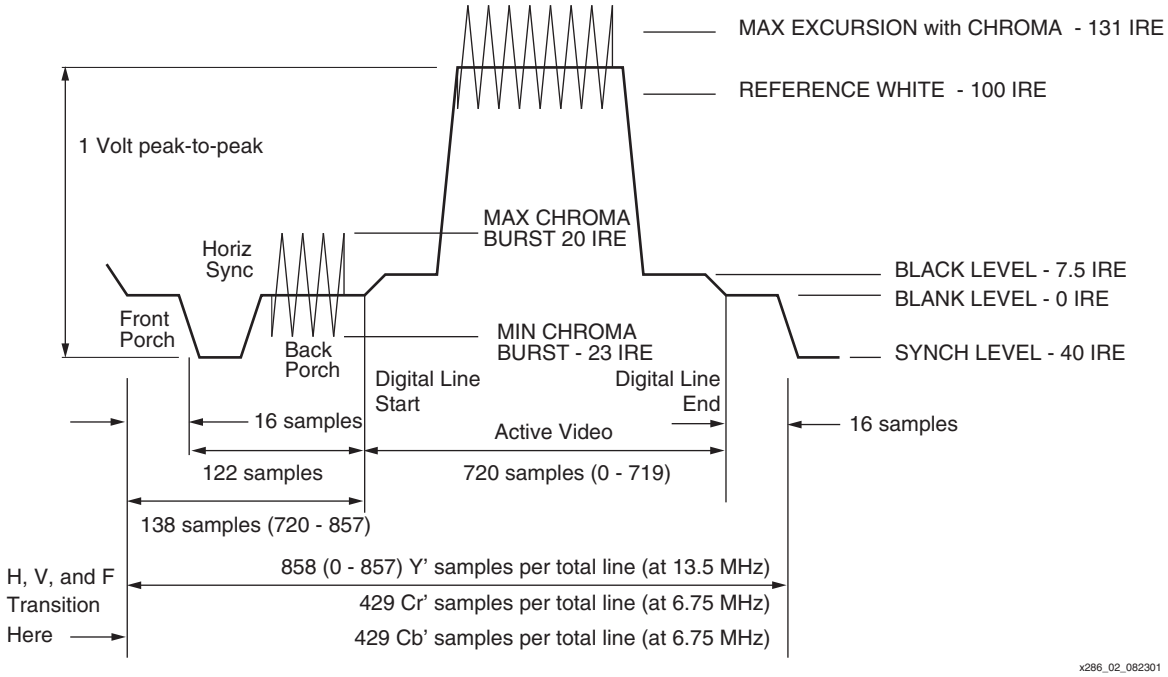


*Figure 2:* **Composite NTSC (525 Line With Set-up) Horizontal Scan Line Detail**

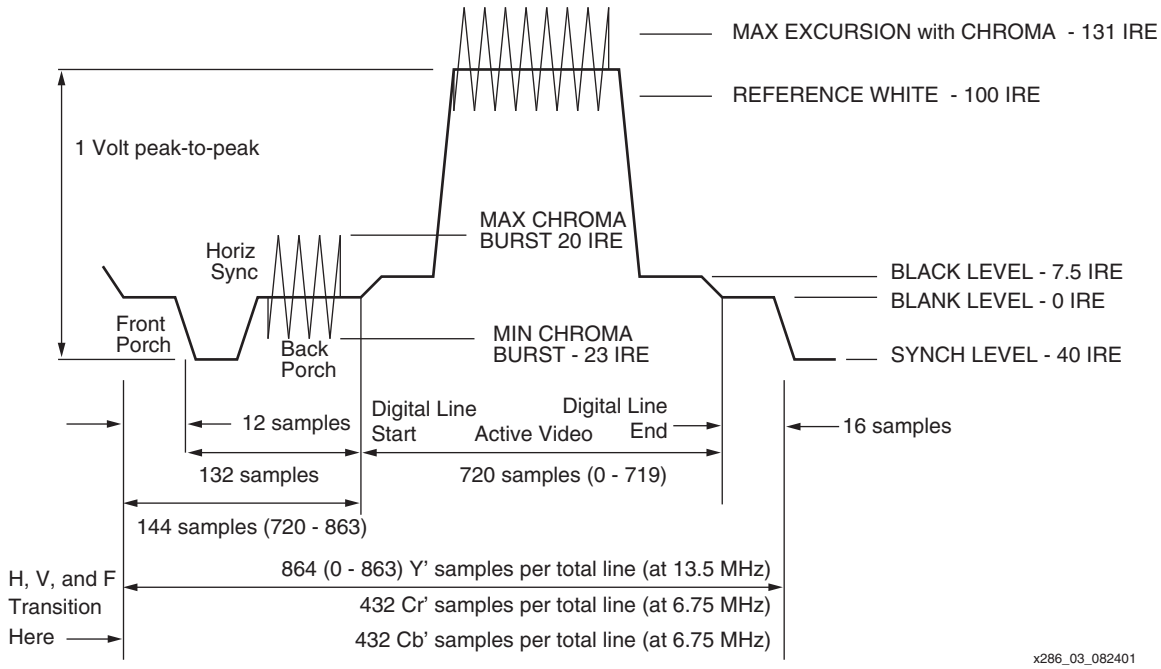


*Figure 3:* **Composite PAL (625 Line With Set-up) Horizontal Scan Line Detail**

## Video Timing Information Embedded in Each Video Line

As shown in the previous figures, the video data words are conveyed as a 27 MHz data stream, in the following order:

Cb0, Y'0, Cr0, Y'1, Cb1, Y'2, Cr1, Y'3, Cb2, Y'4, Cr2, Y'5...

All the data values are sampled on the rising edge of the 27 MHz clock. In an 8-bits-per-word implementation, the data values `FFh` and `00h` are used to form the TRS preamble. A TRS preamble consists of three words, `FFh`, followed by `00h`, followed by `00h`. In 10-bit implementations, the data values `3FFh` and `000h` are used for the TRS preamble. The TRS preamble and following XY word are decoded and combined with various counts, such as line count, to completely specify the NTSC or PAL timing to the rest of the video algorithms in a system design.

Field and frame timing is actually embedded in the data stream by the word following the TRS. This word, known as XY can be decoded for different timing events.

The terms SAV and EAV are abbreviations for "Start of Active Video" and "End of Active Video", respectively. SAV is identified with the timing reference code (`FF 00 00`) followed by the XY word where bit four of the XY word is a logic Low. EAV is identified as a logic High in bit four of the XY word. SAV signals that active video pixels will follow. EAV signals that horizontal blanking follows. Figure 4 shows this detailed horizontal pixel information for a horizontal NTSC 525 line and Figure 5 shows the same information for a PAL 625 line.

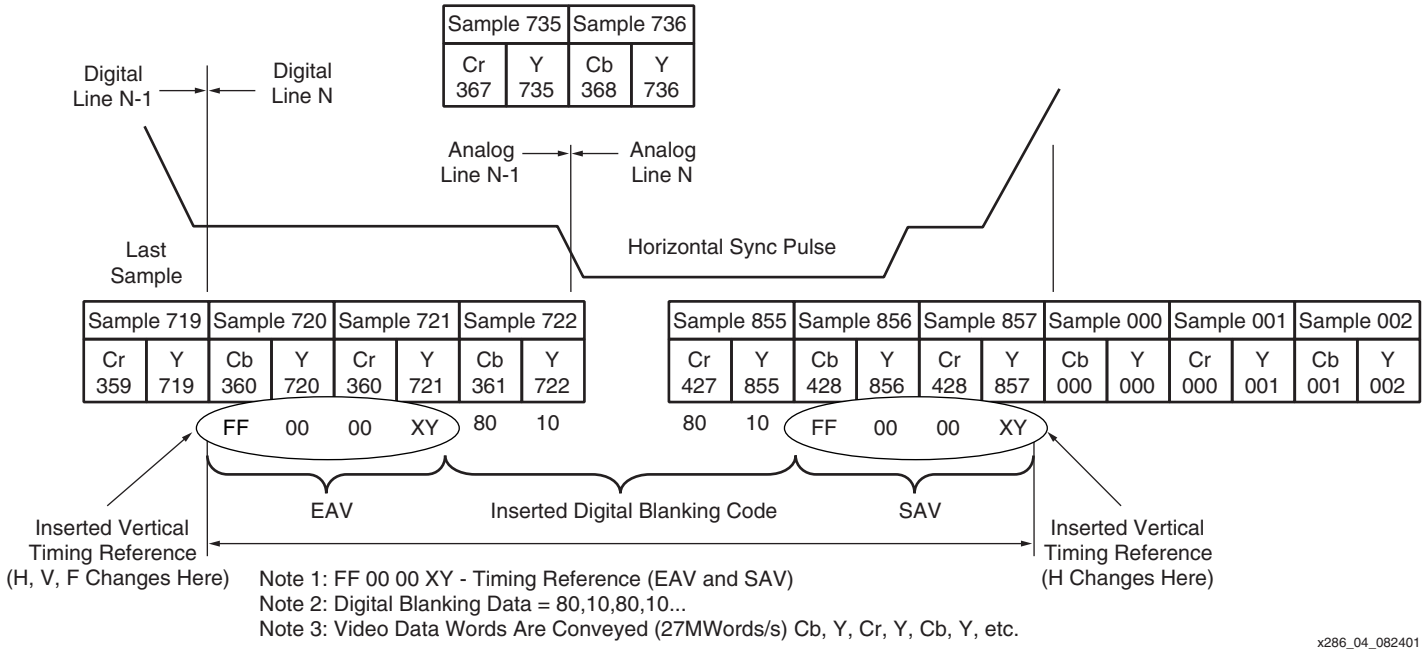


*Figure 4:* **NTSC (525 Line) Horizontal Scan Line Detail, Inserted Codes**

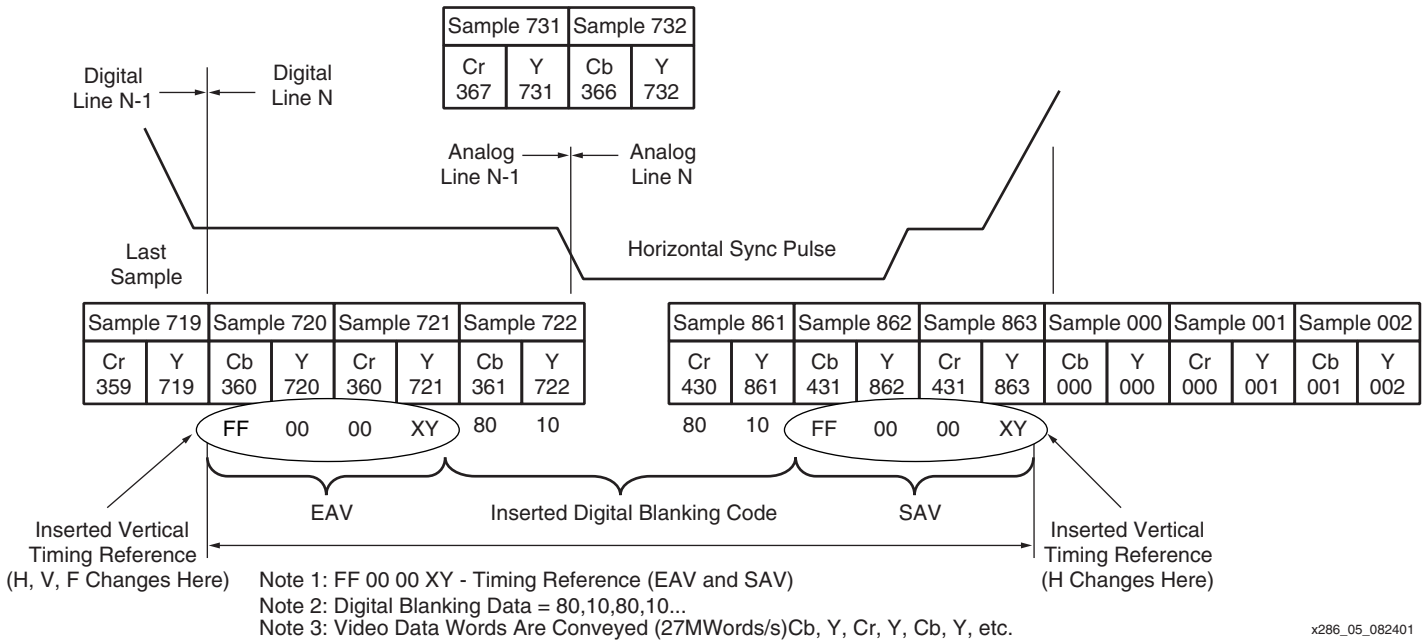


*Figure 5:* **PAL (625 Line) Horizontal Scan Line Detail, Inserted Codes**

Field number and vertical blanking are also conveyed by XY, following a field ID. The "F bit" or bit-position six and the "V bit" or bit-position five are decoded as follows:

F = 0, denotes field 1

F = 1, denotes field 2

V = 0, denotes no vertical blanking

V = 1, denotes vertical blanking

## Video Line and Field Timing

There are more pixels in the blanking period for PAL than NTSC (144 vs. 138), but the number of active pixels, in a line, are the same (720). While there are more lines in PAL (625 per frame for PAL vs. 525 for NTSC), there are less frames per second (25 for PAL vs. 30 for NTSC). In fact, the pixel frequencies are approximately equal.

As ideas and inventions are introduced, video evolves in many different ways creating enormous variations in formats. For example, the introduction of computer systems generated a desire to mix video broadcast systems and computers further complicating formats with the notion of the square pixel. When looking at a table of information about pixels per line, lines per frame, and frames per second, a basic understanding of the specific format is necessary.

Figure 6 and Figure 7 show the detail associated with NTSC and PAL vertical information conveyed by the standard.

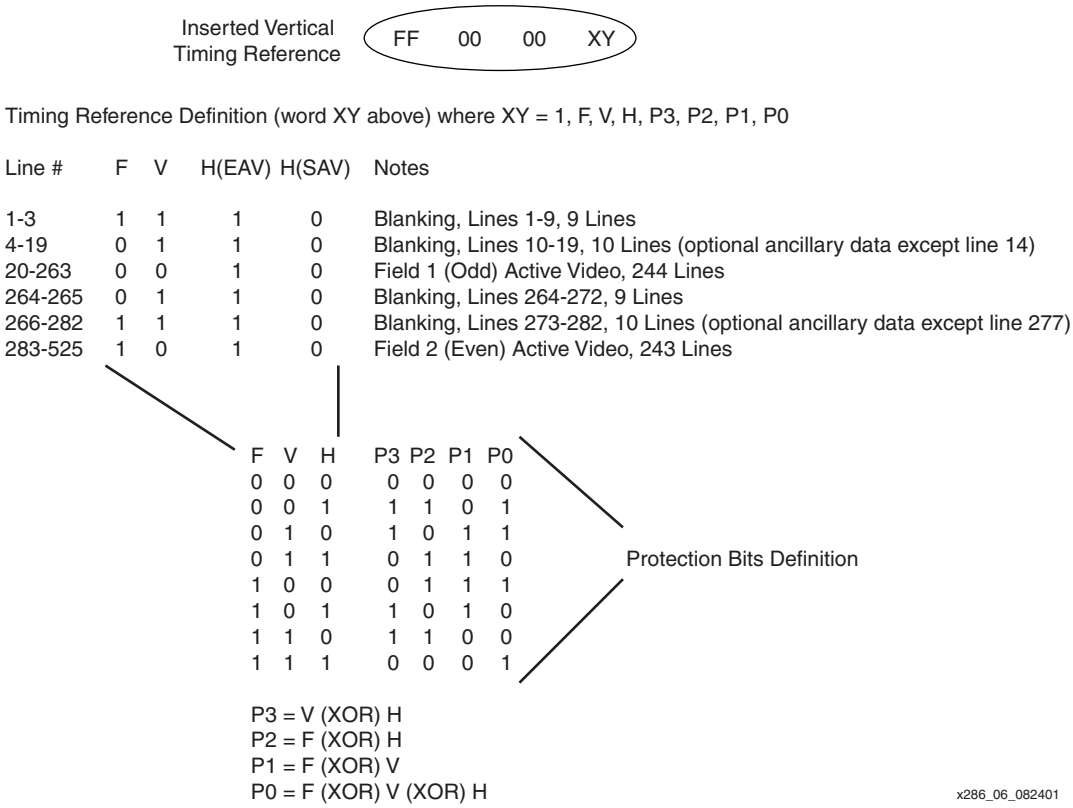


*Figure 6:* **NTSC (525 Line) Vertical Timing Reference (8-bit Implementation)**

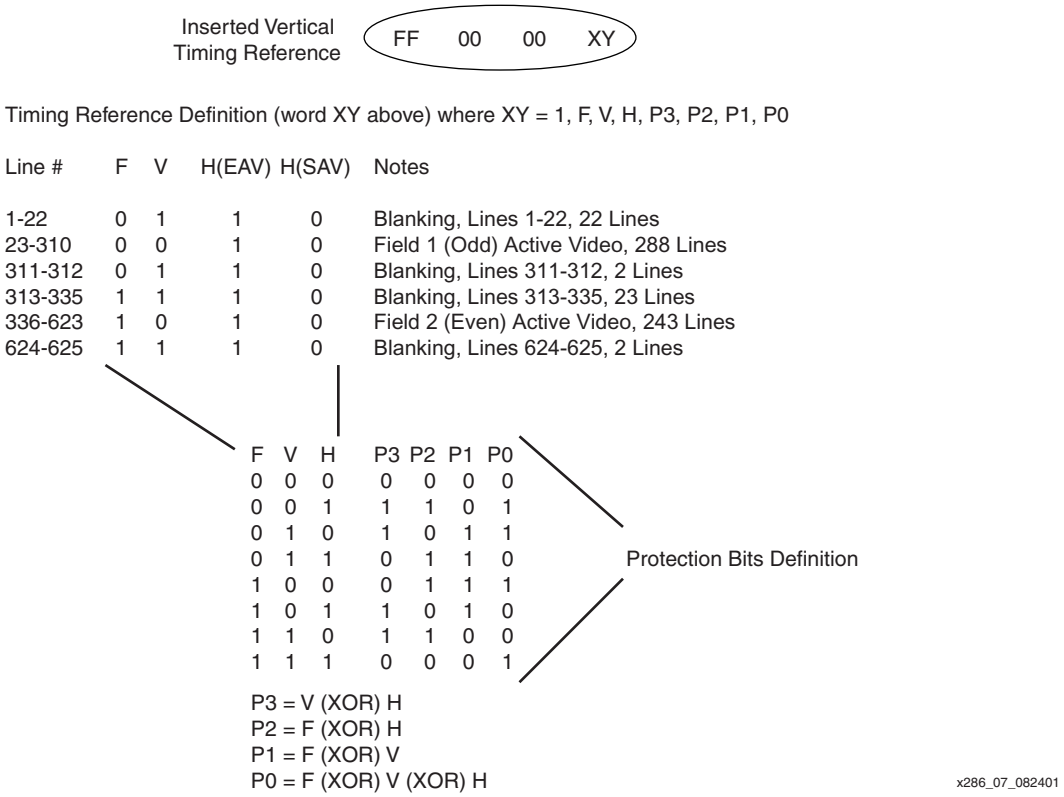


*Figure 7:* **PAL (625 Line) Vertical Timing Reference (8-bit Implementation)**

Figure 8 and Figure 9 shows the vertical detail scope waveforms as if H, V, F, HSYNC, BLANK, and VSYNC were decoded from the digital component video and presented. This is essentially what the line field decoder state machine does.

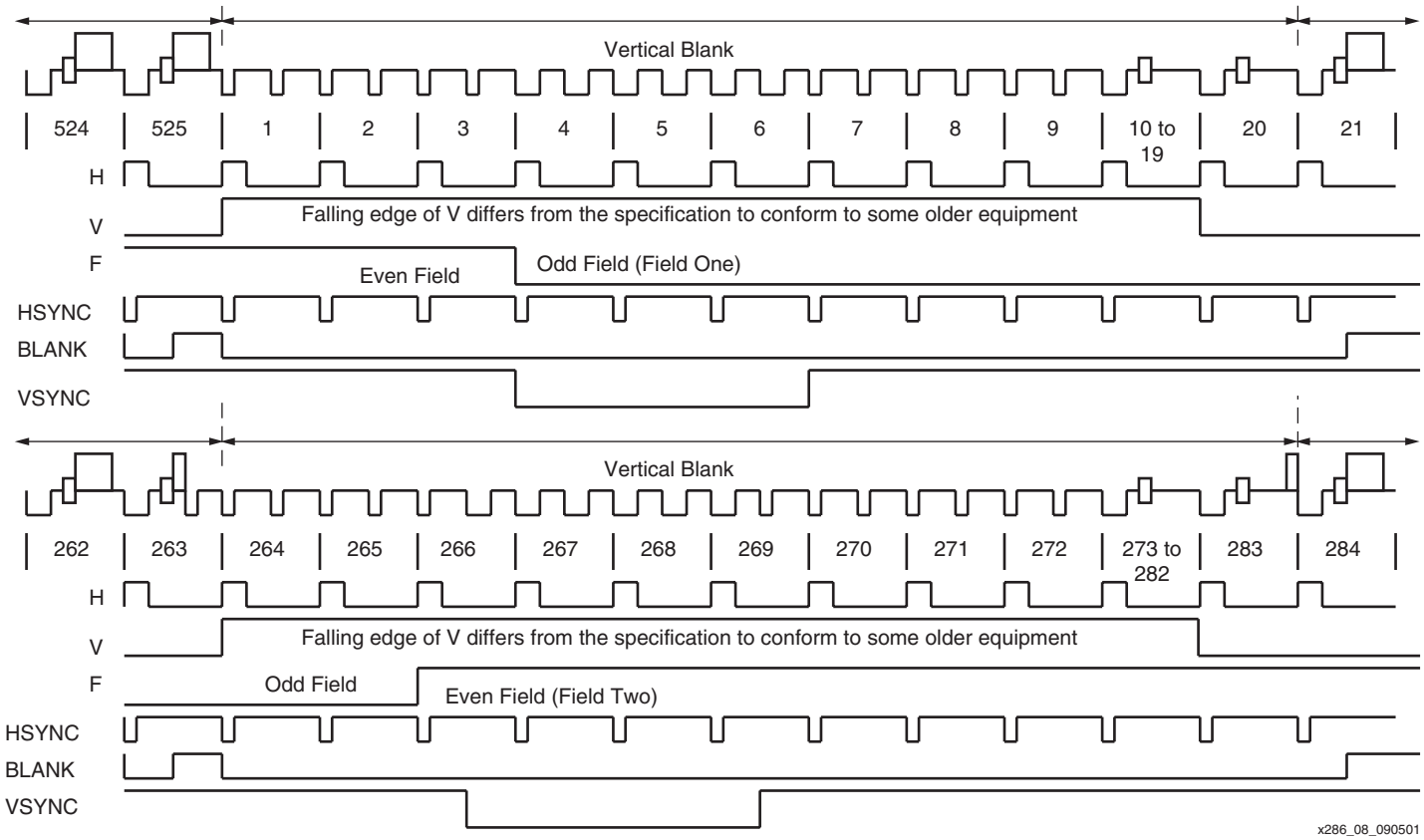


*Figure 8:* **Composite NTSC 525 Vertical Timing Detail**

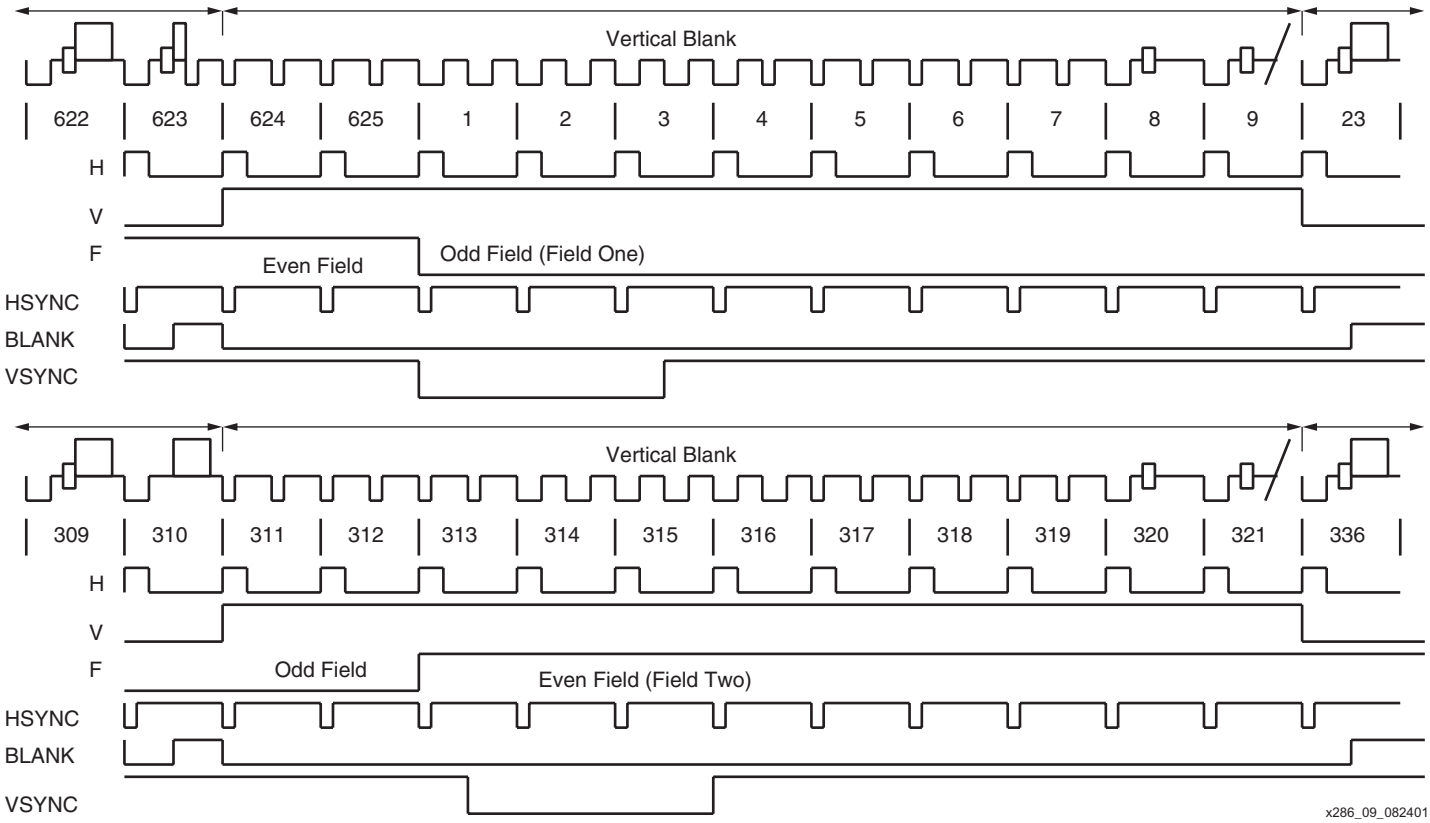


*Figure 9:* **Composite PAL 625 Vertical Timing Detail**

## Reference Design

The reference design for this application note, in both VHDL and Verilog code, is available on the Xilinx FTP site at: ftp://ftp.xilinx.com/pub/applications/xapp/xapp286.zip. A simple description of the video line and field decoder module state machine function is:

1. Auto detect the format by counting clocks between EAV and SAV
2. Determine and output the horizontal sync or H bit
3. Determine and output the Field bit
4. Determine and output the line and pixel count

This "Line Field Decoder" reference design is a modification of the auto-detect module found in XAPP248. It uses the autodetect code to track the TRS symbols and report the format. Steps 2, 3, and 4 are added to support other modules in the demonstration board.

The auto-detect module in XAPP248 examines a digital video stream to determine the matching video standard. The supported video standards are listed in Table 1.

*Table 1:* **Supported Video Standards**

| Video Format | Corresponding Standards |
|---|---|
| NTSC 4:2:2 component video | SMPTE 125M, ITU-R BT.601, ITU-R BT.656 |
| NTSC composite video | SMPTE 244M, SMPTE 259M |
| NTSC 4:4:4 component 13.5 MHz sample | SMPTE RP174 |
| PAL 4:2:2 component video | ITU-R BT.656 |
| PAL composite video | EBU 3280-E |
| PAL 4:2:2 16 x 9 component video | ITU-R BT.601 |
| PAL 4:4:4 component 13.5 MHz sample | ITU-R BT.799 |

Since the Microblaze and Multimedia demonstration board only supports NTSC 4:2:2 component video and PAL 4:2:2 component video, the design could be made smaller by eliminating the other standards. XAPP248 has details of a finite state machine used to track timing reference symbols.

Once TRS symbols are being tracked accurately, the horizontal sync and field bits are decoded by looking at the SAV XY word. The line count must be determined. When the F-bit transitions from Low to High, a line counter can be loaded with the correct value based on the format. If NTSC then load 266, otherwise use the PAL value of 313.

## Conclusion

The design receives a pixel clock (27 MHz) used to clock in each Y', Cr, and Cb value. Currently pixels pass through the module with a delay. Future additions to the module might zero them or duplicate them during blanked portions of a line. This will produce different effects in the 422 to 444 module. The outputs of this module are a signal that suggests the incoming video is NTSC or PAL (PAL_NTSC_out), a line count (lcnt), the H, V, and F signals and the three sync signals, hsync_out, vsync_out, and blank_out. Figure 8 and Figure 9 the signal behavior.

Downstream modules that receive the ITU656 stream will need this information to further process and store the input pixels.

Each input video stream will use this code to allow other data path elements and control elements examining the input video stream to know what format the stream is (NTSC or PAL), and to know what pixels are available and any given time. The simple control logic easily runs at the pixel rate of 27 MHz in the Virtex-II and Spartan-II families.

The results of the synthesis and implementation are included for this simple controller here:

*Table 2:* **Size and Performance Results using FPGA Express 3.5, Xilinx 3.3i**

| Part Number | Flip-Flops | LUT | Ports | Clock Latency | Speed |
|---|---|---|---|---|---|
| XC2V1000-5 | 117 | 152 | 38 | 8 | 8 ns (125 MHz) |
| XC2S200-5 | 117 | 152 | 38 | 8 | 11 ns (91 MHz) |

## References:


1. The video standards beginning with ITU come from the International Telecommunication Union. ITU-R BT.656 and by ITU-R BT.601 standards are available on the International Telecommunication Union's web site, http://www.itu.int/itudoc/itu-r/rec/bt/ for a small fee. The SMPTE or Society of Motion Picture and Television Engineers standards can be found on http://www.smpte.org and will also require membership or a fee.
2. "Video Demystified", by Keith Jack, published by Harris, ISBN 1-878707-23-X, is a good beginners guide to video techniques. It can be read or purchased on line at the following URL; http://www.video-demystified.com
3. Analog Devices ADV7194 Data Sheet, "Professional Extended-10 Video Encoder with 54 MHz Over Sampling". URL: http://www.analog.com


## Revision History

The following table shows the revision history for this document.

| Date | Version | Revision |
|---|---|---|
| 12/13/01 | 1.0 | Initial Xilinx release. |