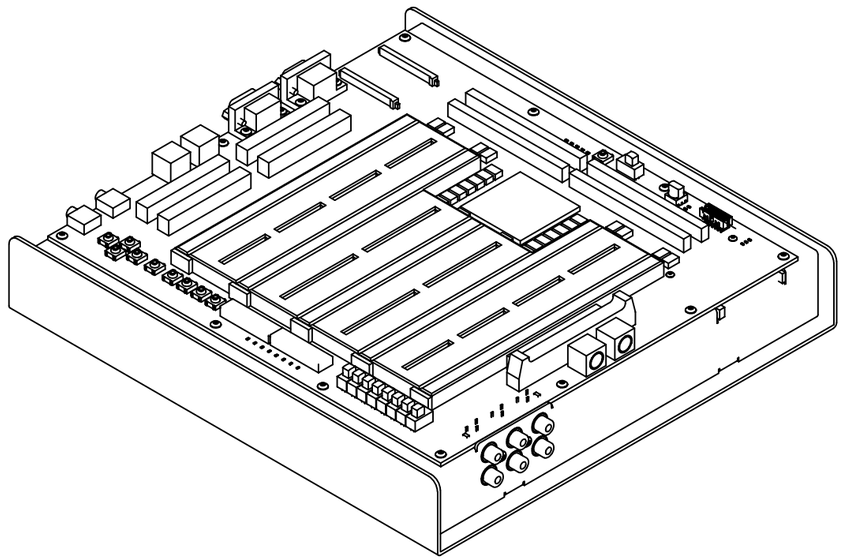
6.111 FPGA LABKIT SCHEMATIC



2 Audio CODEC
3 VGA Ouput
4 Video Encoder (TV Output)
5 Video Decoder (TV Input)
6 RAM Bank 0
7 RAM Bank 1
8 Flash ROM
9 RS–232 and PS/2 Ports
10 Alphanumeric Displays
11 Switches, LEDs, and Clocks
12 User I/O: Banks 1 and 3
13 User I/O: Banks 2 and 4
14 Daughtercard Connectors
15 FPGA I/O Banks 0 and 1
16 FPGA I/O Banks 2 and 3
17 FPGA I/O Banks 4 and 5
18 FPGA I/O Banks 6 and 7
19 FPGA Power
20 SystemACE CompactFlash Port
21 SystemACE MPU and JTAG Ports
22 SystemACE Power
23 Configuration EPROMs
24 Configuration Logic
25 Power Supplies
26 Breadboards
27 Logic Analyzer Connectors
28 Case Wiring
29 Revision History

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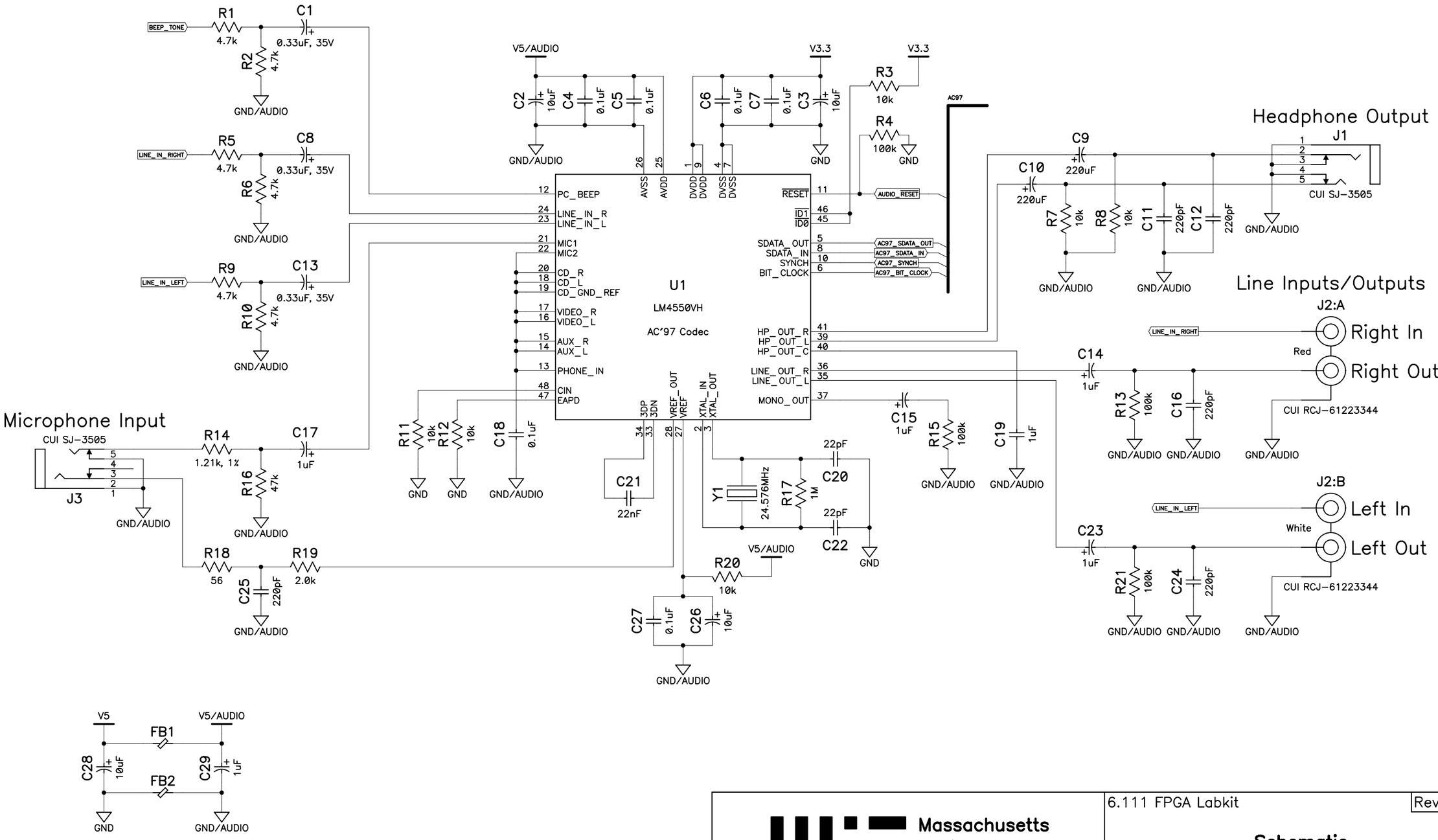
Schematic

Title Sheet

Sheet 1 of 29 | Wed Feb 09, 2005

Designed by N. Ickes (MIT), R. Ballantyne (Xilinx)



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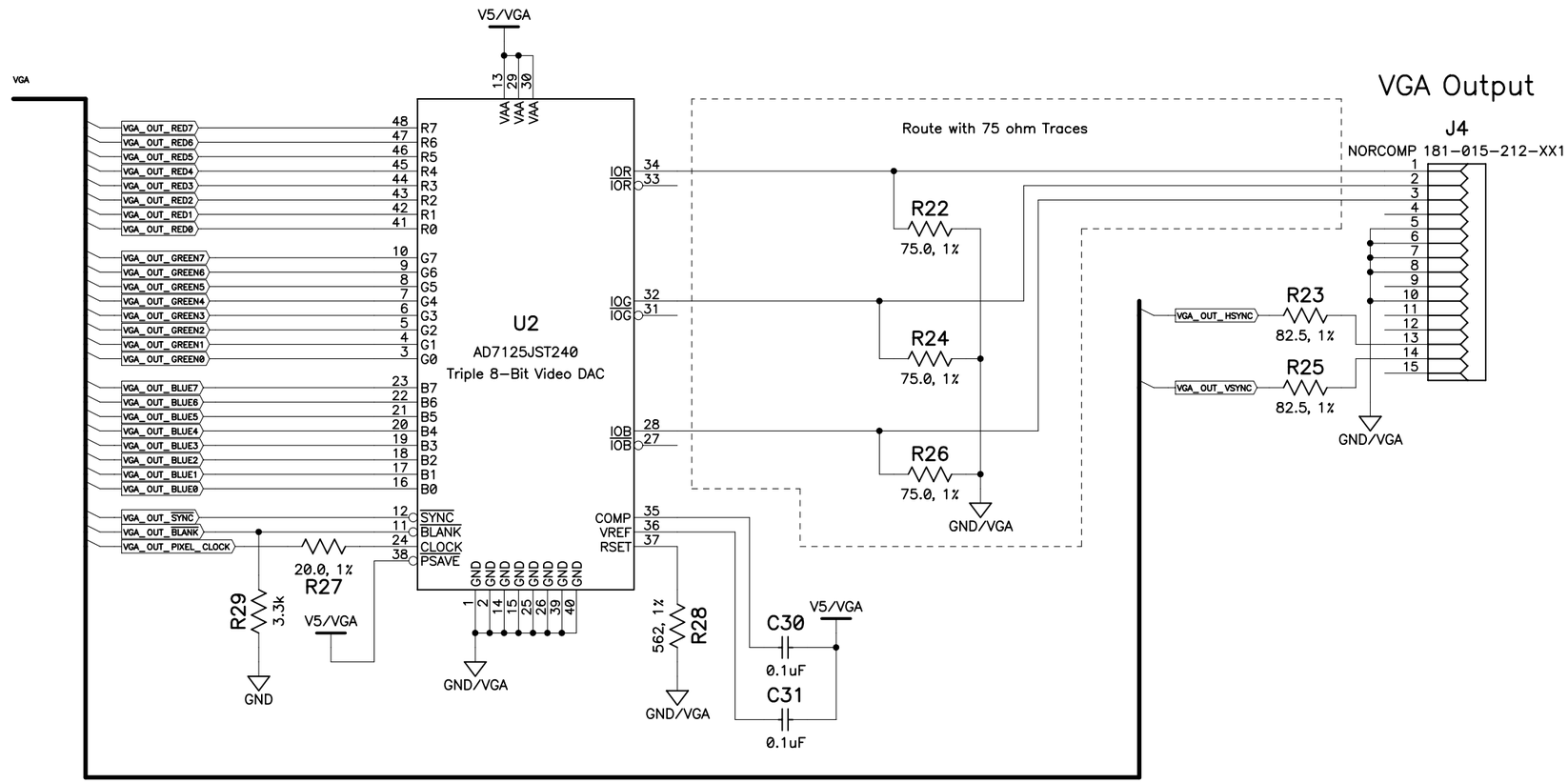
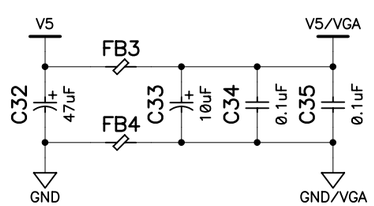
Schematic

Audio CODEC

Sheet 2 of 29 — Wed Feb 09, 2005

Designed by N. Ickes (MIT), R. Ballantyne (Xilinx)





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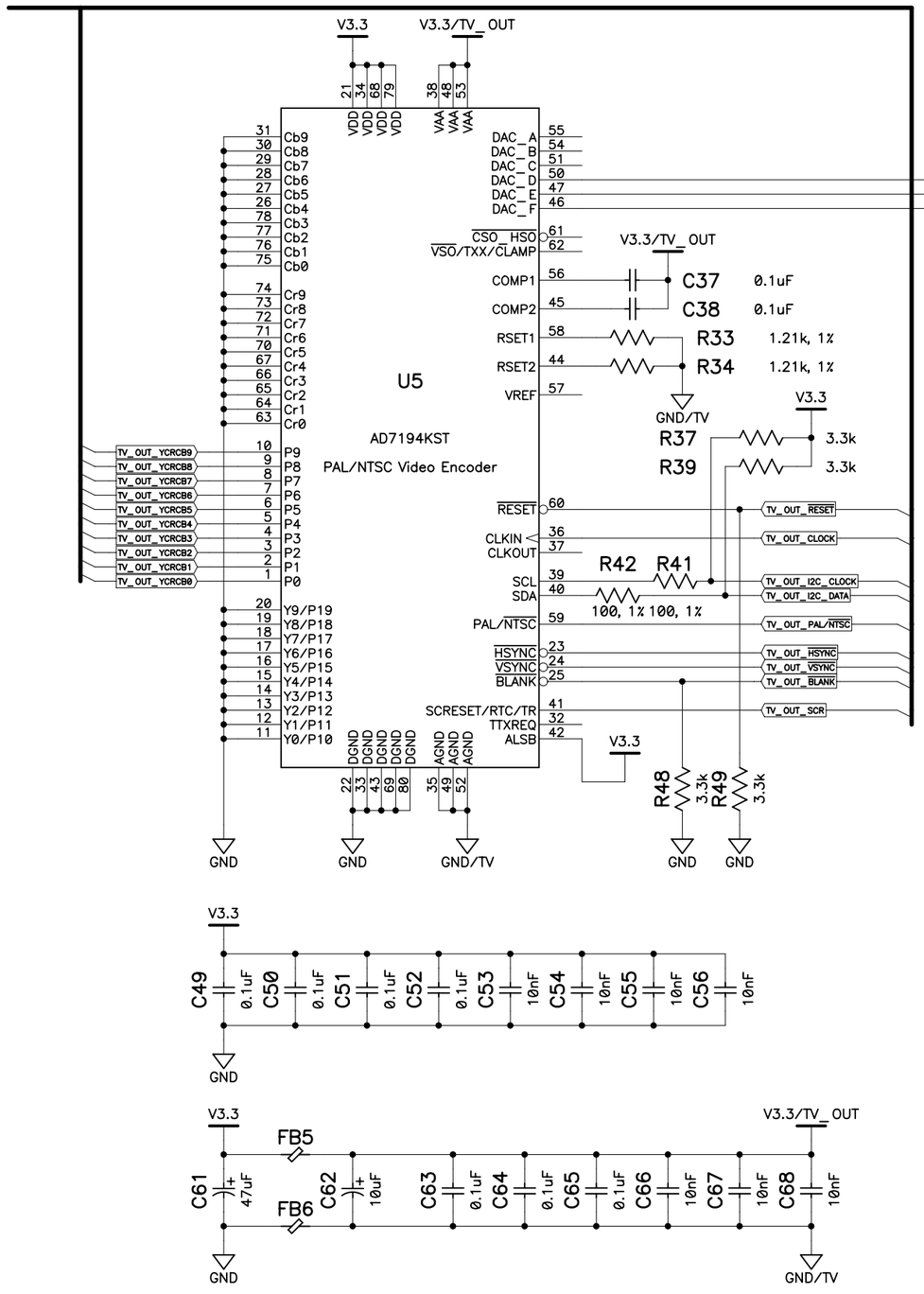
Schematic

VGA Ouput

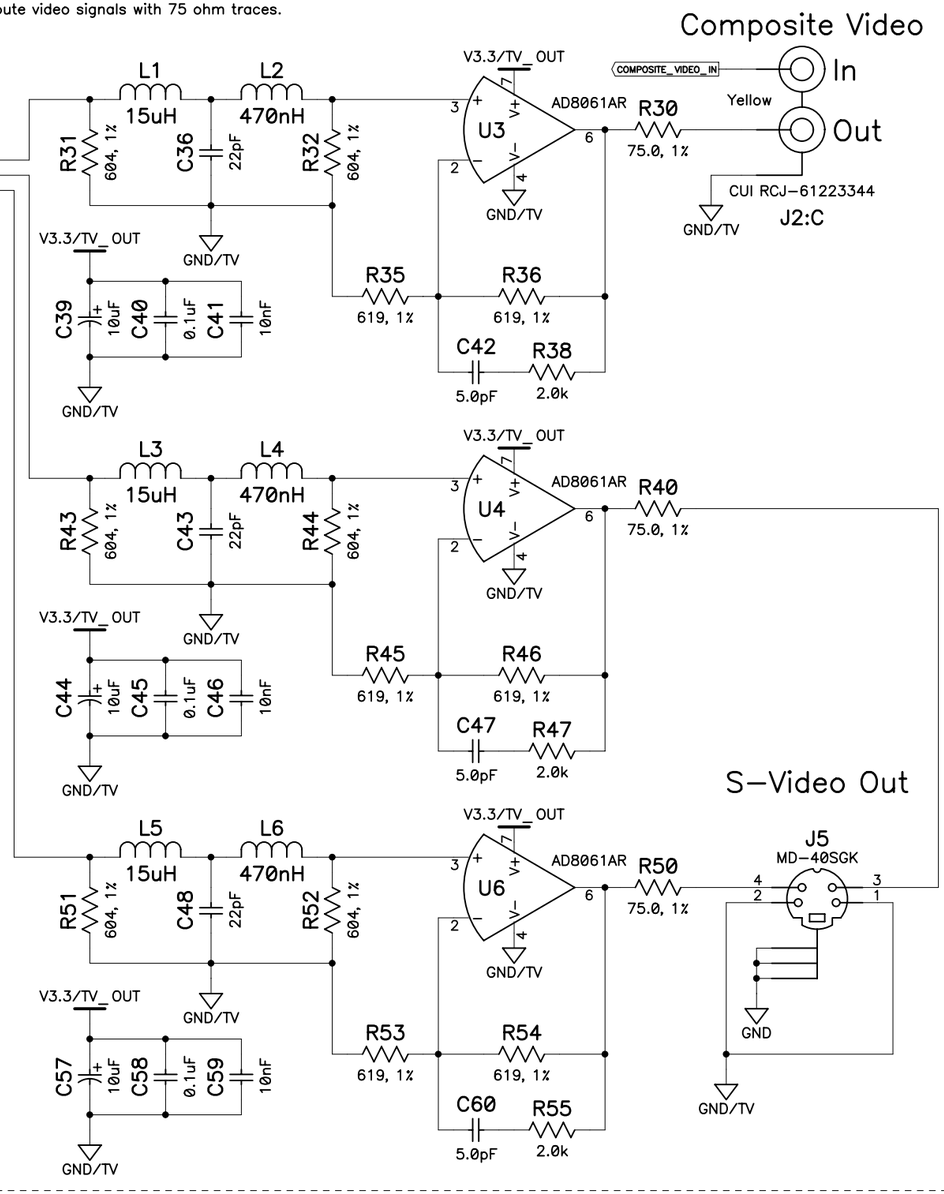
Sheet 3 of 29 | Wed Feb 09, 2005

Designed by N. Ickes (MIT), R. Ballantyne (Xilinx)

TV_OUT



Route video signals with 75 ohm traces.



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Schematic

Video Encoder (TV Output)

Sheet 4 of 29 | Wed Feb 09, 2005

Designed by N. Ickes (MIT), R. Ballantyne (Xilinx)

Route video signals with 75 ohm traces.

S-Video In

J6
MD-40SGK

U7
ADV7185KST
Video Decoder

RP1
EXB2HV
56

RP2:D 56
RP2:C 56
RP2:B 56
RP2:A 56

RP3 EXB2HV
56

RP2:E 56
RP2:F 56
RP2:G 56
RP2:H 56

R56 75.0, 1%
R59 75.0, 1%
R60 75.0, 1%
R61 100, 1%
R62 100, 1%
R57 3.3k
R58 3.3k
R63 56
R64 56
R65 3.3k
R66 5.62k, 1%

C69 0.1uF
C70 0.1uF
C71 0.1uF
C72 10uF
C73 0.1uF
C74 0.1uF
C75 0.1uF
C76 10uF
C77 0.1uF
C78 0.1uF
C79 2.2nF, NPO
C80 0.1uF
C81 68pF, NPO
C82 10uF
C83 0.1uF
C84 0.1uF
C85 47uF
C86 10uF
C87 47uF
C88 10uF
C89 47uF
C90 10uF
C91 0.1uF
C92 10nF
C93 0.1uF
C94 10nF
C95 10nF
C96 10nF
C97 10nF
C98 0.1uF
C99 0.1uF
C100 0.1uF
C101 10nF
C102 10nF
C103 0.1uF
C104 0.1uF

FB7
FB8
FB9

V5
V5/TV_A
V5/TV_P
V3.3
V3.3/TV_IN
GND
GND/TV

COMPOSITE_VIDEO_IN
LUMA_IN
CHROMA_IN

AIN1 AVSS1 AIN2 AVSS2 AIN3 AVSS3 AIN4 AVSS4 AIN5 AVSS5 AIN6 AVSS6
REFOUT CML CAPY1 CAPY2 CAPC1 CAPC2 XTAL1 XTAL2 ALSB ELPF
AVDD DVDD DVSS DVSSIO PWRDN RESET ISO
P19 P18 P17 P16 P15 P14 P13 P12 P11 P10 P9 P8 P7 P6 P5 P4 P3 P2 P1 P0
SCLOCK SDATA RD DV OE VREF/VRESET HREF/HRESET LLCREF LLC2 LLC1/PCLK AEF HFF/QCLK/GL AFF CLKIN FIELD HS/HACTIVE VS/VACTIVE

TV_IN
TV_IN_YCRCB_19 TV_IN_YCRCB_18 TV_IN_YCRCB_17 TV_IN_YCRCB_16 TV_IN_YCRCB_15 TV_IN_YCRCB_14 TV_IN_YCRCB_13 TV_IN_YCRCB_12 TV_IN_YCRCB_11 TV_IN_YCRCB_10 TV_IN_YCRCB_9 TV_IN_YCRCB_8 TV_IN_YCRCB_7 TV_IN_YCRCB_6 TV_IN_YCRCB_5 TV_IN_YCRCB_4 TV_IN_YCRCB_3 TV_IN_YCRCB_2 TV_IN_YCRCB_1 TV_IN_YCRCB_0
TV_IN_I2C_CLOCK TV_IN_I2C_DATA TV_IN_FIFO_READ TV_IN_DATA_VALID TV_IN_LINE_CLOCK_2 TV_IN_LINE_CLOCK_1 TV_IN_AEF TV_IN_HFF TV_IN_AFF TV_IN_FIFO_CLOCK TV_IN_ISO TV_IN_RESET TV_IN_CLOCK

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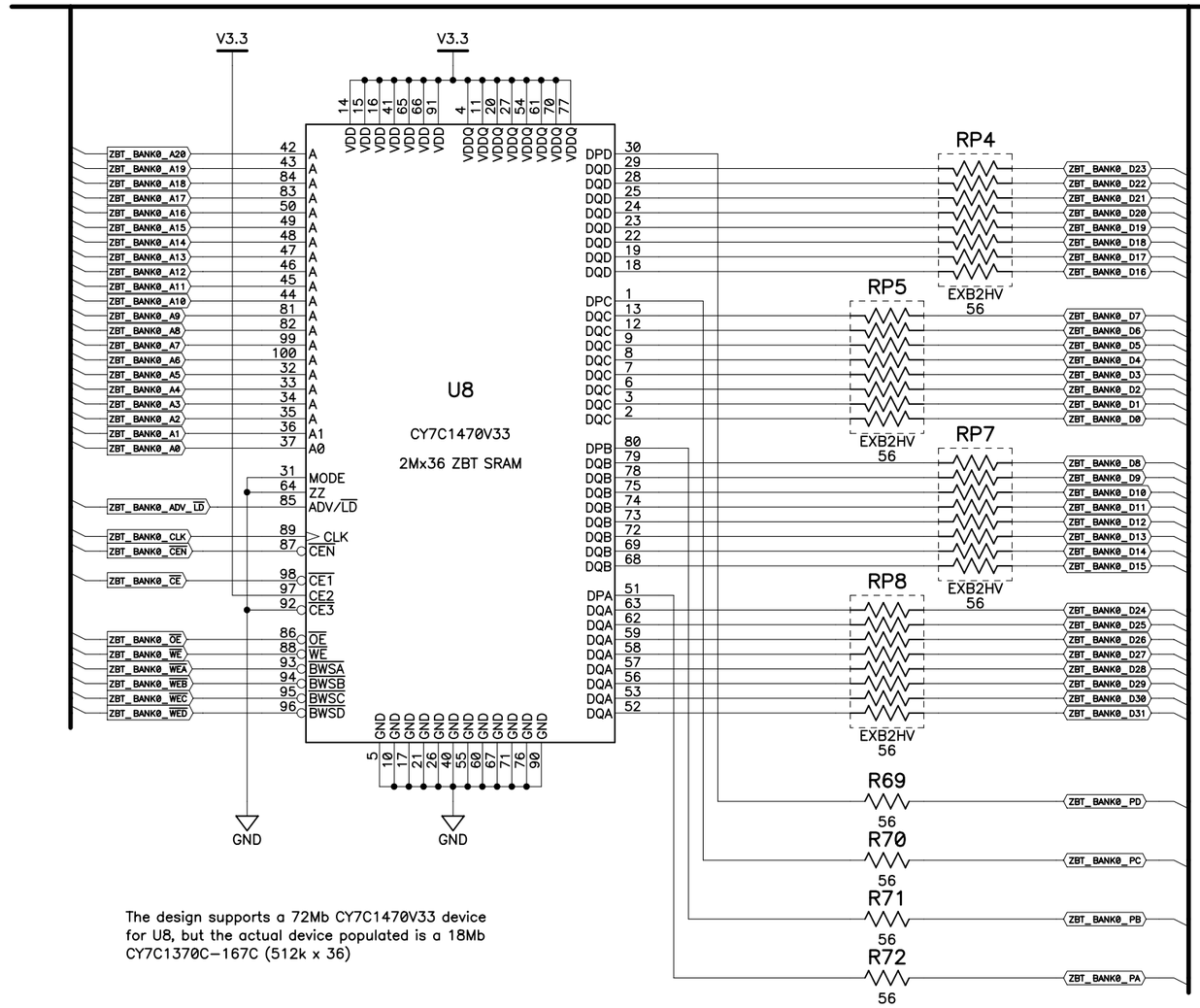
Schematic

Video Decoder (TV Input)

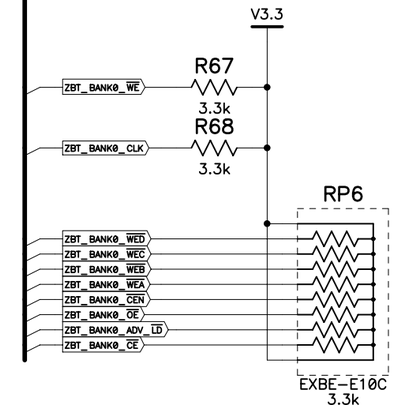
Sheet 5 of 29 | Wed Feb 09, 2005

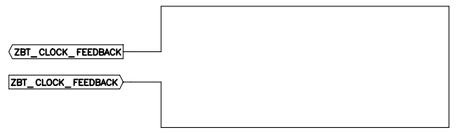
Designed by N. Ickes (MIT), R. Ballantyne (Xilinx)

RAM_BANK_0



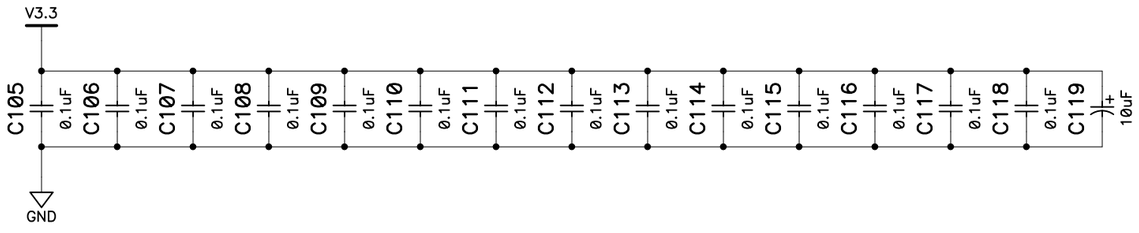
The design supports a 72Mb CY7C1470V33 device for U8, but the actual device populated is a 18Mb CY7C1370C-167C (512k x 36)





All SRAM data, address, and control signal traces are 2.100in long.

The ZBT_CLOCK_FEEDBACK loop is also 2.100in long and is used to de-skew the SRAM clock



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Schematic

RAM Bank 0

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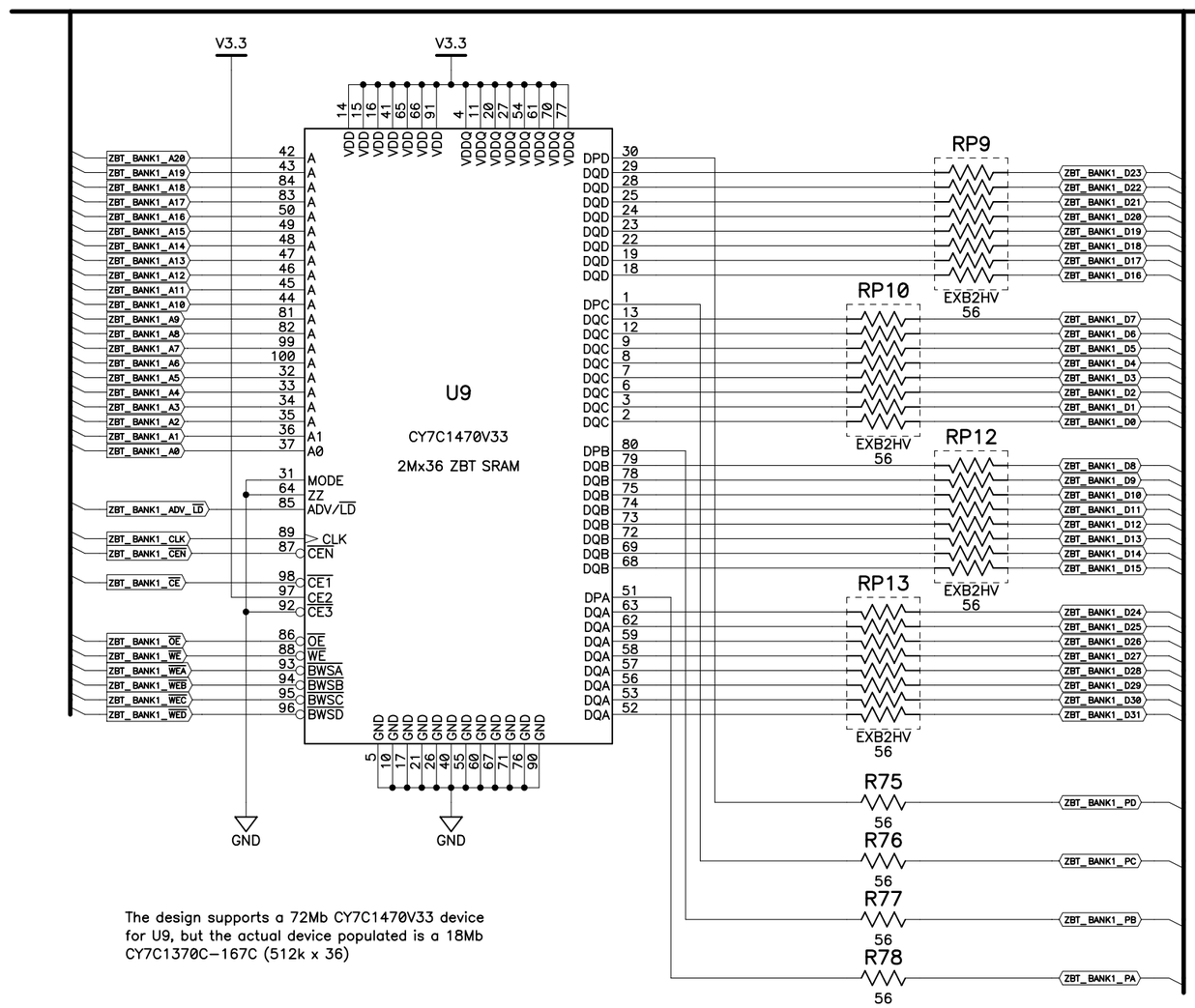
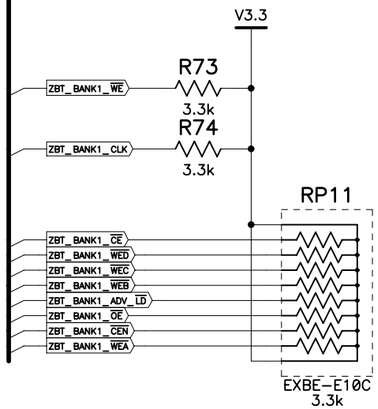
Designed by N. Ickes (MIT), R. Ballantyne (Xilinx)

RAM_BANK_1

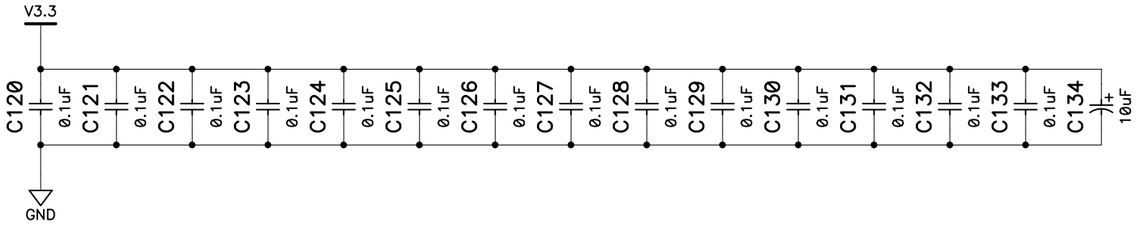


The design supports a 72Mb CY7C1470V33 device for U9, but the actual device populated is a 18Mb CY7C1370C–167C (512k x 36)



All SRAM data, address, and control signal traces are 2.100in long.

The ZBT_CLOCK_FEEDBACK loop is also 2.100in long and is used to de–skew the SRAM clock



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Schematic

RAM Bank 1

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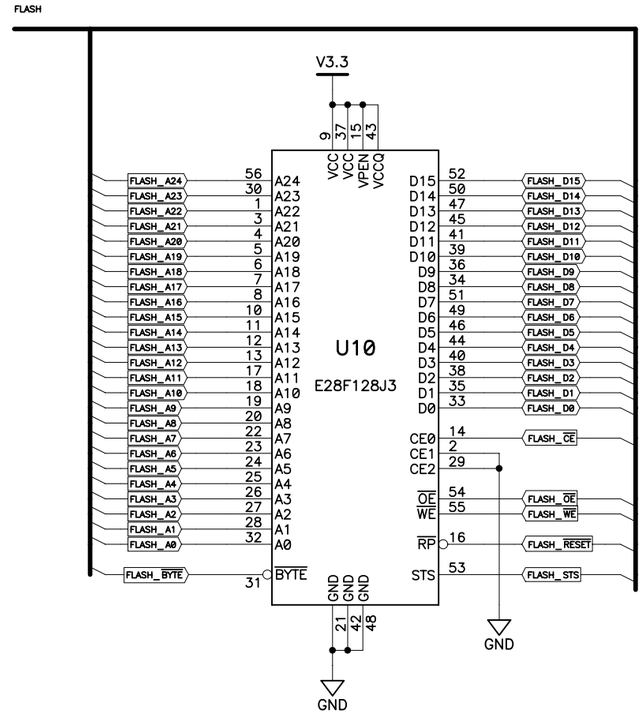
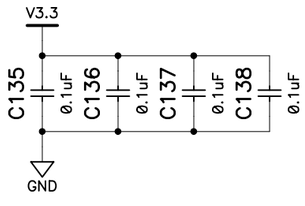
FLASH





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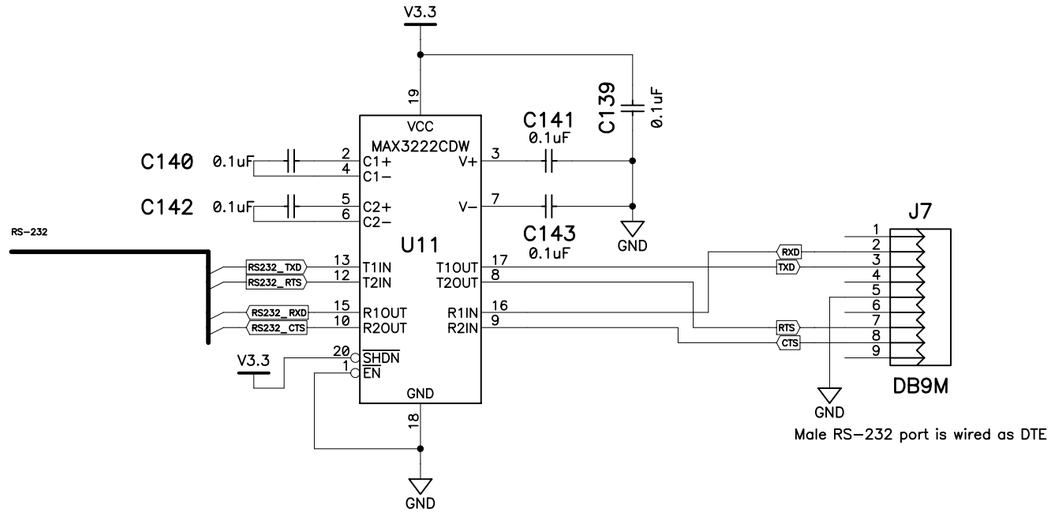
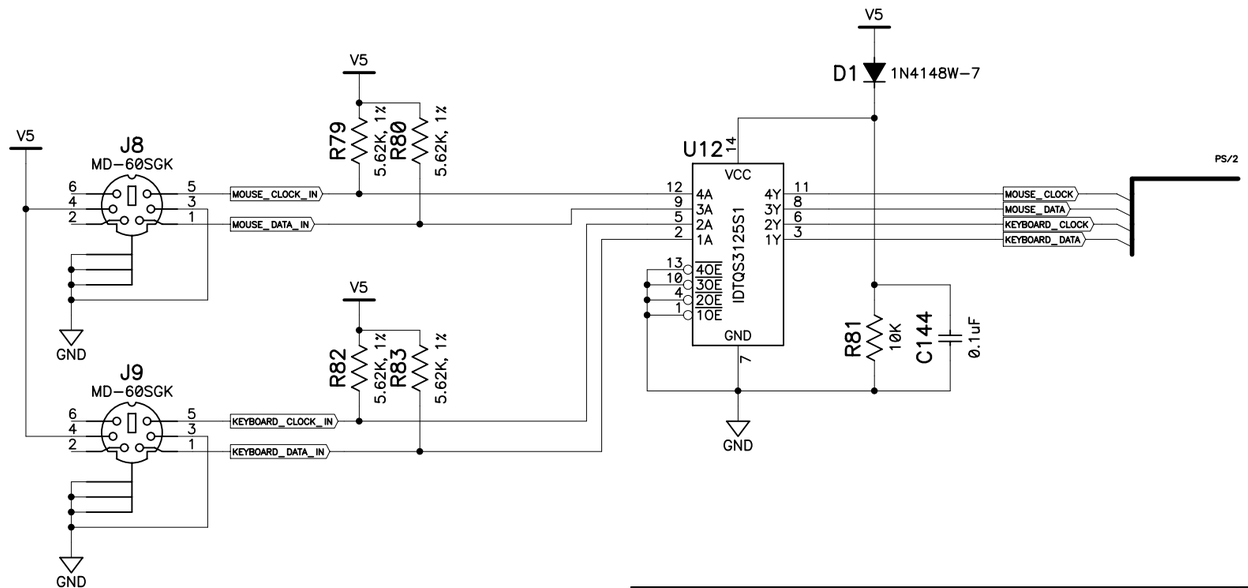
Schematic

Flash ROM

Sheet 8 of 29 | Wed Feb 09, 2005

Designed by N. Ickes (MIT), R. Ballantyne (Xilinx)





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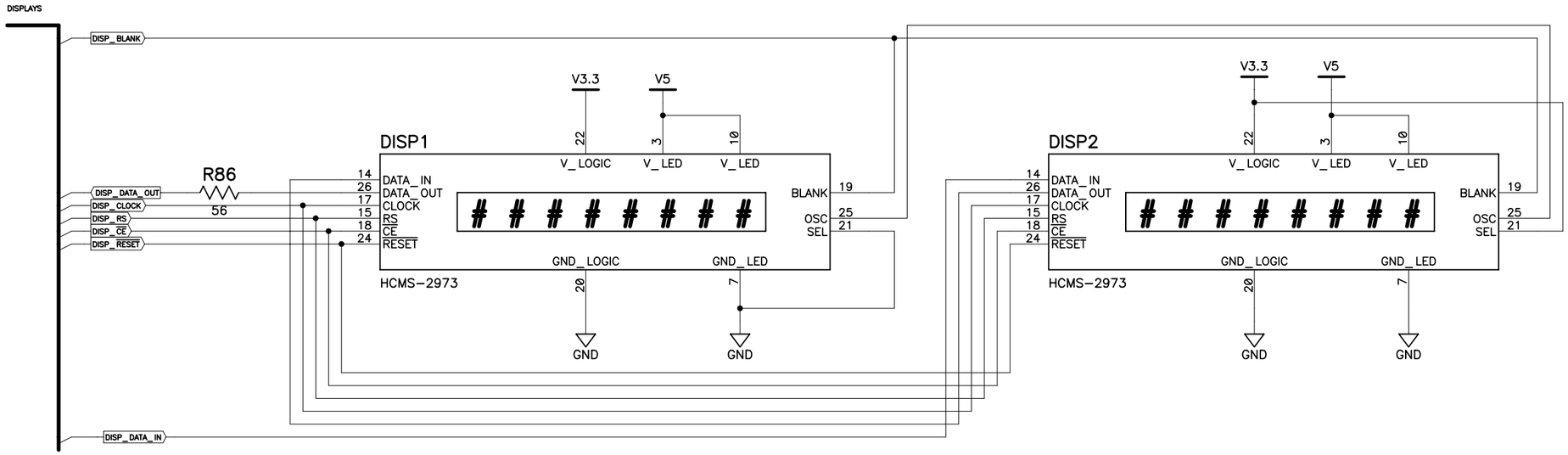
Schematic

RS–232 and PS/2 Ports

Sheet 9 of 29 — Wed Feb 09, 2005

Designed by N. Ickes (MIT), R. Ballantyne (Xilinx)



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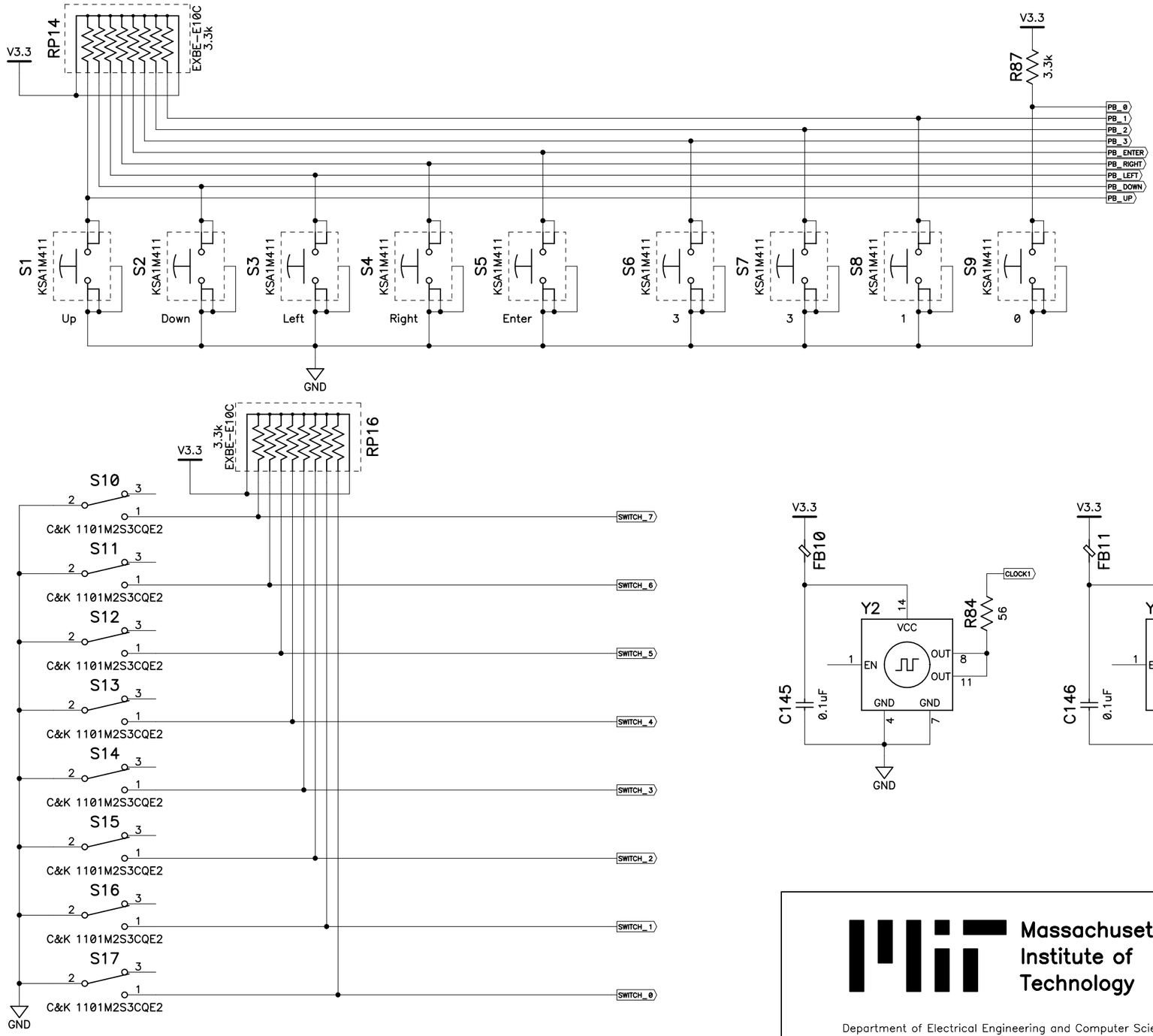
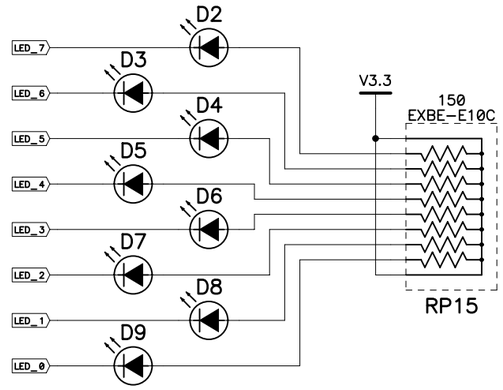
Schematic

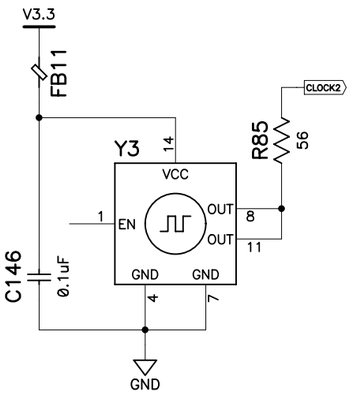
Alphanumeric Displays

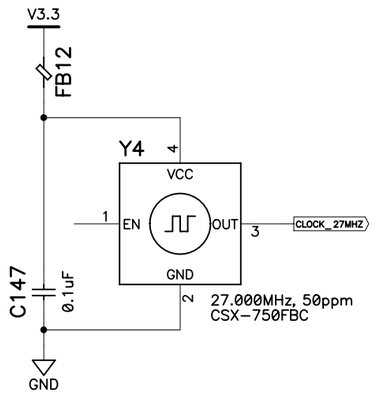
Sheet 10 of 29 — Wed Feb 09, 2005

Designed by N. Ickes (MIT), R. Ballantyne (Xilinx)









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Schematic

Switches, LEDs, and Clocks

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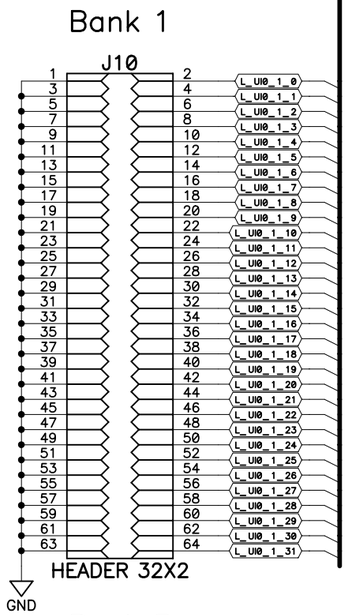
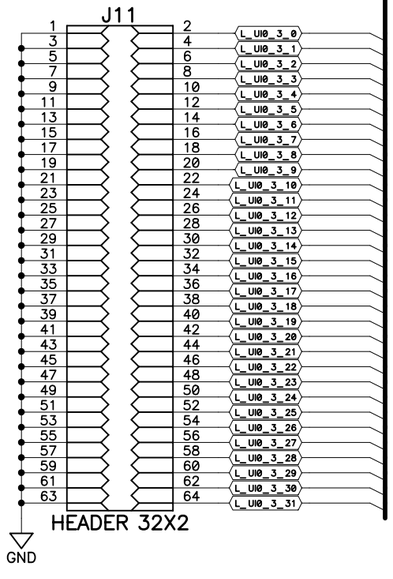
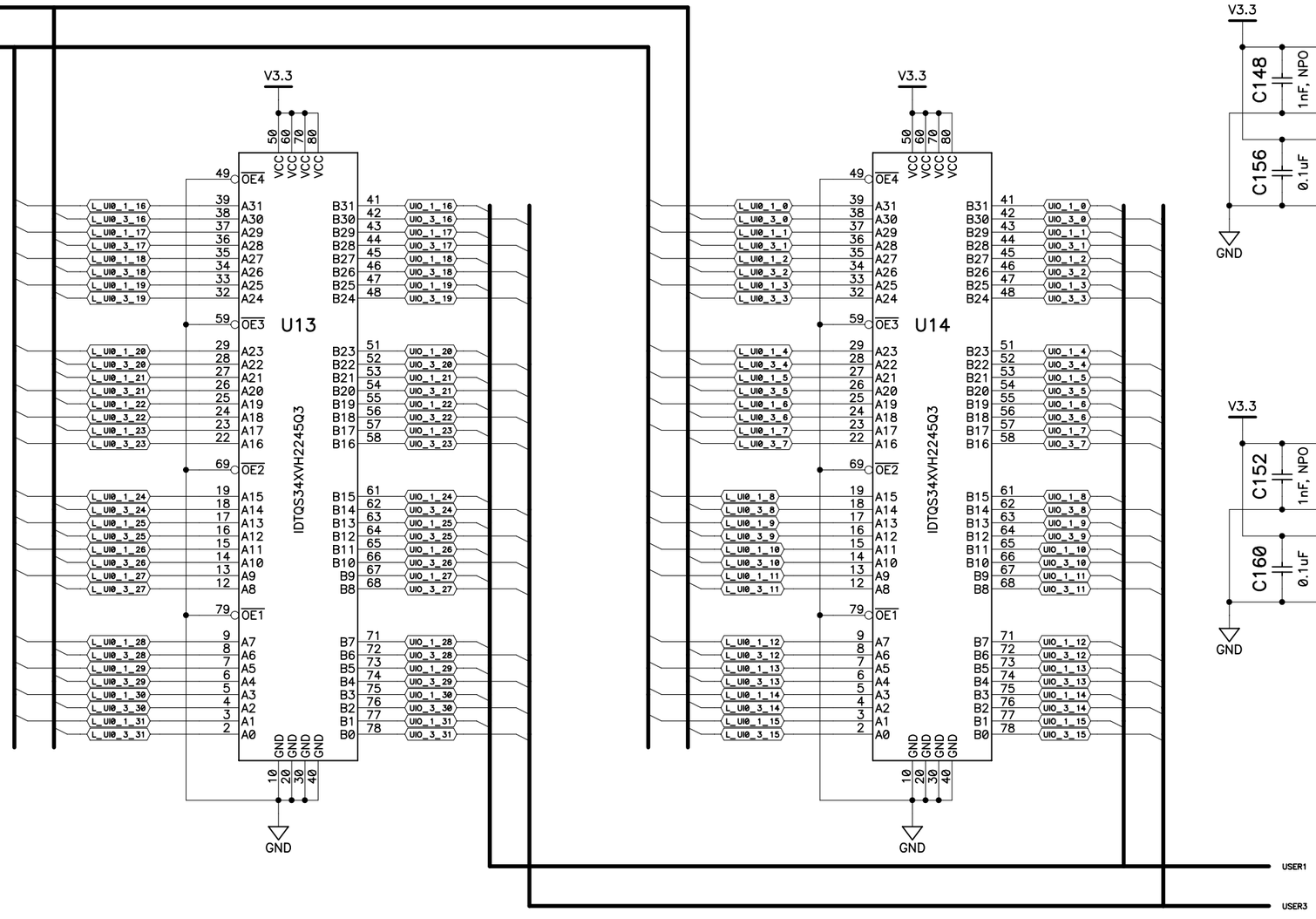
Designed by N. Ickes (MIT), R. Ballantyne (Xilinx)

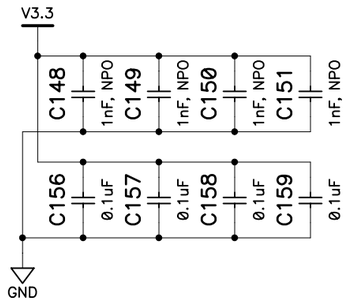
Bank 1

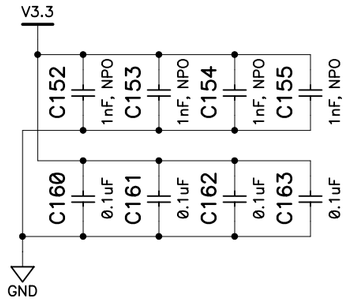


Bank 3









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Schematic

User I/O Banks 1 & 3

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Bank 2

J12

HEADER 32X2

Bank 4

J13

HEADER 32X2

U15

U16

IDTQS34XVH2245Q3

V3.3

GND

C164 1nF, NPO
C165 1nF, NPO
C166 1nF, NPO
C167 1nF, NPO
C172 0.1uF
C173 0.1uF
C174 0.1uF
C175 0.1uF

C168 1nF, NPO
C169 1nF, NPO
C170 1nF, NPO
C171 1nF, NPO
C176 0.1uF
C177 0.1uF
C178 0.1uF
C179 0.1uF

USER2

USER4

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Schematic

User I/O Banks 2 & 4

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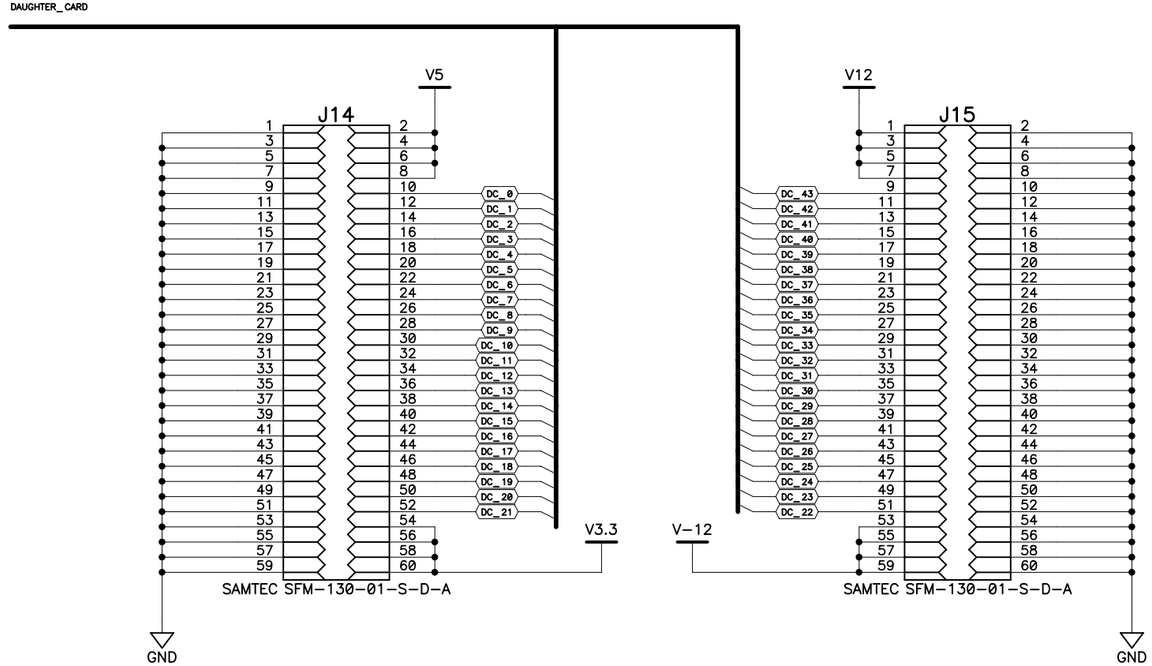
Wed Feb 09, 2005

Designed by N. Ickes (MIT), R. Ballantyne (Xilinx)

DAUGHTER_CARD



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Schematic

Daughter Card Connectors

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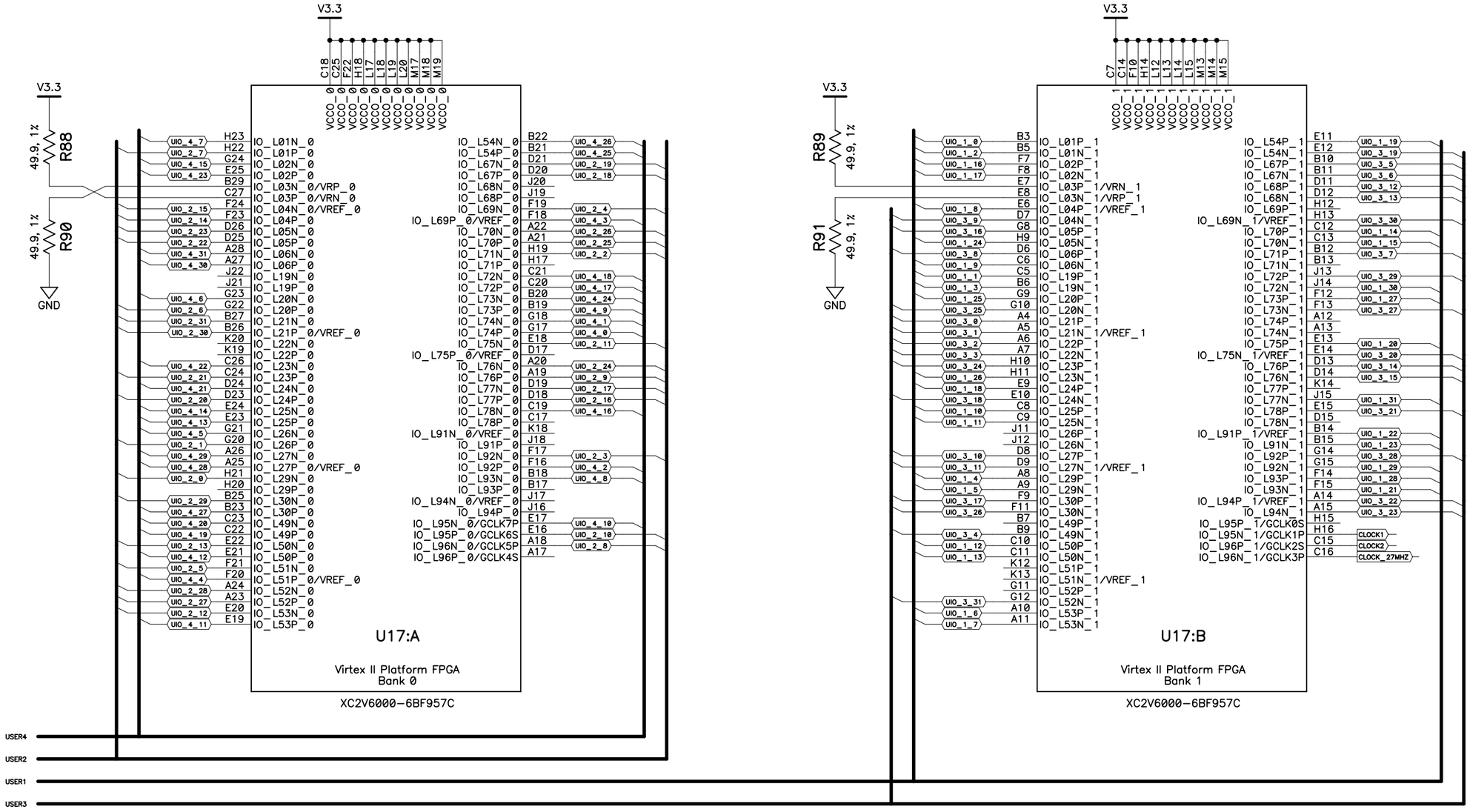
Designed by N. Ickes (MIT), R. Ballantyne (Xilinx)



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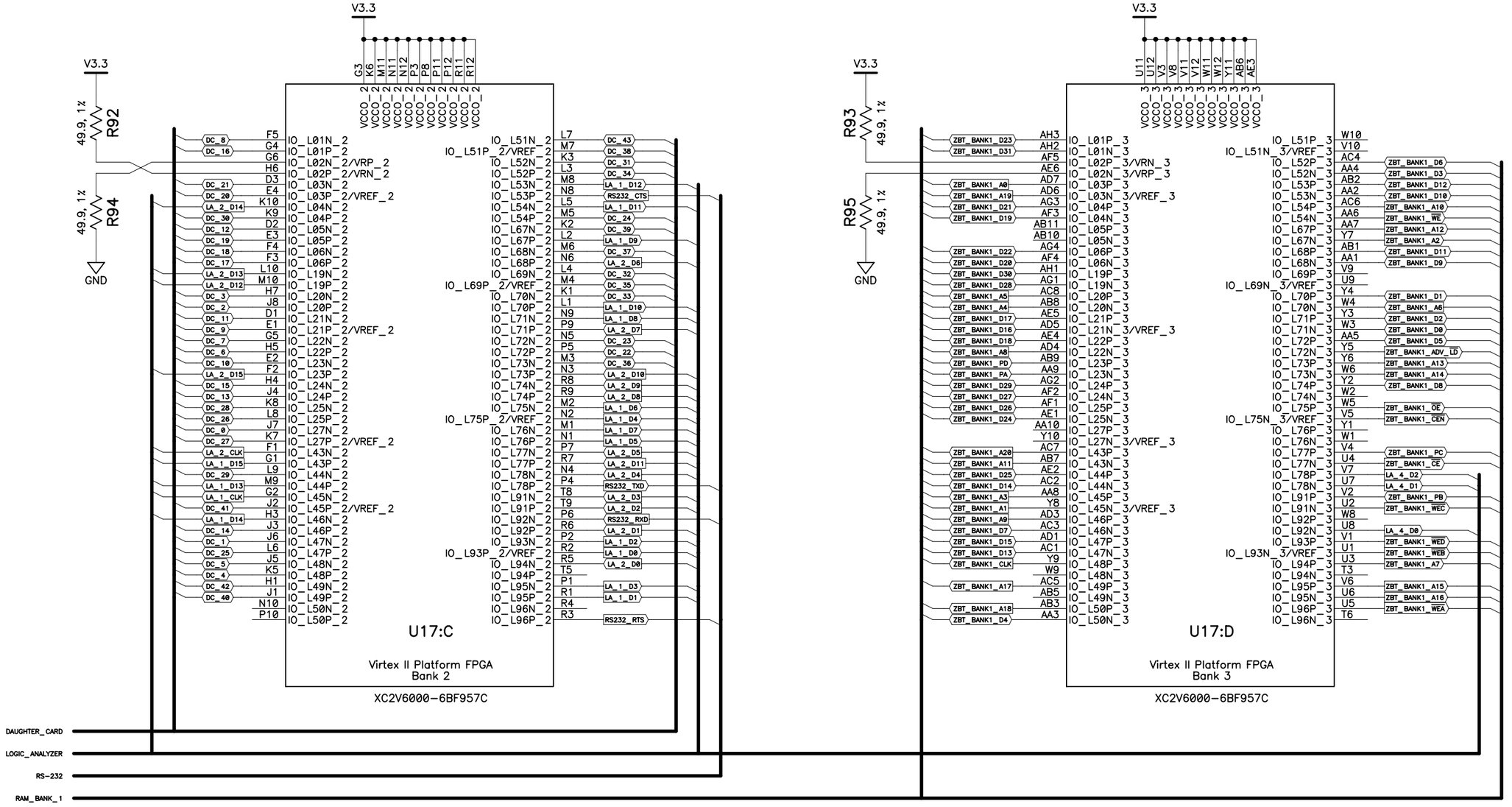
Schematic

FPGA I/O Banks 0 and 1

Sheet 15 of 29 | Wed Feb 09, 2005

Designed by N. Ickes (MIT), R. Ballantyne (Xilinx)



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Schematic

FPGA I/O Banks 2 and 3

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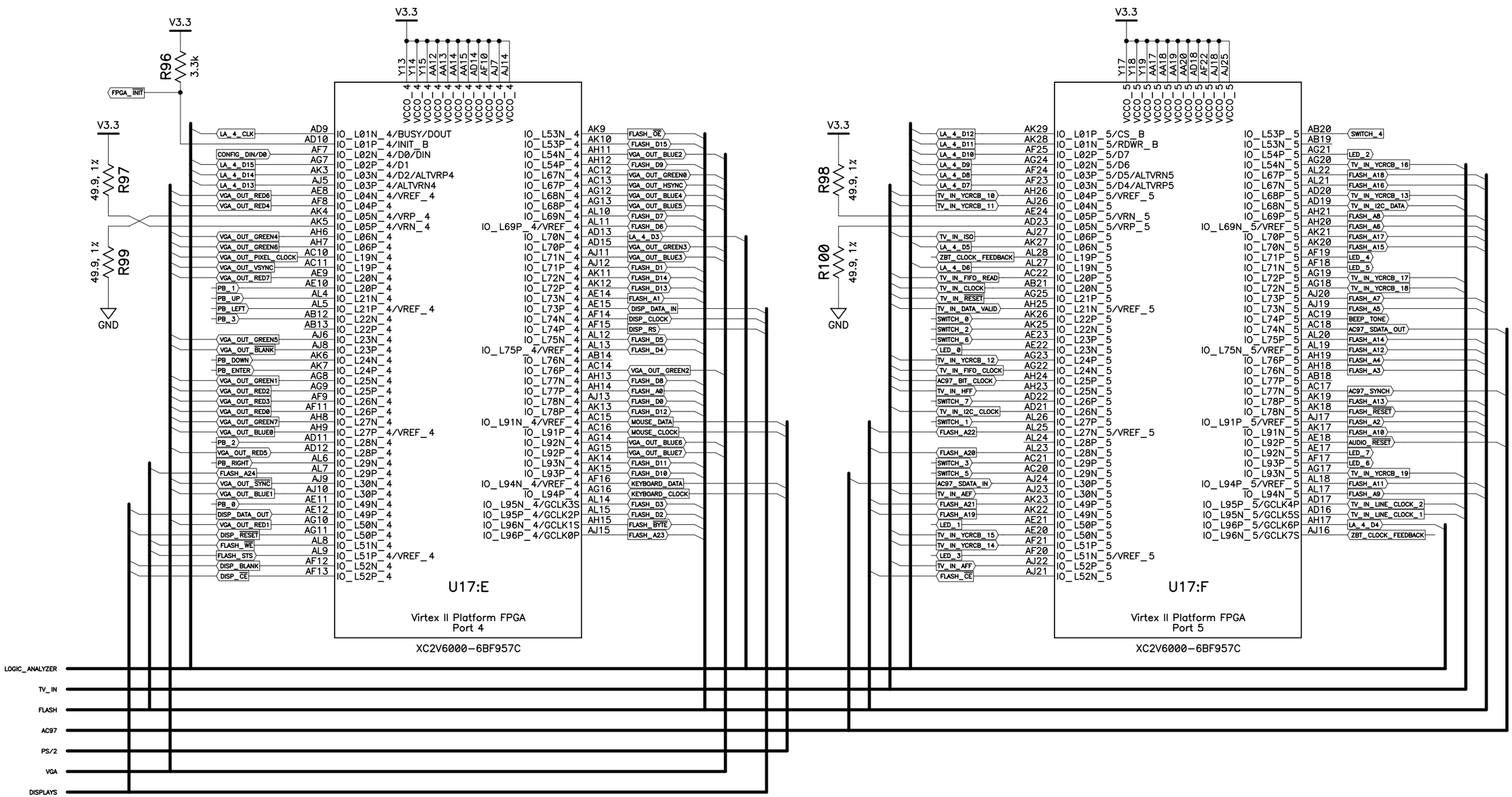
Designed by N. Ickes (MIT), R. Ballantyne (Xilinx)



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Schematic

FPGA I/O Banks 4 and 5

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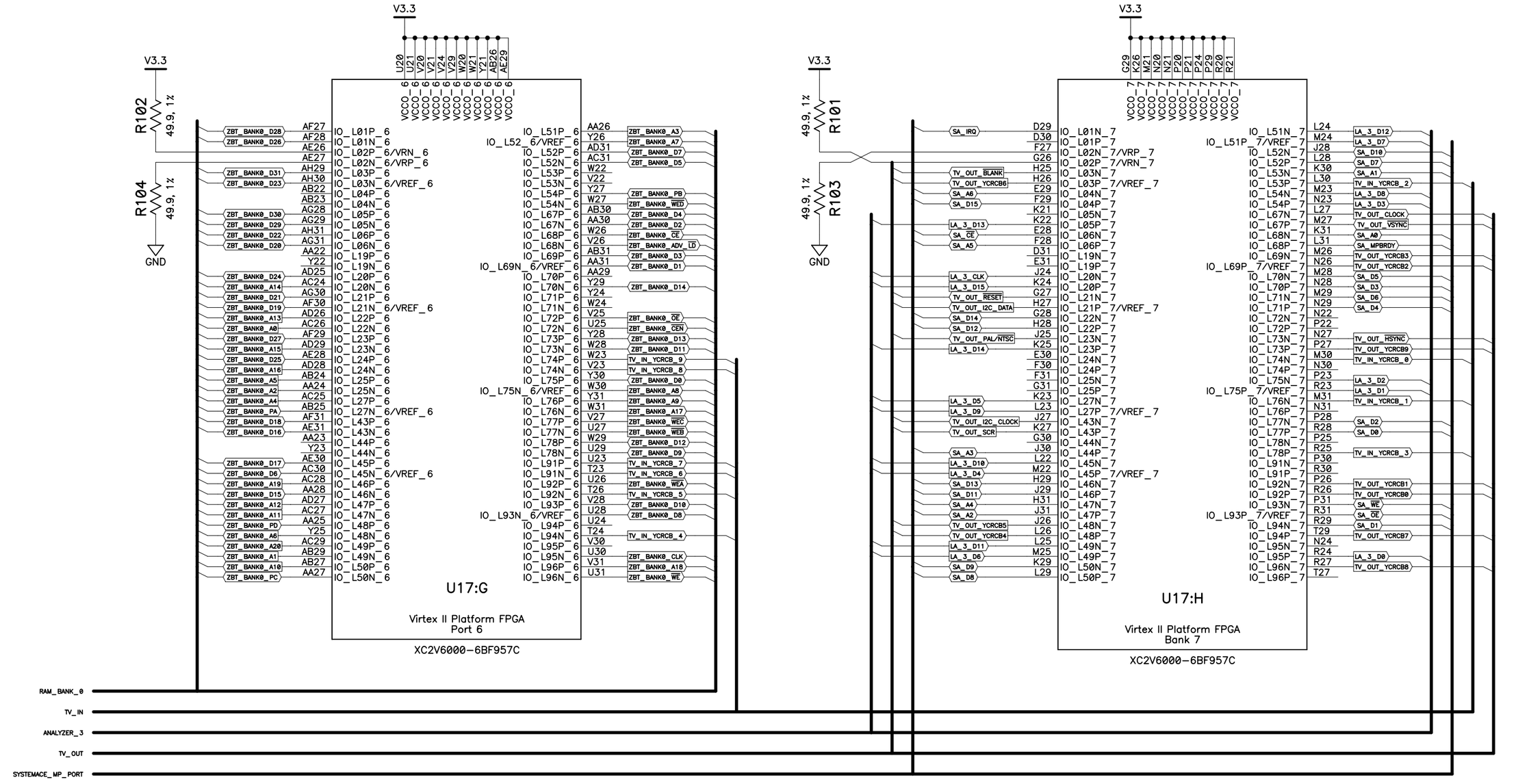
Designed by N. Ickes (MIT), R. Ballantyne (Xilinx)



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Schematic

FPGA I/O Banks 6 and 7

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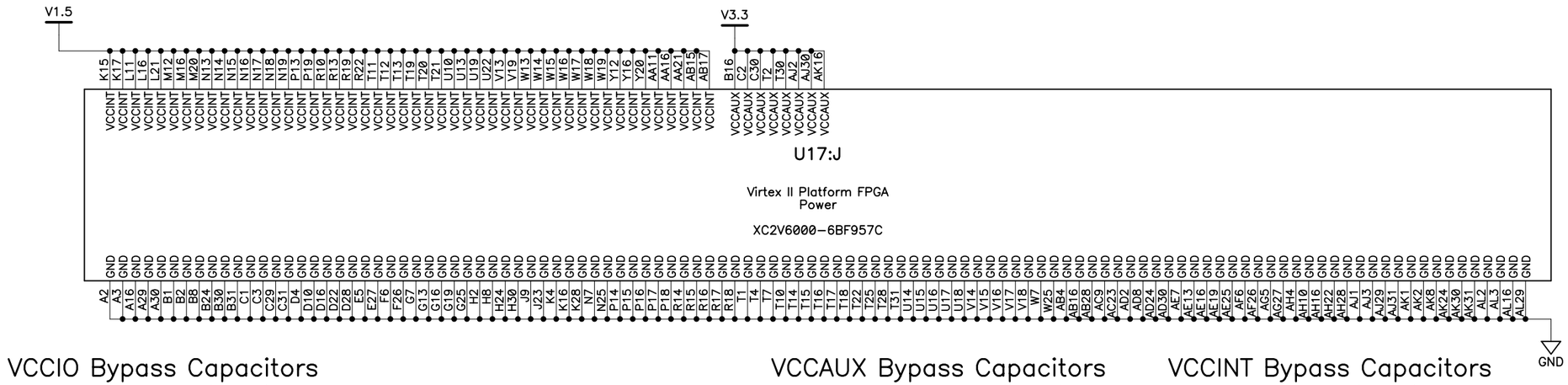
Designed by N. Ickes (MIT), R. Ballantyne (Xilinx)



VCCIO Bypass Capacitors

47uF, Tantalum, Size D (8 places)

V3.3 C180 C181 C182 C183 C184 C185 C186 C187

0.1uF, X7R, 0603 (44 places)

C201 C202 C203 C204 C205 C206 C207 C208 C209 C210 C211 C212 C213 C214 C215 C216 C217 C218 C219 C220 C221 C222

C243 C244 C245 C246 C247 C248 C249 C250 C251 C252 C253 C254 C255 C256 C257 C258 C259 C260 C261 C262 C263 C264

10nF, X7R, 0603 (22 places)

C281 C282 C283 C284 C285 C286 C287 C288 C289 C290 C291 C292 C293 C294 C295 C296 C297 C298 C299 C300 C301 C302

1nF, NPO, 0603 (22 places)

C319 C320 C321 C322 C323 C324 C325 C326 C327 C328 C329 C330 C331 C332 C333 C334 C335 C336 C337 C338 C339 C340

GND

VCCAUX Bypass Capacitors

0.1uF, X7R, 0603 (4 places)

V3.3 C197 C198 C199 C200

1nF, NPO, 0603 (4 places)

C223 C224 C225 C226

GND

1nF, NPO, 0603 (16 places)

C341 C342 C343 C344 C345 C346 C347 C348 C349 C350 C351 C352 C353 C354 C355 C356

GND

VCCINT Bypass Capacitors

47uF, Tantalum, Size D (8 places)

407uF, Tantalum, Size D

V1.5 C188 C189 C190 C191 C192 C193 C194 C195 C196

0.1uF, X7R, 0603 (32 places)

C227 C228 C229 C230 C231 C232 C233 C234 C235 C236 C237 C238 C239 C240 C241 C242

C265 C266 C267 C268 C269 C270 C271 C272 C273 C274 C275 C276 C277 C278 C279 C280

10nF, X7R, 0603 (16 places)

C303 C304 C305 C306 C307 C308 C309 C310 C311 C312 C313 C314 C315 C316 C317 C318

GND

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Schematic

FPGA Power

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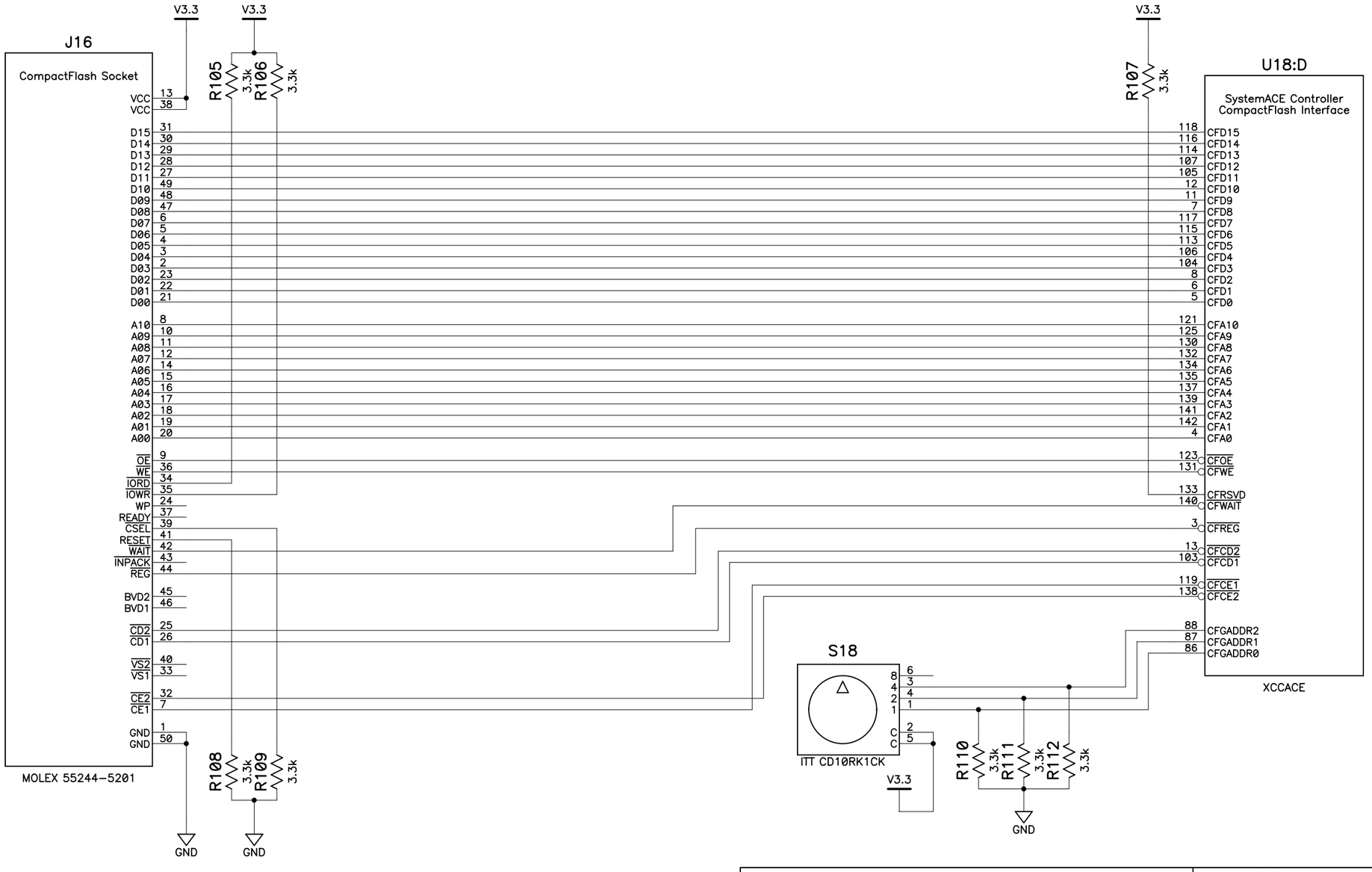

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SystemACE CompactFlash Port

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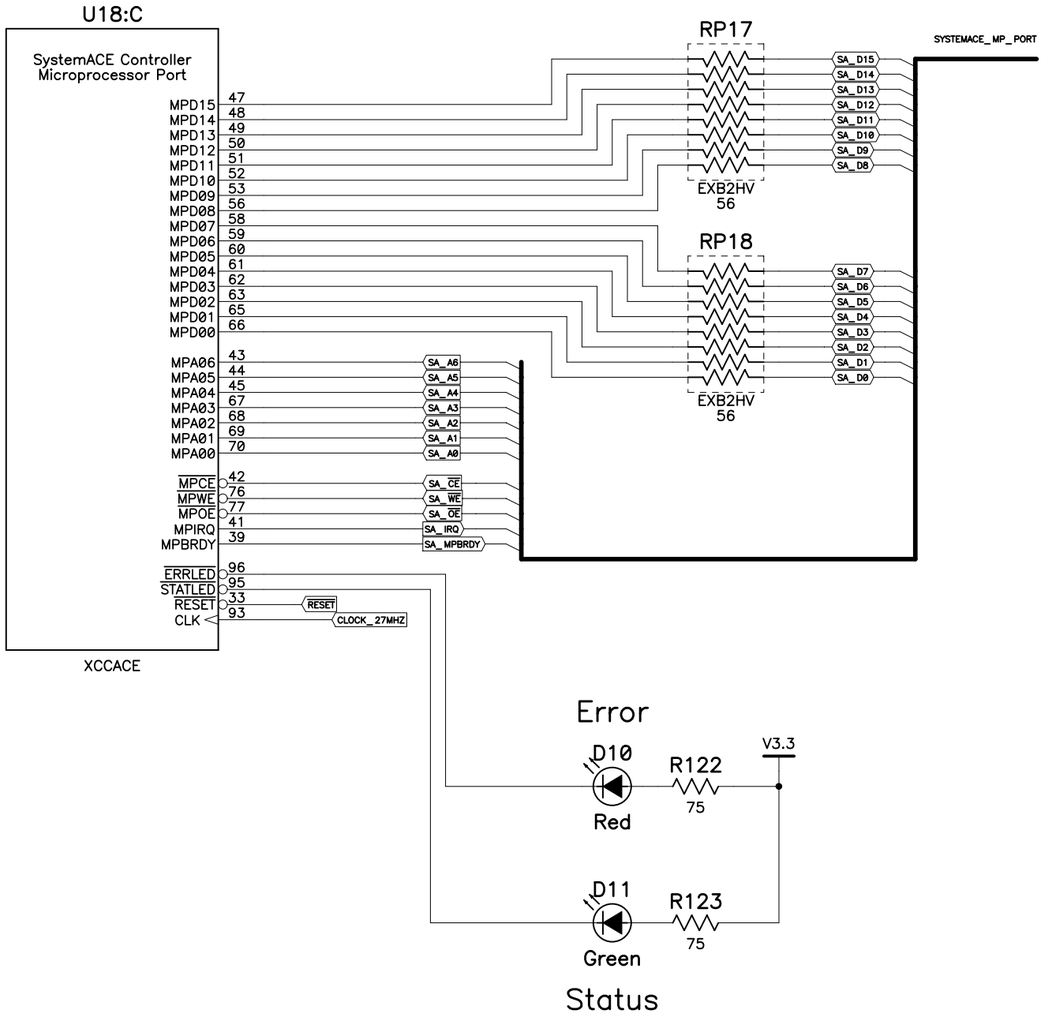

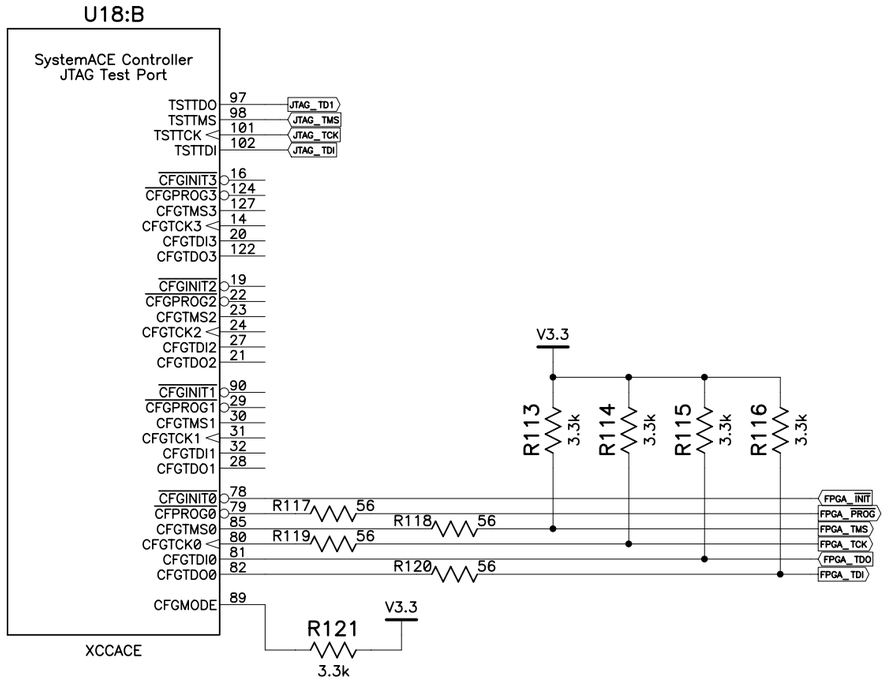

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SystemACE JTAG and MPU Ports

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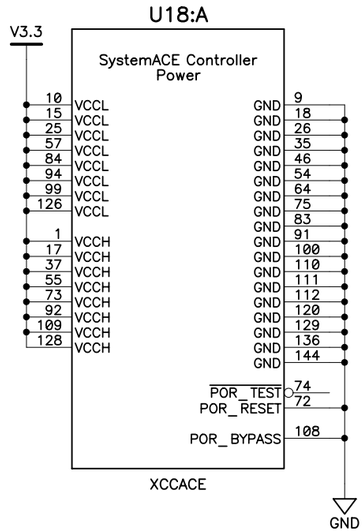

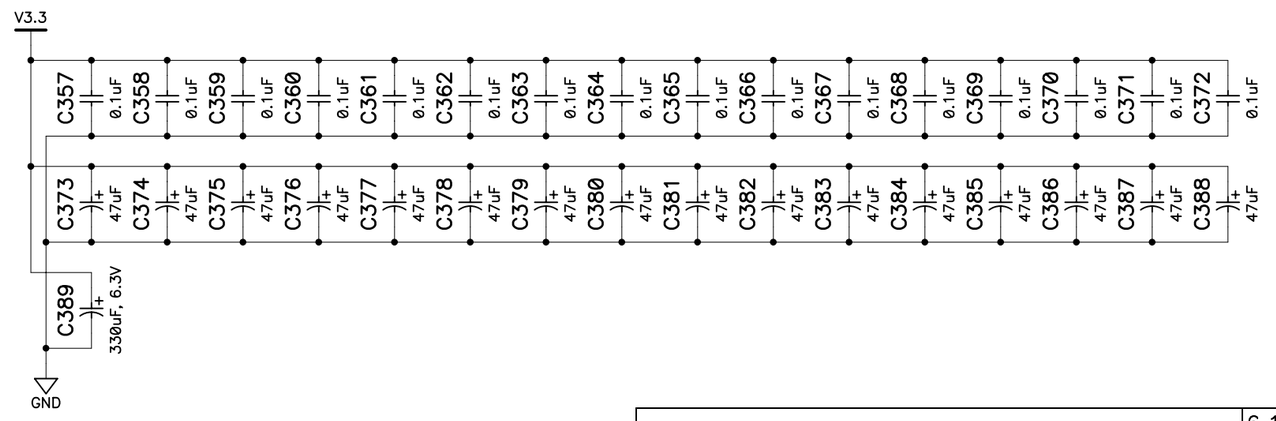

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SystemACE Power

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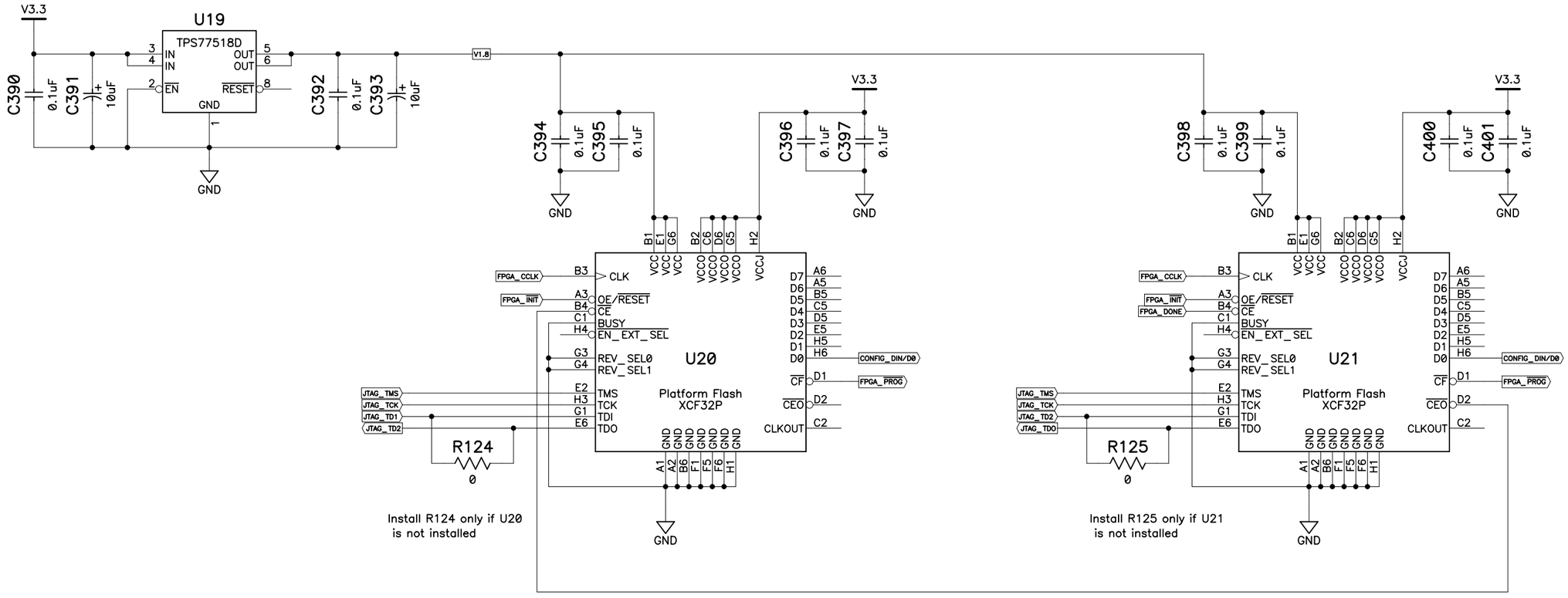

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Configuration EPROMs

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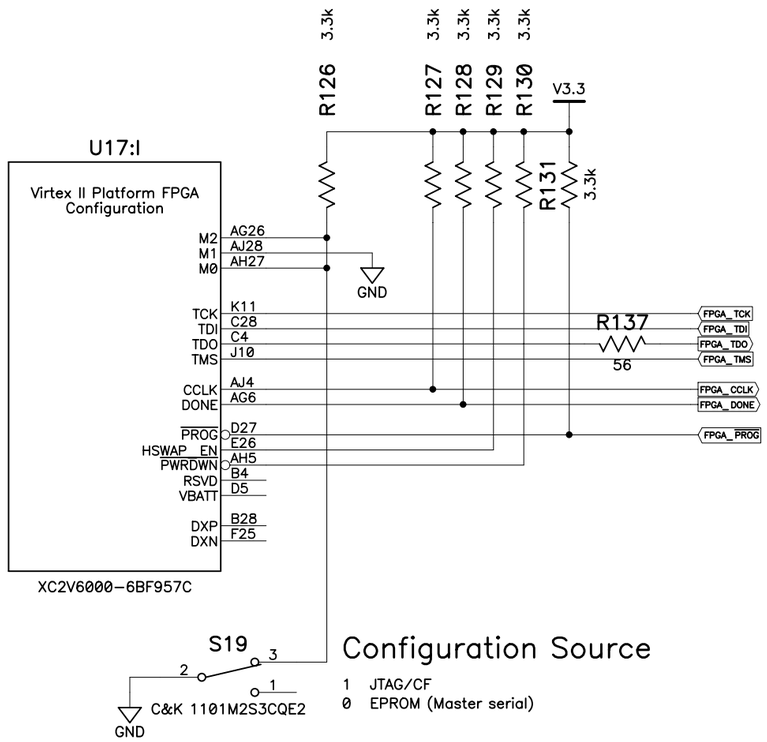

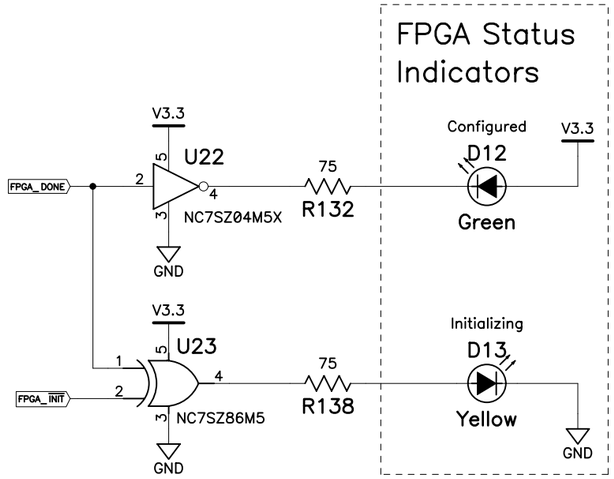

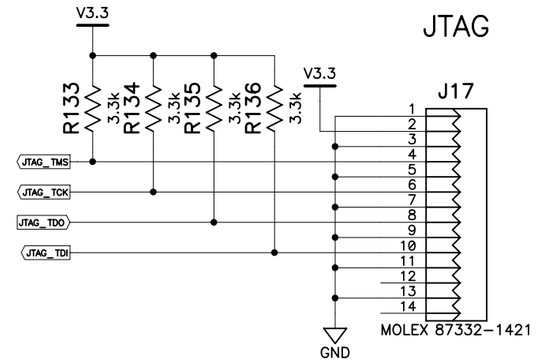

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Configuration Logic

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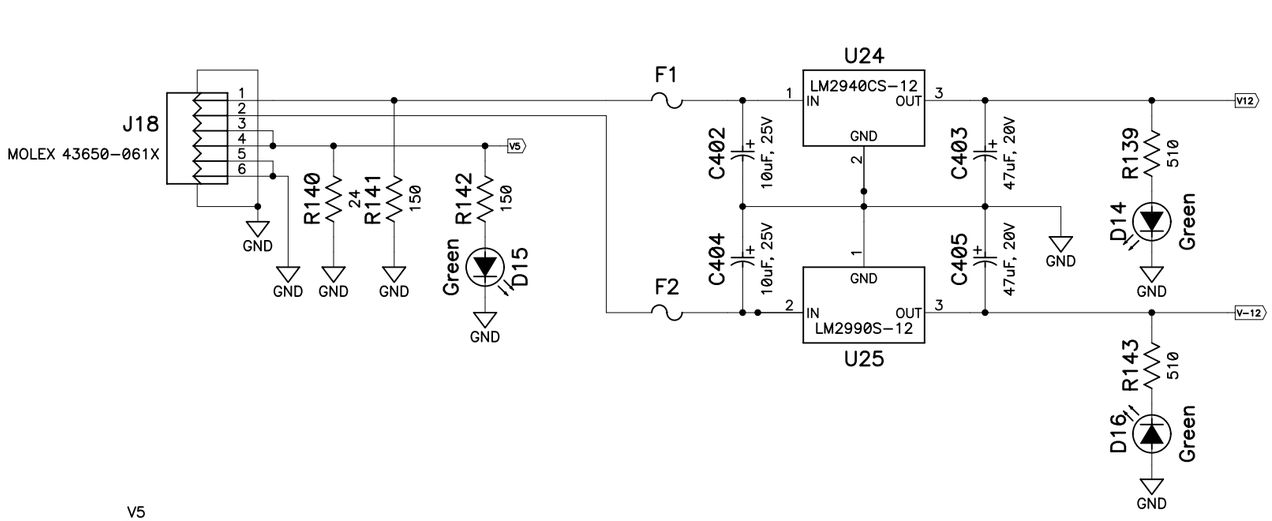

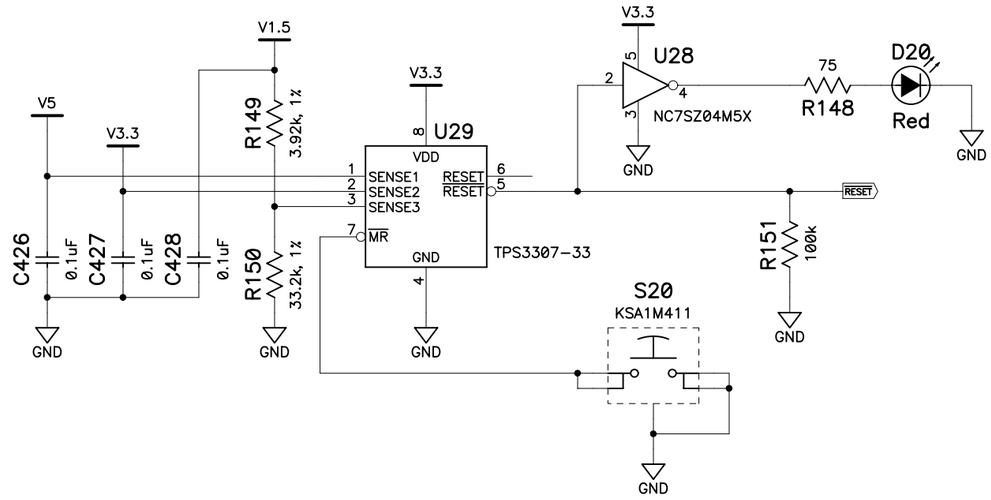

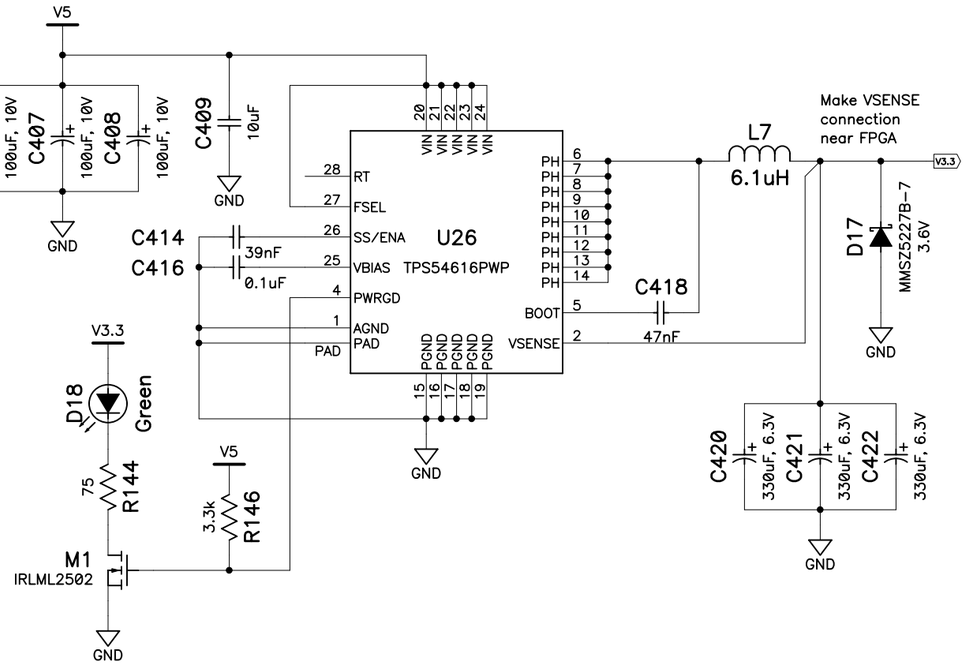

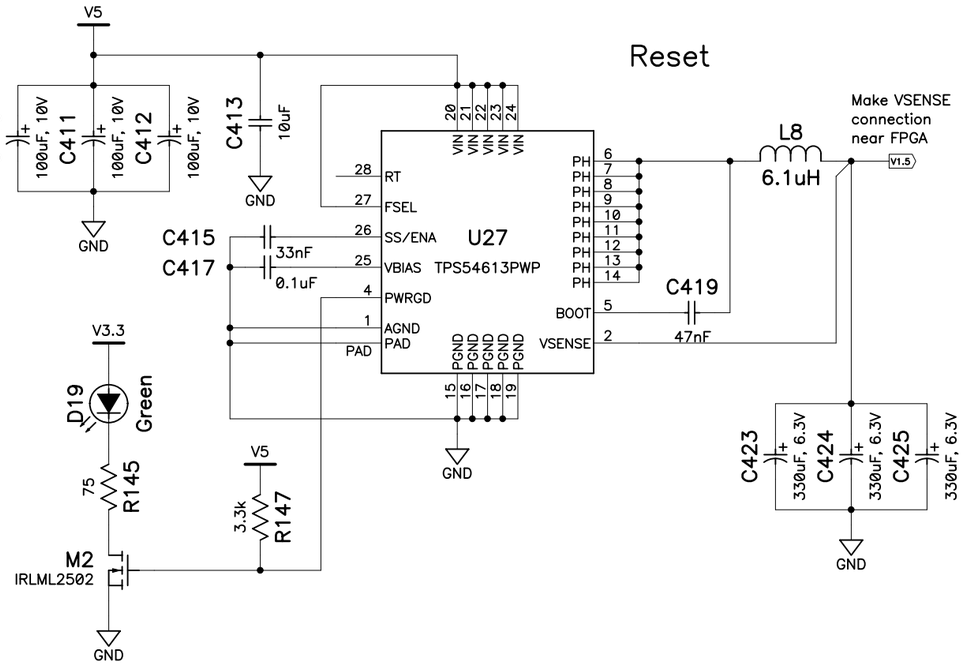

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Power Supplies

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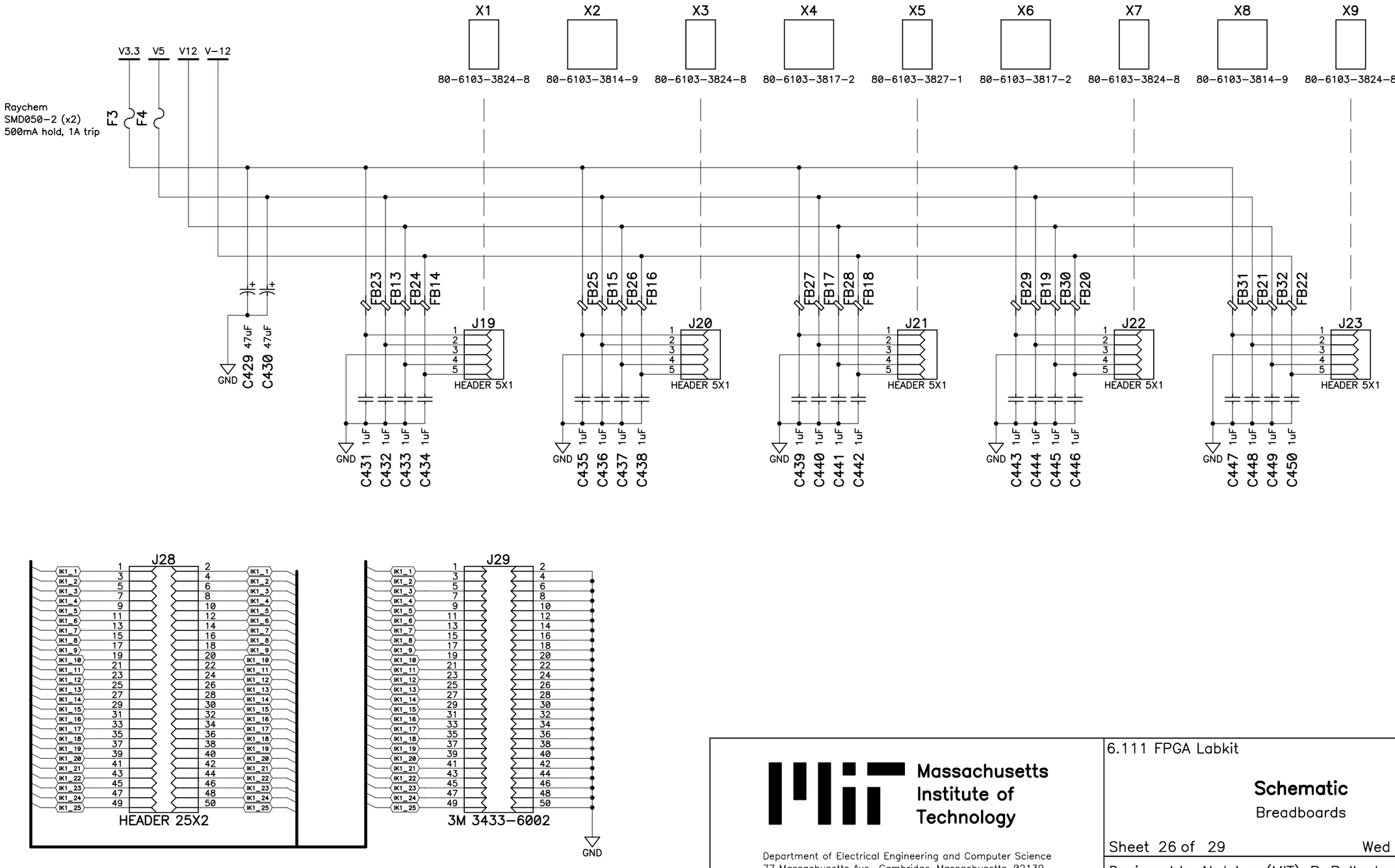

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Breadboards

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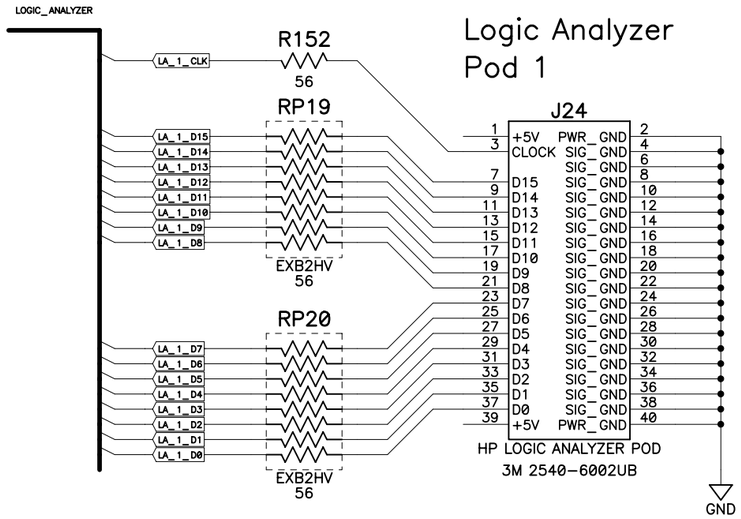

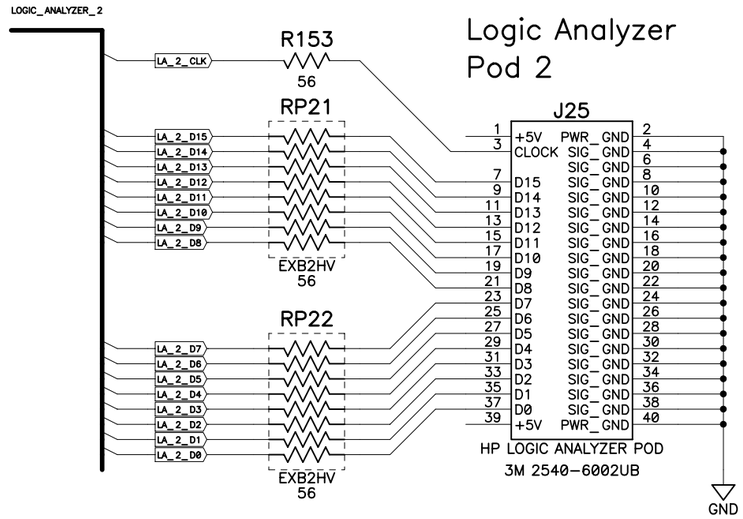

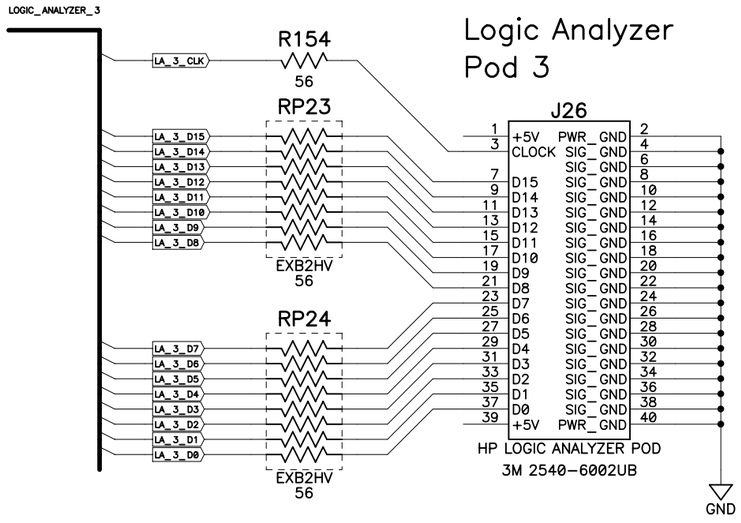

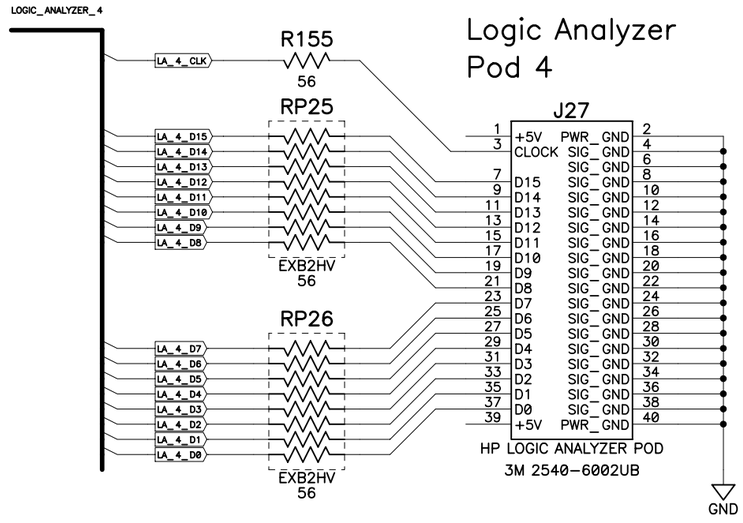

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Logic Analyzer Connectors

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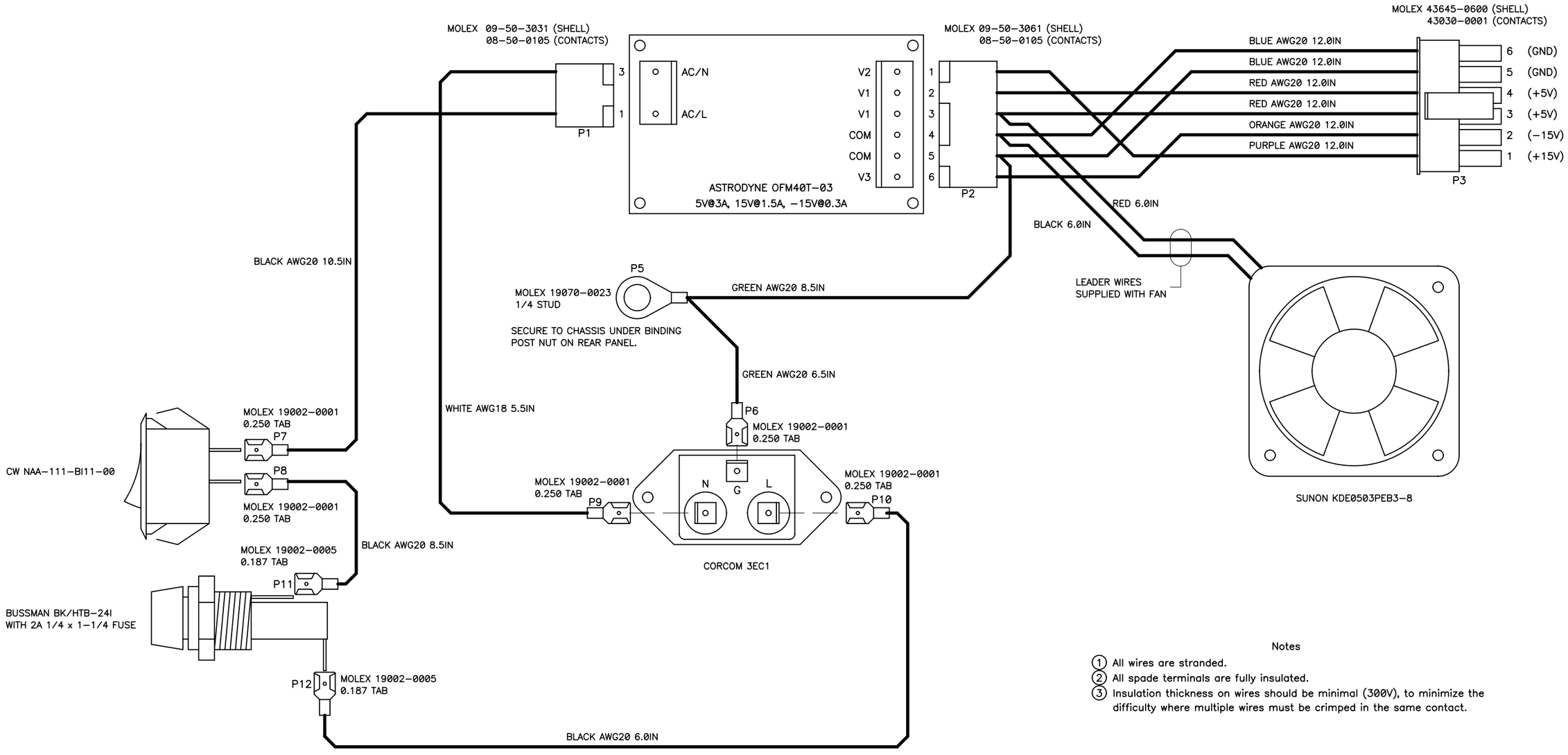

Notes

1. All wires are stranded.
2. All spade terminals are fully insulated.
3. Insulation thickness on wires should be minimal (300V), to minimize the difficulty where multiple wires must be crimped in the same contact.

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Case Wiring

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Revision History (Circles: changes in revision 002; Triangles: changes in revision 003, Sqares: changes in revision 004)

(1) Changed SystemACE clock source to built-in 27MHz oscillator
(2) Corrected "Init" LED logic.
(3) Fixed polarity of -12V bus capacitor.
(4) Added 12V linear regulators.
(5) Moved ZBT_BANK1_CLK to FPGA pin Y9, so that it does not share a I/O pair with a non-clock signal.
(6) Redesigned audio section around the LM4550 (instead of the AD1885). Removed the audio amplifier.
(7) Added pre-load resistors to +5V and +12V busses.
(8) Corrected CF configuration select switch polarity. ("Open" now means "0".)
(9) Changed pinout of FPGA configuration flash to match revised datasheet.
(10) Changed alphanumeric display part numbers to HCMS-2973. Eliminated 3.3V/5V configuration resistors. (Displays now hard-wired for 5V LED power, 3.3V logic power.)
(11) Moved UIO_1_30 to FPGA pin J14 and UIO_3_29 to J13. Added SRAM clock feedback loop.
(12) Combined power input jacks into one 6-pin jack.
(13) Moved four of the SRAM bypass capacitors to the Flash sheet.
(14) Renumbered all components.
(15) Added sheet showing off-board circuitry.
(16) Grounded CE1 and CE2 pins of flash memory. The flash chip is now enabled only by the single FLASH_$\overline{CE}$ net.
(17) Moved the SRAM clock feedback net to FPGA pins AL28 and AJ16 (GCLK7S), in order to accomodate some clock routing restrictions in the FPGA.
(18) Moved FLASH_A1 to FPGA pin AE14 to keep AH17 free. (GCLK6P is the differential pair of GCLK7S, the ram clock feedback input.)
(19) Moved RS232_RTS from FPGA pin T3 to pin R3, so that ram signals are not paired with any non-ram signals.
[20] Changed fuses to a larger package, and moved +/- 12V fuses before the regulators.
[21] All Logic analyzer pods are now wired to the FPGA, and Agilent termination networks have been removed and replaced by 56 ohm series resistors.
[22] Removed parallel termination resistors on CLOCK_27MHZ.
[23] Completely revised configuration logic, eliminating the slave serial and SelectMAP ports, and combining the ERPOM and FPGA/SystemACE JTAG chains. Added a second EPROM component, enabling the use of XCF16P parts.
[24] Removed R125 from CompactFlash interface. (This component was never installed on previous boards.)
[25] Expanded TV_IN_YCRCY bus to 20 bits.
[26] Case wiring diagram updated for new sheemetal chassis.

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Revision History

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