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Cite this: *Nanoscale Horiz.*, 2022, 7, 211

Received 21st October 2021,
Accepted 6th January 2022

DOI: 10.1039/d1nh00553g

rsc.li/nanoscale-horizons

GaAs nanowires on Si nanopillars: towards large scale, phase-engineered arrays†

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Large-scale patterning for vapor–liquid–solid growth of III–V nanowires is a challenge given the required feature size for patterning (45 to 60 nm holes). In fact, arrays are traditionally manufactured using electron-beam lithography,for which processing times increase greatly when expanding the exposure area. In order to bring nanowire arrays one step closer to the wafer-scale we take a different approach and replace patterned nanoscale holes with Si nanopillar arrays. The method is compatible with photolithography methods such as phase-shift lithography or deep ultraviolet (DUV) stepper lithography. We provide clear evidence on the advantage of using nanopillars as opposed to nanoscale holes both for the control on the growth mechanisms and for the scalability. We identify the engineering of the contact angle as the key parameter to optimize the yield. In particular, we demonstrate how nanopillar oxidation is key to stabilize the Ga catalyst droplet and engineer the contact angle. We demonstrate how the position of the triple phase line at the SiO_2/Si as opposed to the SiO_2/vacuum interface is central for a successful growth. We compare our experiments with simulations performed in surface evolver™ and observe a strong correlation. Large-scale arrays using phase-shift lithography result in a maximum local vertical yield of 67% and a global chip-scale yield of 40%. We believe that, through a greater control over key processing steps typically achieved in a semiconductor fab it is possible to push this yield to 90+% and open perspectives for deterministic nanowire phase engineering at the wafer-scale.

New concepts

This study outlines for the first time that Si nanopillars are enablers in the integration of III–Vs on silicon. In particular, the success arises from contact-angle engineering at the initial stages of growth. We add on by demonstrating the versatility of this method for NWs diameter and crystal phase engineering, which is highly desirable in solar cells and optoelectronics in general. The deterministic choice on crystal phase (hexagonal wurtzite or cubic zinc blende) is a key contribution in materials science. It allows the engineering of the band structure. It also paves the way towards obtaining other semiconductors in the uncommon hexagonal phase by epitaxially growing a shell (*e.g.* hexagonal SiGe, Ge). We also go a step further and illustrate the technological relevance of the method by implementing it with industry-relevant lithography techniques such as displacement Talbot lithography and deep-ultraviolet stepper lithography, illustrating how this method can be implemented for very large area applications (latest generation of wafers).

1 Introduction

The increasing need for performance in applications including self-driving cars, next-generation computers, hyper-efficient solar panels and quantum computers had pushed Si to the verge of its fundamental capacities. Promising candidates for many applications are III–V materials, as they exhibit valuable electronic/optoelectronic properties, which outperform Si in these domains. Yet the lattice mismatch, polarity mismatch and surface defects are prohibiting the integration of III–V thin films on Si. One way that researchers have tried to address these challenges is through nucleation and growth at the nanoscale, for example *via* nanowires (NWs). These filamentary structures also permit crystal phase engineering by controlling the formation of either wurtzite (WZ) or zinc blende (ZB) phases. They can be obtained in perfect arrays, making them promising for infrared and/or terahertz detection,[1] high-mobility transistors,[2,3] topological superconductors[4–6] or high-yield photovoltaïcs.[7–9]

Semiconductor NWs can be grown using a plethora of techniques, from top-down[10] to bottom-up vapor-phase methods.[11]

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† Electronic supplementary information (ESI) available. See DOI: 10.1039/d1nh00553g

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In this work we will solely focus on GaAs NWs grown by the vapor–liquid–solid method (VLS) in a molecular beam epitaxy (MBE) system.[12] Operating at ultra-high vacuum, MBE allows for very precise control over precursor fluxes, making it an ideal tool for fundamental studies of vapor-phase nanostructure growth on Si. MBE appears as the ideal tool for fundamental studies about vapor-phase nanostructure growths on Si.[13] We use self-catalyzed VLS, meaning the droplet catalyst is composed of Ga (and As at low concentration).[14–16] This differs from conventional VLS that uses Au or other metals as the liquid catalyst.[17] Self-catalyzed VLS avoids metal contamination in the grown material.[11]

Vertical NW arrays are a promising platform, but their fabrication comes with a twist: the most common processing methods rely on electron-beam lithography (EBL), a slow technique with processing times that increase dramatically with the exposed area, even taking several days for a single wafer.[18] The community is actively looking for alternatives, and methods like nano-imprint lithography[19,20] have been proposed, permitting the rapid fabrication of large-scale arrays using a patterned stamp and an imprinted polymer layer. Here, we propose a different approach based on the use of advanced photolithography for substrate patterning, the same technology used to pattern Si wafers for current CMOS technology.

We trade the common use of nano-patterned holes[21] for the use of SiO_2/Si pillars that, by oxidation and dimension engineering, permit to potentially obtain high-yield vertical nanostructure arrays. We showed previously how VLS contact-angle engineering on Si pillars enables vertical ⟨100⟩-oriented GaAs growth on Si.[22] In this study we first demonstrate the growth of ⟨111⟩-oriented, EBL-patterned SiO_2/Si pillars and discuss the key growth parameters. We then transfer the concept to displacement Talbot phase-shift lithography (PSL) and grow large-scale NW arrays with a higher local yield of 67% (defined as the number of vertical structure over the total number of nucleation sites). DUV-stepper lithography (DUVSL) will also be discussed as a reliable way for patterning Si (111) wafers for III–V NW growth. Finally, we also examine the possibility of phase engineering by showing both WZ and ZB NWs grown on Si pillars.

2 Electron-beam lithography

In this section, Si substrate preparation is analogous to our previous work:[22] Si pillars[23] of various diameters, ranging from 65 nm to 250 nm in diameter, are patterned by EBL using the negative resist hydrogen silsesquioxane (HSQ). We etch the pillars by a top-down method using a reactive-ion etcher (RIE) with a fluorine chemistry plasma. After an oxygen plasma and a hydrofluoric acid (HF) cleaning, a dry oxidation is performed at 900 °C for a nominal planar thickness of 50 nm. Fig. 1 summarizes the next steps for oxide etching and NW growth: after the oxidation, a polymer layer is spin-coated onto the sample. This layer is either poly methyl methacrylate (PMMA) 495 K or styrene methyl acrylate (ZEP). It is worth noting that Fig. 1b. shows the ZEP 20% wetting behavior. The meniscus effect can be experimentally observed and is visible for the reader in the ESI.† A RIE step is used to partially remove the top oxide, though 5 to 10 nm are left on top to avoid damage to the Si by the RIE plasma. A following HF 1% etching allow to uncover the Si core completely.

The sample is then loaded in the MBE for vapor-phase growth. Fig. 1e represents the Ga predeposition step that forms the liquid catalyst droplet necessary for VLS. A constant Ga flux is sent to the substrate and Ga selectively aggregates at the Si pillar core, forming a droplet. The predeposition time, *i.e.* the time during which Ga flux is on, as well as the substrate temperature,[24] determine the droplet volume. This step is crucial as the volume of the droplet is one of the determining parameters for the contact angle, defined as β, discussed later in this section. The liquid catalyst configuration was thoroughly characterized prior to NW growth by performing a predeposition-only growth with identical Ga fluxes and time.

Fig. 2a is a scanning electron microscopy (SEM) image at a 20° tilt angle of the NWs grown on 135 nm nominal diameter Si pillars with a 50 nm nominal oxidation. Fig. 2b shows the yield as a function of the pillar nominal diameter for the growth shown in a. named growth 1. It is worth noting that the nominal diameter differs from the real pillar diameter due to EBL dose/development (real size 20% smaller for sizes <100 nm diameter and 10% smaller for larger pillars until 300 nm diameter) and oxygen incorporation during oxidation (the SiO_2 volume is 2.25 times that of Si[25]). For growth 1, the set manipulator temperature was 610 °C. Predeposition time was set at 15 min with a Ga beam equivalent pressure (BEP) of 2.1×10^{-7} Torr. We subsequentially open As for a V/III ratio of 11 for 30 min. Fluxes are then stopped and the substrate is cooled down to 100 °C.

Fig. 2a gives us information about the growth mechanisms and growth selectivity; a Ga droplet is visible on top of each GaAs NW, confirming the VLS growth mechanism, and no parasitic growth is visible on the oxide mask, confirming the expected selectivity for NW arrays. Each vertical nanowire starts from a SiO_2/Si pillar, which indicates a good selectivity. NWs possess a slight inverse tapering due to a Ga droplet volume increase during growth.[24]

Fig. 2b informs us about the evolution of the vertical yield with respect to pillar diameter. The average was calculated on areas of ~ 2200 μm^2 for each value. The curve shows a global maximum value at $55 \pm 3\%$ for a nominal diameter of 135 nm. This value then decreases steadily. We can link this behaviour with the study by Matteini *et al.*[26] showing that vertical growth is initiated at an optimal β; as the entire substrate is exposed to the same Ga flux for the same amount of time, we assume the resulting droplet on top of every pillar has the same volume. After a certain volume threshold we also assume that the droplet is pinned at the SiO_2/Si pillar sidewall. Therefore we expect very large β for smaller diameters and lower β for higher diameters. In this context, the vertical yield is maximized when the diameter of the SiO_2/Si pillar permits the optimal β for vertical NW growth at the SiO_2/Si interface.

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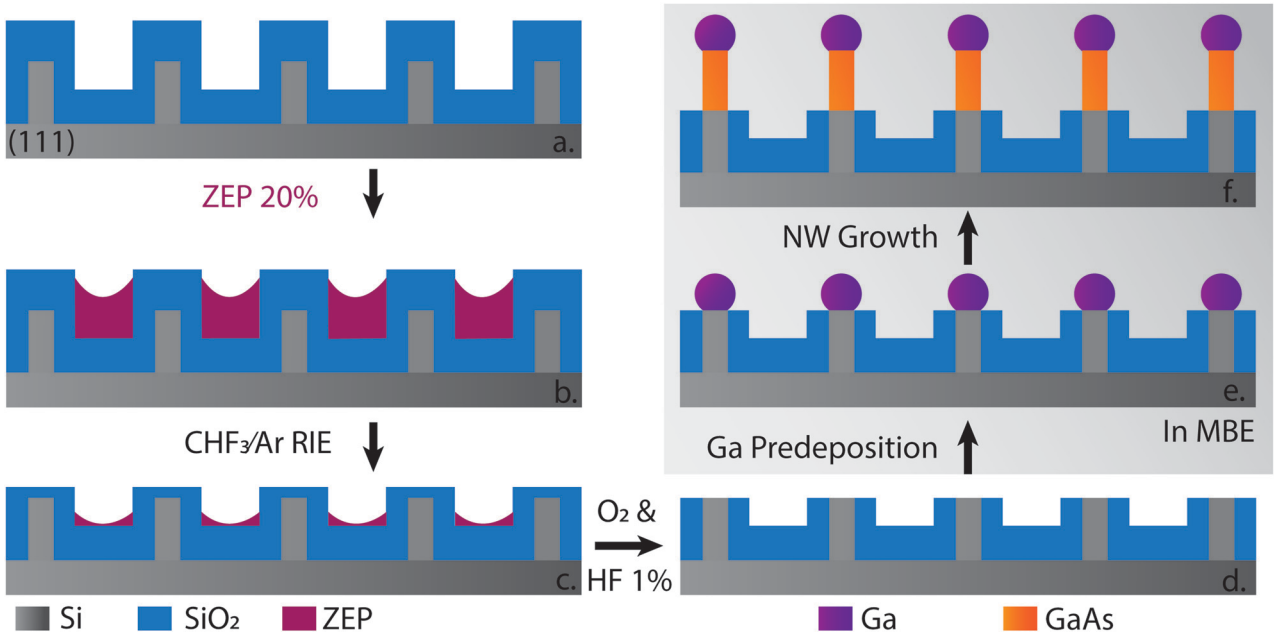

Fig. 1 Schematic detailing the fabrication steps of SiO_2/Si(111) pillars for self-catalyzed VLS GaAs NW growth. (a and b) The resist spin-coating process, (b and c) The RIE step and (c and d) the last wet etching before MBE loading. (e) Shows the very critical Ga predeposition step followed by (f) showing NW growth.

The droplet contact angle β and its configuration on the SiO_2/Si pillar is crucial for the growth. In order to study the Ga catalyst more in detail and verify our assumption, we measured droplets contact angles at various pillar diameters. Fig. 2c and d show measurements on pillars oxidized for a nominal thickness of 10 nm. Fig. 2c shows SEM images of SiO_2/Si pillar cross-sections for the same predeposition time as growth 1. SEM images used for contact angle measurements of this figure can be found in the ESI.† The SiO_2/Si pillars' nominal diameters are 65 nm, 100 nm and 135 nm. Fig. 2d shows both β (in black) and NW vertical yield (in red) as a function of the pillar nominal diameter for a second growth with the same conditions used in growth 1. The variation of β shows a linear decrease when increasing the pillar diameter. The maximum vertical yield is obtained for $\beta = 100^\circ$. This value can be compared with the one of Matteini *et al.* where the optimum β value is 94°. The difference between both values can be explained by the Ga droplet constraint; Matteini *et al.* experimented on flat SiO_2 surfaces, whereas we use SiO_2/Si pillar. The measurement method also exhibits an error of $\pm 5^\circ$.

So far, we have shown that self-catalyzed VLS growth of GaAs NWs on SiO_2/Si pillars is possible at a good yield. We drew attention to the importance of reaching $\beta = 100^\circ$ for maximizing vertical NWs. As we linked the droplet volume to a given predeposition time, we can expect a variation of the maximum vertical yield in SiO_2/Si pillar diameter by changing the predeposition time. In Fig. 3 we show the comparative results of three different growths having predeposition times of 10 min, 15 min and 20 min. The rest of the parameters are identical to growth 1. Fig. 3a shows schematics that illustrate the shift in Ga droplet volume for a given β. We observe a shift of the maximum yield to higher SiO_2/Si pillar nominal diameters by increasing the predeposition time, which corroborates the previous assumption. The SiO_2/Si pillar geometry therefore permits to choose a desired NW diameter by tuning the predeposition time, which can be attractive for applications that couple optical/acoustic/microwave modes with NWs for higher efficiencies, such as photodetectors[27] or solar cells.[8] Nevertheless we observe a decrease in the maximum yield for a predeposition time of 20 min. We explain this by the fact that all three growths share identical conditions (apart from the predeposition time) for the sake of the experiment, and a larger droplet is expected to require a higher As flux for an optimum NW growth.

Coming back to Fig. 2b and d focusing on the yield curves for 50 nm and 10 nm oxidation: comparing the yield curves for 50 nm and 10 nm oxidation in Fig. 2b and d, respectively, we observe that, for identical growth conditions, the global maximum stands at different SiO_2/Si pillar diameters. Its value also varies from 55% to 26%. We thus deduce that there is an influence of the oxide thickness on the maximum yield and optimum SiO_2/Si diameter. We develop this hypothesis in Fig. 4 by showing a comparative study of three different growths identical to growth 1, but on substrates oxidized for nominal thicknesses of 10 nm, 30 nm and 50 nm. The Ga predeposition time and flux being fixed, we assume the Ga droplet volume is identical throughout the growths. We see that we have an increase in optimum SiO_2/Si pillar diameter by increasing the oxide thickness. We link this with the fact that thicker nominal oxidations result in a reduction of the Si core.[25] The Ga droplet volume being constant, $\beta = 100^\circ$ is reached at fixed Si core diameter, *i.e.* larger SiO_2/Si nominal diameter for a higher nominal oxide thickness. This is illustrated

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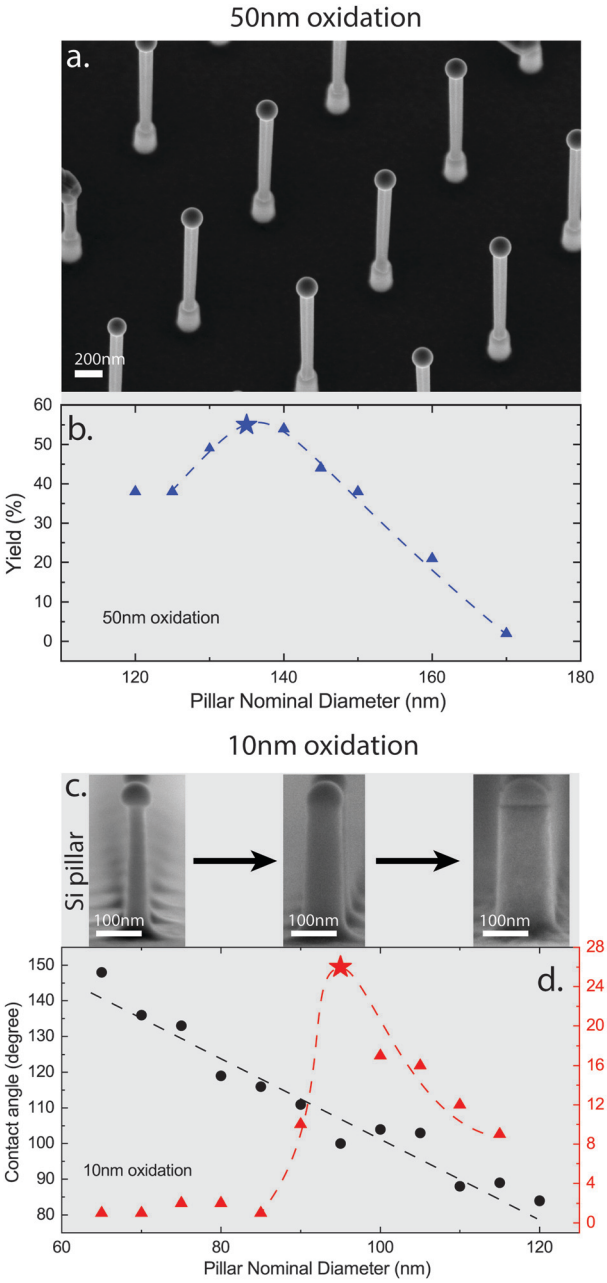

Fig. 2 Aspects and statistics of NW growths done on EBL-patterned SiO_2/Si pillars. (a) SEM image (20° tilt) showing vertical GaAs NWs grown on SiO_2/Si (111) pillars. (b) Vertical yield as a function of pillar nominal diameter. (c) SEM images showing Ga droplets on top of SiO_2/Si pillars of different nominal diameters. (d) Contact angle and yield as a function of pillar nominal diameter for pillars as shown in c. The optimum contact angle is identified as the one showing the best vertical yield.

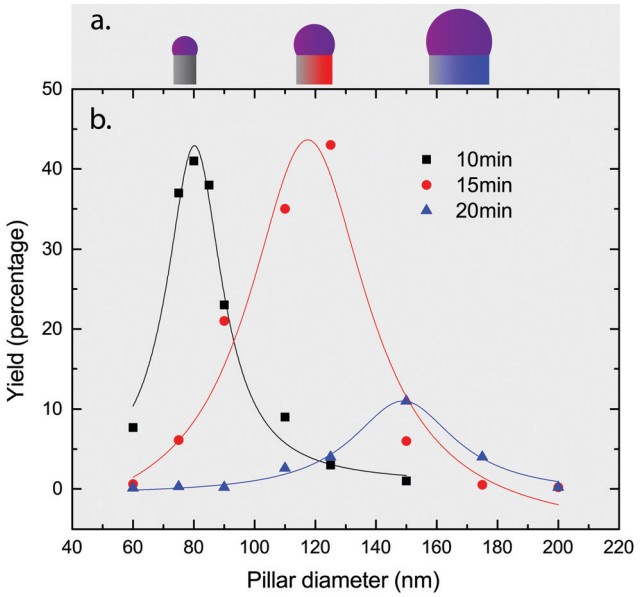

Fig. 3 (a) Schematics showing the increase in droplet volume with SiO_2/Si pillar diameter at a fixed contact angle. (b) Vertical yield as a function of SiO_2/Si pillar nominal diameter for Ga predeposition times of 10 min, 15 min and 20 min.

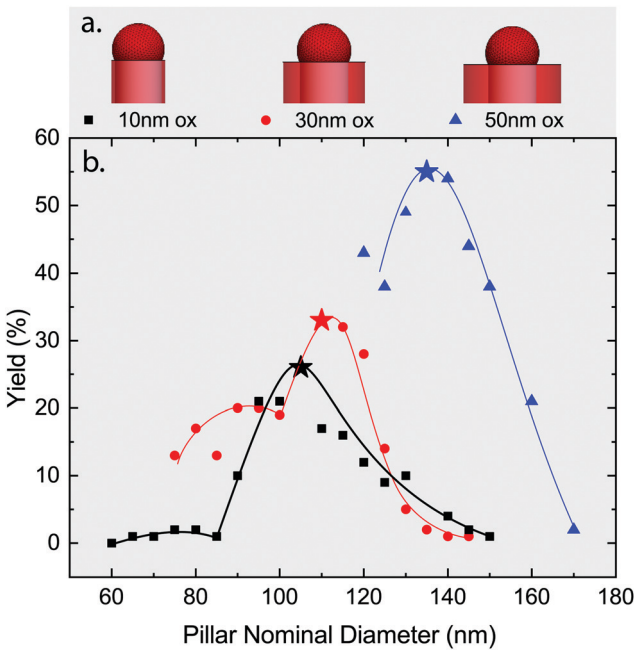

Fig. 4 (a) Schematics showing the change in SiO_2/Si pillar nominal diameter for a fixed Si core diameter and Ga dropelt volume. (b) Vertical yield as a function of the SiO_2/Si pillar nominal diameter for nominal oxidations of 10 nm, 30 nm and 50 nm.

in Fig. 4a where the Si core diameter at $\beta = 100°$ for the three different oxidations is schematically illustrated.

We now focus on the increase of maximum yield with oxidation; Fig. 4b shows that increasing the oxide thickness around the Si core permits a higher yield. We explain this by studying the location of the triple phase line (TPL), *i.e.* the line that simultaneously separates liquid Ga, solid Si and vapor phases.[28] We assume that the ideal droplet configuration for the vertical NW growth is $\beta = 100°$ with the TPL at the SiO_2/Si interface, *i.e.* the inner interface. During predeposition the droplet volume and β increase simultaneously on top of the Si core. After reaching the equilibrium β value for Si, *i.e.* 51°, the droplet pins at the SiO_2/Si interface and swells until

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reaching the equilibrium β value for SiO_2, *i.e.* 116°. Further swelling, firstly, moves the TPL away from the Si core by keeping β = 116°. Secondly, the droplet pins to the pillar side and continues swelling, increasing β to out-of-equilibrium values, as seen in Fig. 2d. We believe a thicker oxide permits to stabilize the TPL close to the Si core with β relatively close to 100°.

In order to visualize such droplet evolution, we performed simulations using the software Surface Evolver™, which permits one to study the shape of liquid surfaces under the effect of different energies and constraints. We computed the equilibrium shape of the liquid and verified the development of the surface energy of the system as a function of the droplet volume. In Fig. 5 we show six different curves of the apparent droplet angle as a function of the droplet volume for different d_{SiO_2}/d_{Si} ratios, keeping d_{Si} constant, d_{SiO_2} being the oxide thickness and d_{Si} the Si thickness on a pillar diameter. We observe three main evolution regimes: the initial steep increase for very small diameters corresponding to the swelling with the TPL at the SiO_2/Si interface. All d_{SiO_2}/d_{Si} ratios share the same curve in this regime, as d_{Si} defines the critical volume for the onset of the first pinning. The second regime is a plateau at the equilibrium β = 116° value for SiO_2. The length of this plateau depends on d_{SiO_2}/d_{Si}: the thicker the oxide, the longer the plateau. We attribute this evolution to the free increase of the droplet volume with the TPL on the SiO_2. Therefore this regime covers a larger range of volumes for a higher d_{SiO_2}/d_{Si} ratio. The third regime corresponds to the second pinning at the pillar side wall where β increases again. The simulations are in agreement with experiments, showing that thicker oxides exhibits a contact angle relatively close to 100° for a larger droplet volume window.

This study on EBL pillars permits us to understand the underlying mechanisms and critical parameters for maximizing the NW vertical yield; SiO_2/Si pillars can be larger than 130 nm if oxidized properly and the predeposition time chosen accordingly to reach an initial β = 100°. These criteria open perspectives of large-scale implementation. In fact, pillars larger than 150 nm can be produced using industrial lithography techniques like PSL or DUVSL. The next section aims at growing large-scale GaAs NW arrays on SiO_2/Si(111) pillars based on photolithographically defined patterns.

3 Photolithography

The next NW growths were performed on PSL pillars, though we present analogous arrays using DUVSL in the ESI.† PSL exposure was performed by EULITHA™ using their in-house Phable™ system, which is a displacement Tablot lithography system[29,30] permitting periodic arrays of 130 nm features. The PSL technology allows for exposures lasting few seconds and can be expanded beyond 4 inches wafers. Subsequent RIE steps for anti-reflective coating and Si etching permitted to manufacture arrays shown in Fig. 6a. Fig. 6b shows the same array after dry oxidation, nominal planar thickness 70 nm at 1050 °C. The increase in volume due to oxygen incorporation is visible, as pillars exhibit a 50 nm increase in diameter after oxidation. Fig. 6c shows a cleaved SEM cross section of the pillars used for growth, with a nominal dry oxidation thickness of 160 nm at 1050 °C. This SEM image depicts the influence of geometry on oxidation; the top, side and planar thickness exhibit different values. This is explained by the oxygen incorporation rate and strain build-up inside the SiO_2 for the pillar geometry.[31–33] On Fig. 6c three coloured arrows indicate the local planar (blue), side wall (green) and top (red) oxide thickness.

The array covers the entire 4-inch Si wafer. The potential for very large-scale NW arrays is clear and presented in Fig. 7. Fig. 7a shows a 2 cm × 2 cm chip used for the MBE growth fully covered by a 40% yield array. Local yield variations of ±10% happen between the center and the border due to edge effect during spin-coating.[34] In fact, the spin-coating and the RIE steps depicted in Fig. 1 between a and c are critical for a proper pillar uncovering and droplet configuration. Fig. 7b illustrates this by showing an SEM image of a spin-coating comet, *i.e.* an

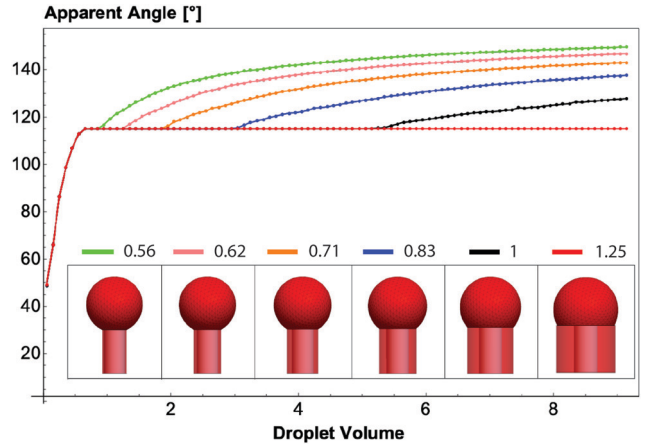

Fig. 5 Results of simulations done on Surface Evolver™. The graph shows the droplet apparent angle, *i.e.* contact angle, for d_{SiO_2}/d_{Si} ratios of 0.56, 0.62, 0.71, 0.83, 1 and 1.25.

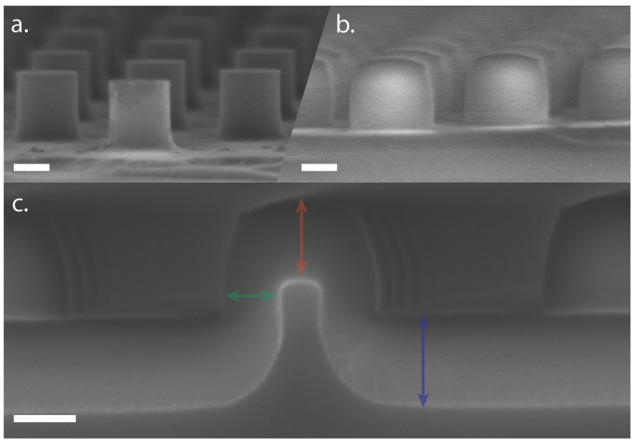

Fig. 6 SEM images showing (a) PSL-patterned Si pillars after RIE, (b) after 70 nm nominal dry oxidation and (c) a cross-section of a SiO_2/Si pillar after 160 nm dry oxidation. Scale bars are 100 nm.

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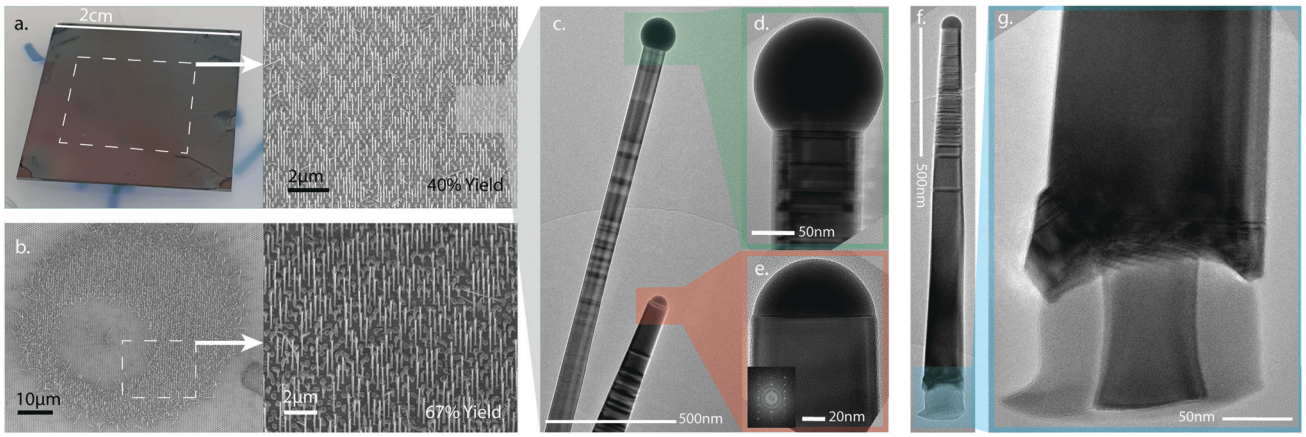

Fig. 7 Self-catalyzed VLS growth of GaAs NWs on SiO_2/Si (111) PSL pillars. (a) Large-scale array showing a 40% vertical yield. (b) Local vertical yield of 67% from a spin-coating comet. (c–e) TEM bright-field images of ZB and WZ nanowires coming from the same SiO_2/Si large-scale array. The WZ FFT is visible. (f and g) WZ GaAs NW and the SiO_2/Si pillar where it grew from. The pillar's Si core and SiO_2 shell are visible.

irregularity in the spin-coated thickness due to an impurity, that locally exhibits a 67% yield whereas the rest of the chip did not give any growth. We believe this unveils the last key parameter in order to obtain 90+% yield arrays: the top SiO_2/Si interface. If we over-etch, the droplet becomes unstable and does not grow into a NW. If we under-etch, Si is still covered by SiO_2 which prevents growth completely. If the spin-coated polymer does not protect the SiO_2 side-walls properly, RIE alters the shape of the pillar and impairs droplet stability. We believe that spin-coating a layer thicker than the pillar's height, planarizing it and controlling precisely the RIE are the key elements to obtain yields comparable to hole-based arrays.[35,36]

We now focus on the transmission electron microscopy (TEM) measurements presented in Fig. 7. Fig. 7c–g show the presence of ZB and WZ NWs simultaneously from the same growth. Whereas this was observed in the past from self-assembled growths,[15] it was mainly through stochastic events and did not open perspectives for precise phase engineering. Many studies point out the correlation between droplet contact angle and NW crystal phase.[28,37,38] Thanks to contact angle engineering from SiO_2/Si pillar diameter and predeposition time tuning, the pillar geometry potentially permits to obtain either WZ NWs, ZB NWs or both at patterned locations in a deterministic way.

Fig. 7d shows a ZB GaAs NW with its characteristic Ga droplet configuration, *i.e.* $>130^\circ$ contact angle.[37] We can also observe the presence of stacking faults that are frequently observed in ⟨111⟩ B NWs.[39] Fig. 7e shows a WZ GaAs NW with the image's fast-Fourier transform (FFT) confirming its phase.[15] Fig. 7f and g show the interface between a WZ NW and the SiO_2/Si pillar from which it grew. The NW starts from the pillar sidewalls, which we believe is the reason for its WZ phase. In fact, as the Ga droplet un-pins from the SiO_2/Si inner interface and pins to the outer SiO_2 side-wall, for a given volume, the contact angle decreases drastically. This decreased contact angle appears nearly ideal for WZ NW growth, triggering pure WZ NWs. We even observed a short growth on 10 nm dry oxide SiO_2/Si pillars where all the vertical NWs appear to be WZ, based on the morphology of the NW and the droplet configuration. This can be seen in the ESI.†

We have highlighted the advantage of using Si nanopillars as opposed to nanoscale holes for the successful integration of GaAs on Si. Our results highlight the importance of controlling the wetting behavior both in terms of contact angle and to position the triple phase line. In particular, we highlight the importance of the triple phase line located at the SiO_2/Si interface as opposed to SiO_2/vacuum or Si/vacuum. Nanopillars are an ideal platform to achieve such exquisite degree of control as well as large scalability on the silicon platform.

As these NWs appear to possess many similarities with NWs grown in nanohole arrays, for example the stacking fault density or Si/GaAs interface, we believe a more in-depth study of the impact of SiO_2/Si pillars patterning on NWs crystal quality, doping and nucleation could be of interest. Methods such as In-situ TEM,[40,41] cathodoluminescence and photoluminescence[42–45] can shine light on these NWs nucleation mechanism and internal defect concentration.

4 Conclusion

In conclusion, we have highlighted the central importance of the Ga droplet contact angle and position of the triple phase line for reaching high vertical yield of GaAs nanowires, as well as also for crystal phase-selection. The SiO_2/Si pillar geometry constitutes an ideal platform, allowing a precise and deterministic contact angle engineering and at the same time opening perspectives for reliable large-area patterning and freedom in design. This work brings NW arrays one step closer to large-scale implementation for devices.

Methods/experimental

For EBL pillars: a 2 min 600 W O_2 plasma in a TEPLATM GigaBatch is done on a 100 mm Si wafer for surface activation before spin coating with Dow Corning HSQ 006 and EBL

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exposure with a Vistec™ EBPG5000ES system. The dose used is 2740 μC cm^{-2} for all the pillar's diameters. The wafer is then developed using a commercial solution of MicropositR MFR CD26 for 2 minutes, and rinsed sequentially with water, acetone and propan-2-ol. A 2 min 600 W O_2 plasma in a TEPLATM GigaBatch is done for further cross-linking the HSQ.

For PSL pillars: after exposure at EULITHA™ using the PHABLE™ system, samples were shipped to EPFL for further processing. Sample is introduced in an SPTS APS plasma etcher where a plasma of CHF_3/O_2 of 20 s is done for anti-reflective coating etching.

The wafer, EBL or PSL, is then introduced in an AlcatelTM AMS200 DSE reactive ion etcher, where a customized recipe using SF_6 and C_4F_8 is used for creating the pillars. A buffered hydrofluoric acid (7 : 1) bath is then used for 2 minutes to remove any trace of resist. A thermal oxidation is then done at 1050 °C for a variable amount of time depending on the desired oxide thickness. The nominal oxide thickness mentioned throughout this study corresponds to the planar thickness obtained for a nominal oxidation time. After the oxide growth, a 50 nm Styrene Methyl Acrylate based resist (ZEP) film is spin coated and heated for 2 min at 180 °C for polymerization. Alternatively, a 170 nm thick poly methyl methacrylate (PMMA) can be used. The sample is inserted in an OxfordTM Plasmalab system 80 PLUS using a mixture of SF_6 and CHF_3 at 100 W plasma power for 40 seconds to uncover the pillars. 10 min of O_2 plasma permits to remove the resist, and a last cleaning involving a 5 min acetone bath, a 2 min propan-2-ol bath and a 35 s HF bath at 1% concentration makes the sample ready for growth.

The growths are conducted in a DCATM MBE chamber under a Ga BEP (beam equivalent pressure) of 0.21×10^{-6} Torr and an As BEP of 2.2×10^{-6} Torr for 45 minutes. The samples were characterized by SEM using a ZeissTM Merlin. NWs were transferred flat onto TEM copper grids and observed using an FEI Talos™ microscope for BF and HR images. The reported MBE growth temperatures are estimations of the substrate temperature. With measurements done with an infrared camera on known standard GaAs samples, we estimate a difference of 130 °C between the set PID and the real temperature.

Author contributions

Lucas G. took part in conceptualization, data curation, formal analysis, investigation, methodology, visualization, resources and writing. Lea G. took part in data curation, formal analysis, investigation, methodology and visualization. L. W., C. D. and H. S. took part in resources. N. M., D. D., J. B. L. and W. K. took part in methodology. A. B. took part in conceptualization, investigation, methodology and resources. R. M. took part in conceptualization, resources and validation. C. C. took part in conceptualization, supervision and validation. A. F. M. took part in conceptualization, funding acquisition, supervision, project administration and validation.

Conflicts of interest

There are no conflicts to declare.

Acknowledgements

L. G. thanks all the MBE team, but also the CMi staff at EPFL without whom none of this study could be possible. LG thanks EULITHA for the precious help in exposing the (111) Si wafers. We thank the SNF and QSIT for funding the project (projects 200021_169908 et IZLRZ2_163861).

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