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Gate-Tunable Hole Transport in In-Plane Ge Nanowires by V-Groove Confined Selective Epitaxy

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Germanium (Ge) nanowires hold great promise as building blocks for hole spin-based quantum processors. Realizing this potential requires their direct integration onto silicon (Si) wafers. This work introduces V-groove-confined selective epitaxy to enable the in-plane growth of nanowires on Si substrates. Nanowires form fully confined within V-shaped grooves, a process driven by surface energy minimization and in agreement with Winterbottom-like construction calculations. This confinement eliminates the direct Ge–SiO_2 interface, reducing spurring charge noise and enhancing nanowire functionality. Aberration-corrected scanning transmission electron microscopy reveals the cross-sectional shape and single-crystalline nature of the nanowires. Low-temperature magnetotransport measurements on Ge nanowire Hall bars demonstrate gate-tunable hole densities and a peak mobility of approximately 600 $cm^2 V^{-1}s^{-1}$ at a density of 1.2×10^{13} cm^{-2}. These findings establish V-groove-confined epitaxy as a scalable pathway for the integration of high-performance Ge nanowire-based quantum devices.

1. Introduction

Semiconductor nanowires offer a versatile platform for exploring a wide range of quantum phenomena, thanks to the precise control achievable over their diameter, composition, morphology, and electronic properties.[1,2] Their one-dimensional structure inherently confines charge carriers, giving rise to quantum effects such as ballistic transport, quantized conductance, and Coulomb blockade.[3–5] These unique properties make nanowires composed of III-V,[6–8] Group IV,[9–11] and IV-VI[12,13] semiconductors highly promising for applications in superconducting[14–16] and spin-based[11,17–19] quantum computing.

Among these materials, Ge nanowires are particularly attractive for realizing hole-spin-based quantum logic.[11] Hole-spin qubits in Ge benefit from a strong and tunable spin-orbit interaction (SOI),[20,21] which enables fast qubit operations.[22,23] Additionally, the low natural abundance of nuclear spins in Ge,[24,25] along with the low susceptibility of holes to hyperfine noise, supports long coherence times.[26] A unique advantage of bottom-up grown nanowires is the precise control achievable over the shape and crystallographic orientation, which can be used to tune

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SOI[20] and further suppress the effects of charge noise[27,28] and hyperfine noise.[29] These distinctive properties have enabled the demonstration of ultrafast, electrically controlled hole-spin qubits in Ge nanowire systems.[22,23]

Despite these advances, the scalability of nanowire-based devices remains a major challenge. Previous studies on Ge nanowire-based hole spin qubits have utilized free-standing Ge/Si core/shell structures[9,30] or self-assembled Ge hut wires,[31–33] which offer limited control over shape and crystallographic orientation. Given the SOI in Ge nanowires depend strongly on their orientation relative to the substrate,[28,34] flexibility in both substrate selection and nanowire orientation is crucial for effectively exploring the properties of holes in these systems.

Selective area epitaxy (SAE) offers a scalable and reliable solution for achieving in-plane nanowires (also referred to as horizontal nanowires in other studies) directly on device substrates with great control over their orientation and shape.[35–38] In SAE, nanowire growth is confined to nanoscale openings on a crystalline substrate covered by an amorphous mask layer. The openings are created by uncovering regions of the underlying crystalline substrate. Under optimized growth conditions–such as controlled temperature and growth rates–nanowire growth proceeds analogously to 2D growth within these openings.[39,40] The resulting cross-sectional shape is determined by surface energy minimization and growth kinetics.[41,42] To date, multiple research efforts have validated the effectiveness of SAE in growing high-quality nanowires and their networks across III-V ,[43–45] Group IV,[10,39] and IV-VI[46–48] materials.

In our previous works, we have successfully demonstrated the SAE of in-plane Ge nanowires with orientation-dependent control of cross-sectional morphologies. The nanowires also exhibited phase-coherent hole transport and a weak antilocalization peak, indicating a strong SOI.[10] However, the direct interface between the Ge nanowire and the SiO_2 dielectric mask remains a serious limitation. The Ge-SiO_2 interface is a major source of disorder and can significantly compromise nanowire functionality for spin qubit application.[49]

This work demonstrates a novel SAE approach for growing in-plane Ge nanowires within an oxidized Si nanopillar featuring a V-groove opening. Unlike conventional SAE, the Ge nanowire growth is confined within the V-groove, eliminating the Ge-SiO_2 interface and reducing disorder. Ge nanowire growth proceeds through island nucleation and coalescence. A Winterbottom-like construction reveals that the coalescence process is driven by surface energy minimization. Additionally, we present a detailed analysis of the resulting Ge nanowire's structural and electronic transport properties and provide ways to improve them. This observed behavior is fundamental and applicable to other material systems, potentially expanding the scope of SAE-grown nanowires in applications in quantum technologies, photonics, sensing, and electronics.

2. Experimental Procedure

Figure 1a–f presents a simplified schematic of the substrate fabrication process. The process begins with the reactive ion etching (RIE) of an array of Si nanopillars on a 4-inch Si (001) wafer (Figure 1a) with a resistivity exceeding 10 000 Ω cm at room temperature using a mixture of SF_6 and C_4F_8, as described in previous works.[50,51] The use of a highly resistive substrate is to avoid parasitic electronic transport in our experiments. The Si nanopillars are rectangular, with the long axis oriented along the <110> crystallographic direction. These pillars range in length from 2 to 10 µm, with widths between 120 and 200 nm. Subsequently, the nanopillars are thermally oxidized at 900 °C to form a conformal SiO_2 layer with a nominal thickness of 50 nm (Figure 1b). The oxide layer serves as both a selective mask and a means to control the effective width of the Si nanopillar. Next, RIE with CF_4 and SF_6 chemistry selectively exposes the top sections of the Si nanopillar (Figure 1(c–e)). Finally, wet etching in a 40% KOH solution exposes atomically sharp, inclined Si {111} sidewalls forming V-grooves (Figure 1f). Additional details on the substrate fabrication process are provided in the Supporting Information.

Figure 1g shows a top-view scanning electron microscopy (SEM) image of a typical Si nanopillar structure featuring a V-groove used in this study. The image is taken from an array of 10 Si nanopillars with a pitch spacing of 1 µm. The bright contrast in the SEM indicates the SiO_2 mask surrounding a 60 nm wide groove opening. The V-shaped structure of the groove is further visible in the atomic force microscopy (AFM) 3D surface plot shown in Figure 1h.

Following a brief etching in a dilute HF solution (1:100 with H_2O), the patterned substrates are loaded into an Aixtron 200 MOVPE system for SAE of Ge. Prior to nanowire growth, the substrates are deoxidized under an arsine (AsH_3) atmosphere at 820 °C, as described in previous work.[10,39] Ge nanowire growth is carried out at 750 °C, using isobutyl germane as the Ge precursor and nitrogen as the carrier gas. Growth time varies from 5 to 110 s to obtain the temporal evolution of Ge nanowires within the V-groove. Additional details on the growth parameters are provided in the Supporting Information.

3. Results and Discussion

We start by revealing the temporal evolution of Ge nanowire formation using SEM and AFM. A detailed description of the nanowire growth evolution is shown in **Figure** 2. Figure 2a provides representative top-view SEM images at various growth times, ranging from 5 to 75 s. An overview SEM image of the entire array is included in the Supporting Information (Figures S3 and S4). To gain further insights into the time evolution of the morphological features, AFM scans are acquired from the top surface of the time-evolution samples shown in Figure 2a. The AFM measurements are acquired in tapping mode from a scan area of 500 nm × 250 nm. More details on the AFM measurements and data processing are provided in Supporting Information. The 3D surface plots resulting from these AFM measurements, along with the corresponding AFM line profile of the nanowire cross-section, are displayed in Figure 2c,b, respectively. The AFM line profiles represent averaged measurements along the scan length of 500 nm compiled from three nanowires, with error bands indicating variations in the height profile. The zero height is set to SiO_2 mask interface. The reported variation in the height profile includes the variation in the nanowire's surface topography and also the roughness in the SiO_2 mask layer.

SEM and AFM images captured after 5 s of growth reveal that the SAE of Ge nanowires inside Si V-grooves begins with the nucleation of multiple Ge islands. These islands primarily

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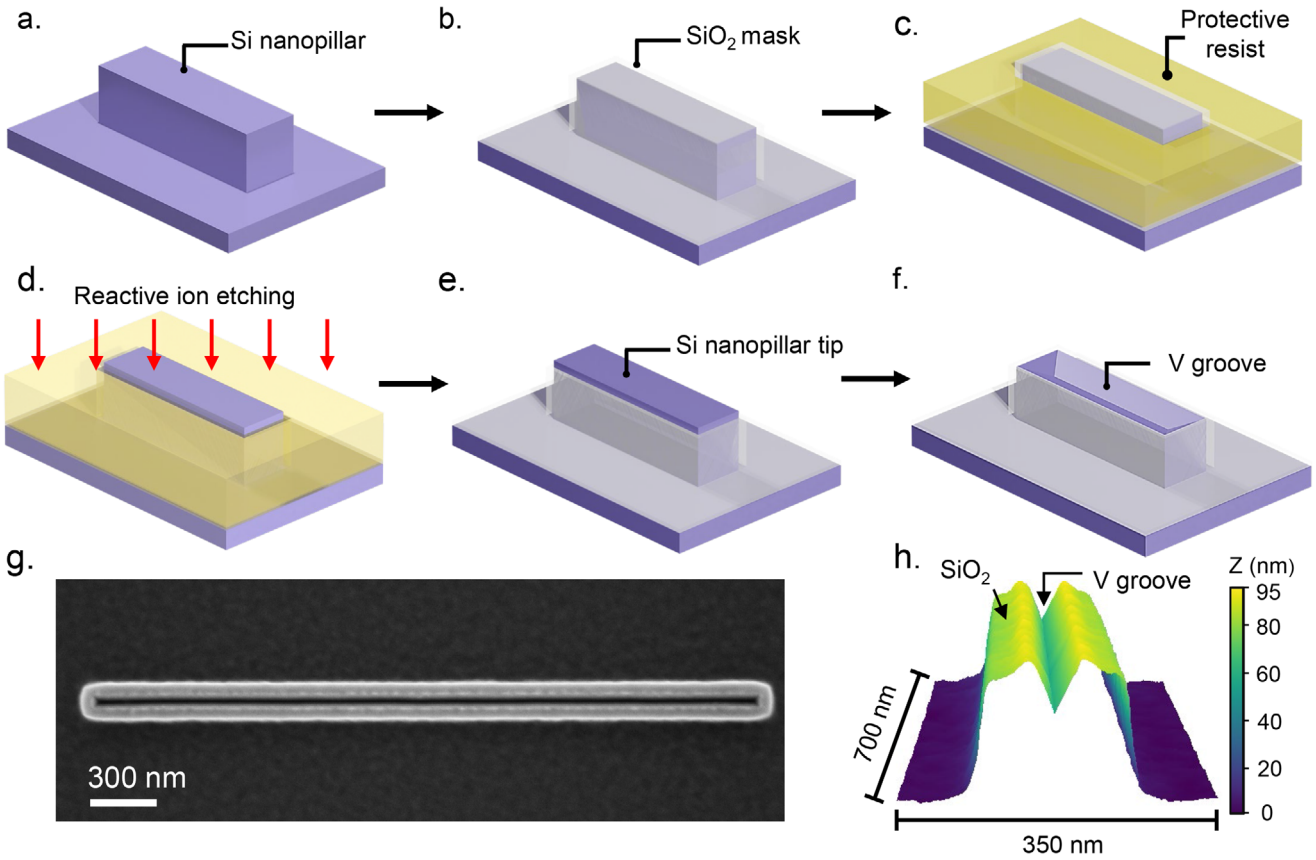

Figure 1. Schematic of the growth substrate fabrication process. a) Top-down fabrication of rectangular-shaped Si nanopillars with the long axis oriented along the [110] crystallographic direction. b) Thermal oxidation at 900 °C forms a conformal SiO_2 dielectric mask on the Si nanopillars. c) A polymeric protective layer is deposited via spin-coating. d) RIE is performed to expose the top surfaces of the Si nanopillars. e) The resist layer is removed. f) Wet chemical etching in 40% KOH solution creates V-shaped openings. g) SEM image and h) AFM 3D surface plot of a single Si nanopillar structure featuring a V-shaped opening. The observed surface roughness in the SiO_2 mask is introduced during the RIE step.

nucleate along the inclined Si {111} surfaces of the V-grooves, though some also appear at the bottom of the groove. We attribute the 3D island nucleation to the Stranski–Krastanov (SK) growth mode of Ge on the Si surface.[52,53] The formation of SK islands has similarly been reported during the SAE of Ge on planar surfaces,[39] micrometer-sized Si pillars,[54] and during Ge growth on Si nanowires.[55] As growth continues, these islands expand and coalesce with neighboring islands. The coalescence of islands from opposite faces of the V-groove leads to the formation of "bridge-like" structures between the two Si {111} surfaces, as observed after 15 s of growth in Figure 2a,c. From this point, the growth evolution of Ge nanowires remains confined to the two inclined Si {111} surfaces, a phenomenon we describe as "confined selective epitaxy."

As material deposition continues, the Si V-groove fills further, initially forming a discontinuous Ge film with a flat top surface, as observed in the AFM measurements after 30 s of growth (Figure 2b,c). The filling process progresses through the coalescence of existing islands and the lateral expansion of bridge-like structures. Finally, the complete coalescence of the Ge nanowire is observed around 60 s into growth. At this point, the Ge nanowire also develops inclined facets, as revealed by the AFM line profiles (Figure 2b).

Based on the AFM data presented in Figure 2b,c, we can infer that the entire coalescence process, from island nucleation to a continuous nanowire, remains confined by the inclined Si {111} surfaces (Figure 2b). The outward growth of the nanowire above the mask level only begins after forming a continuous wire inside the V-groove. The nucleation and coalescence of islands to form a continuous nanowire have been previously reported in the literature.[39,44,46,48,56] However, prior studies on this process have mainly focused on SAE within rectangular SiO_2 trenches. In those cases, the nucleation occurs on a planar surface, and the coalescence process is confined by the SiO_2 mask. To the best of our knowledge, no work has been reported on the coalescence process when confined by V-groove Si surfaces. Therefore, we shift our attention to understanding the differences in nucleation and coalescence processes observed in Figure 2.

The shape of Ge islands at different stages of growth gives insights into the coalescence process. Observing how the island's shape evolves provides insights into the effects of geometric confinement and growth parameters. To investigate this, we prepared focused ion beam (FIB) cross-sections perpendicular to the in-plane orientation of the nanopillar and examined them using an aberration-corrected scanning transmission

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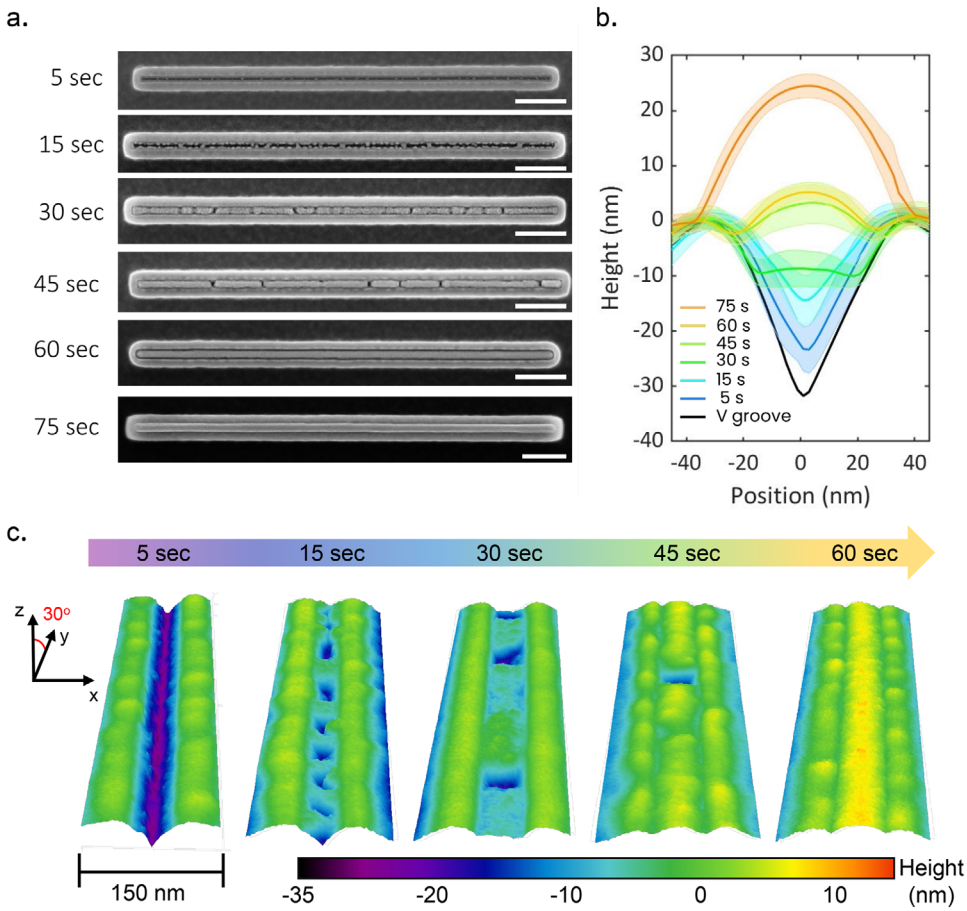

Figure 2. Temporal evolution of Ge nanowire growth. a) Top-view SEM images of Ge nanowires at different stages of growth from 5 to 75 s. The scale bar represents 300 nm. b) AFM line profile acquired from the nanowires shown in (a), illustrating the shape evolution of the Ge nanowires as a function of time. The line profiles represent the average height profile compiled from three nanowires. c) AFM 3D surface plots showing the nucleation and coalescence of Ge nanowires inside the V-groove.

electron microscope (Cs-STEM). Facets defining the nanowire cross-section were indexed by measuring their relative orientation with the Si (001) substrates. The results are presented in **Figure 3**. The FIB cross-sections were prepared from an array of Si nanopillars with nominal widths of 200 nm (Figure 3a), 150 nm (Figure 3b), and 120 nm (Figure 3c), after 60 s of growth. Since larger V-groove openings require more material to fill, the presented cross-sections represent Ge islands at different stages of growth.

Figure 3a reveals the shape of a Ge island at the nucleation stage, where the cross-sectional shape is defined by facets belonging to {111}, {110}, and {113} family. Figure 3b presents the cross-sectional morphology of a Ge island fully confined within the V-groove, defined by inclined {111} facets and a flat {001} facet, which is consistent with the AFM line profiles. Finally, Figure 3c depicts the stage where the Ge nanowire begins to grow upward from the V-groove, with the cross-sectional shape characterized by vertical {110} facets, inclined {111} and {113} facets, and a flat top {001} facet. The complete set of cross-sectional morphologies for all observed nanowires is provided in the Supporting Information (Figure S7). However, the Cs-STEM micrographs only provide information about the facets determined by the projected shape of the islands and no direct information on their 3D shape.

From a thermodynamic perspective, the equilibrium crystal shape (ECS) is the one that minimizes total surface energy for a fixed volume. The shape of an isolated particle–and, therefore, its facets—is determined by the Gibbs–Curie–Wulff theorem.[57–59] The Winterbottom construction provides a method to determine the equilibrium shape of a crystal in contact with a substrate—it is equivalent to including an additional surface energy (γ_{cs}-γ_{sv}) with a normal matching the substrate.[60] We will use the Winterbottom construction to gain insights into the 3D morphology of Ge nanowires at different stages of growth.

The Winterbottom method involves first constructing a Wulff polyhedron using planes perpendicular to the vector $\hat{n}\gamma(\hat{n})$, where $\gamma(\hat{n})$ represents the surface energy of a plane oriented along the crystallographic direction $\hat{n}$.[58,61,62] To account for the crystal-substrate interface, the surface energy $\gamma(\hat{n})$ of the plane in contact with the substrate is replaced by an effective interfacial energy term, $\gamma_i(\hat{n})$.[60,63] The magnitude of the $\gamma_i(\hat{n})$ vector is determined by the difference between the surface energy of the crystal-substrate interface, γ_{cs}, and the surface energy of the substrate-vapor interface, γ_{sv}. The ECS can be determined by the γ

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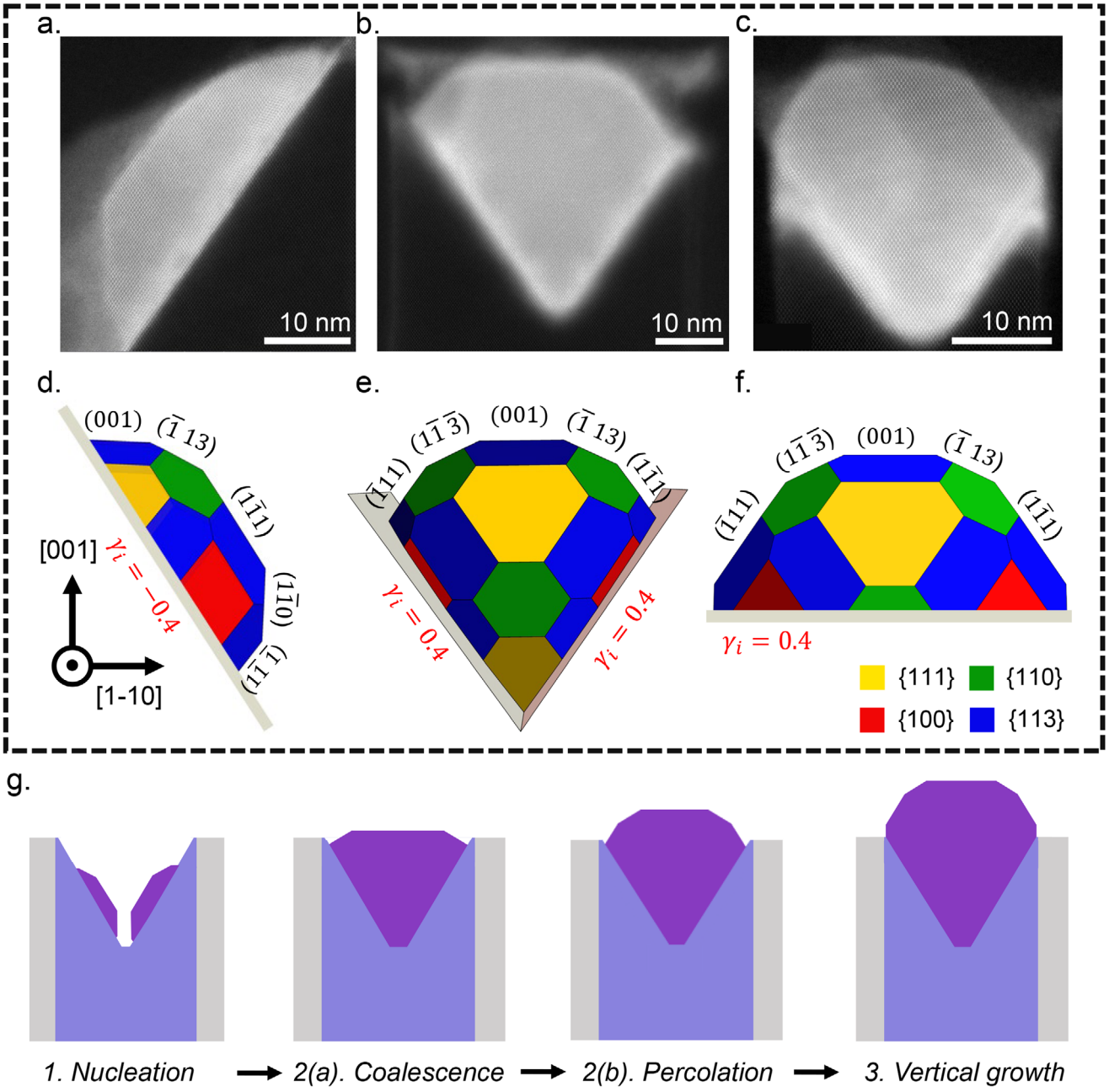

Figure 3. a–c) Atomic-resolution HAADF-STEM micrographs of Ge islands at various growth stages, showing cross-sections of Ge nanowire grown on Si nanopillars with nominal widths of 200 nm (a), 150 nm (b), and 120 nm (c) after 60 s of growth. d) Winterbottom construction of Ge islands on a flat Si (111) surface. e) Grooved-substrate construction of Ge islands confined to two inclined Si (111) surfaces. f) Winterbottom construction of Ge islands on a flat Si (001) surface. g) Schematic representation of the nanowire growth process, illustrating the stages; note that this schematic is not intended to depict the precise geometry of the islands.

polyhedron dual method described by Roosen et al.[64] Several numerical implementations of this approach can be found in the literature.[64–66]

We extended the Winterbottom construction method to determine the shape of Ge islands confined within a V-shaped interface. For Ge growth within Si V-grooves aligned along the ⟨110⟩ direction, the two planes forming the crystal-substrate interface correspond to the Si $(\bar{1}11)$ and Si $(1\bar{1}1)$ surfaces. Therefore, we performed a "Winterbottom-like" construction of Wulff polyhedra, replacing the surface energy values for the planes along the $[\bar{1}11]$ and $[1\bar{1}1]$ directions associated with the groove with the effective interfacial energy term $\gamma_i(\hat{n})$. We call this extension of the Wulff theorem a "grooved-substrate construction".

Figure 3e shows the ECS obtained from the grooved-substrate construction for Ge. For comparison, the ECS obtained from the Winterbottom construction for Ge on flat Si (111) and (001)

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surfaces are presented in Figure 3d,f, respectively. We used experimental values for surface energies $\gamma(\hat{n})$ from Ref. [67], and the interfacial energy term $\gamma_i(\hat{n})$ was adjusted to match the experimentally observed cross-sectional shape. The Winterbottom construction on planar surfaces is performed using the Wulfmaker software.[66] The ECS obtained for the Si (001) surface (Figure 3f) closely matches the experimental morphologies reported for the selective area epitaxy (SAE) of Ge[10,39] and SiGe alloys.[68,69] One notable observation is that two different $\gamma_i(\hat{n})$ values are required to describe the morphology of the Ge island at different stages: –0.4 for the Ge nuclei and 0.4 after coalescence. There are at least two plausible explanations for this observation: 1) The epitaxial elastic strain energy is large enough that small crystallites do not satisfy the conditions of the Wulff construction; 2) The substrate-crystallite interface loses its coherency at a critical size; the observed shape is from a transition from a growth mode where the slowest facets dominate the shape to a shape dominated by the lower-energy facets.[70] An illustration of the effect of different $\gamma_i(\hat{n})$ values on the ECS is provided in the Supporting Information (Figure S6).

Using the insights from experimental observations and equilibrium crystal shapes, we propose a growth mechanism to explain the temporal evolution. Figure 3g illustrates our model, which includes three stages. Stage 1 involves the strain-induced nucleation of Ge islands on the Si surface. These islands expand and begin to coalesce upon impingement. In Stage 2, the coalescence of islands from opposite faces of the Si V-groove initially forms discontinuous bridge-like structures (2a). These bridges expand laterally and eventually coalesce to form a continuous Ge nanowire fully confined within the V-groove (2b). The Ge nanowire also develops inclined facets, as defined by the grooved-substrate construction. Coalescence is inevitable in the SK growth mode; the observations suggest that the fused particle's morphology is energy-minimizing. Finally, in Stage 3, the nanowire extends above the mask level. At this point, the grooved-substrate condition must be modified because 1) the substrate normal does not pass through the origin of the γ-plot; 2) the groove corner may stabilize other facets; 3) the ECS contains interfaces between the top surface and the crystallite. Our observations suggest that the cross-sectional shape resembles the ECS given by the Winterbottom construction on a planar Si (001) surface (Figure 3f).

Having outlined the temporal evolution of Ge nanowire growth, we now shift our attention to a more detailed study of the crystal quality. For this purpose, we prepared FIB cross-sections perpendicular to the in-plane orientation of the nanowires and studied them using Cs-STEM. The nanowire samples were covered by a 50 nm thick layer of amorphous Si_3N_4 to prevent any FIB-induced damage. The results are presented in **Figure 4**.

Figure 4a shows a high-angle annular dark-field (HAADF) STEM image providing an overview image of six nanowire cross-sections. A close-up image of the highlighted nanowire is shown in Figure 4b, with the inset revealing the cross-sectional shape. The fully grown Ge nanowire exhibits a cross-sectional shape defined by facets belonging to the {110}, {111}, {113}, and {001} families. The presence of a small {113} facet in the transition region between the {111} and {001} facets imparts a curved cross-sectional profile to the nanowires observed in AFM line scans and low-magnification images. Close-up images of the remaining nanowires are provided in the Supporting Information (Figure S8). We note that the cross-sectional morphologies exhibit variations in the relative proportions of different facets. This will be explained here below.

We characterized the chemical composition of the nanowires in the cross-section shown in Figure 4b using electron energy loss spectroscopy (EELS). The EELS maps in Figure 4c,d confirm the nanowire's Ge-rich composition and reveal the substrate's sharp interface. Additionally, integrated differential phase contrast (iDPC) imaging was performed near the nanowire-substrate interface to precisely resolve the atomic positions. Figure 4e,f display the iDPC STEM image of the nanowire-substrate interface and the fast Fourier transform (FFT) analysis, respectively.

As observed in Figure 4e,f, the majority of the Ge nanowire retains the crystal orientation of the underlying Si substrate, with quasi-symmetrical twin regions along the Si {111} interface indicated by the red arrows. Notably, these twin defects are confined to the Ge-Si interface and do not propagate throughout the structure. This behavior is likely due to the nanowire growth process, which involves nucleation and coalescence. The growth of the Ge nanowire starts with the nucleation of Ge islands on the Si {111} surfaces. Given the low formation energy of planar defects along the [111] direction in face-centered cubic (FCC) crystals, minor fluctuations in growth conditions can result in the formation of twins along the Si {111} interface.[71] After the initial growth stage, the coalescence of islands from opposite sides of the V-groove shifts the nanowire growth direction to [001], which interrupts the propagation of the twins. A similar phenomenon has been observed in the growth of V-shaped InAs membranes and GaAs nanospades.[50,72]

The presence of twin defects along the {111} interfaces could also alter the interfacial energy $\gamma_i(\hat{n})$. A difference in $\gamma_i(\hat{n})$ value between the two Si {111} interfaces can give the nanowires an asymmetric cross-sectional shape, as observed in Figure 4b. Finally, the distinct diffraction spots for Ge and Si in the FFT images (Figures 4f) indicate that the Ge crystal has fully relaxed the strain from lattice mismatch. Geometric phase analysis (GPA) of the nanowire cross-section (included in Supporting Information) confirms the plastic relaxation of the strain through the formation of a periodic array of misfit dislocations at the Ge/Si interface. The bright contrast of the iDPC image along the interface region in Figure 4e (indicated by the white arrows) further reflects the strain field generated by these misfit dislocations.

From a microscopic point of view, Ge nanowires grown on Si nanopillars with V-grooves offer a promising approach to engineering the size and shape of the nanowires. This method also helps to avoid the interface between the Ge nanowire and the SiO_2 dielectric, which results in further defects and trapped charges. As previously shown, defects near the substrate interface or the gate dielectric interface can affect electronic transport properties.

We evaluated the electronic transport properties of Ge nanowires through Hall measurements. Ge nanowire networks were grown on V-groove Si nanopillars in a Hall bar configuration. **Figure 5a** shows a false-color SEM image of the Hall bar device, with Ti (10 nm)/Au (150 nm) as the ohmic contact. A top gate was fabricated on this nanowire device by evaporating a Ti (10 nm)/Au (150 nm) layer. We used a 30 nm thick AlO_x layer

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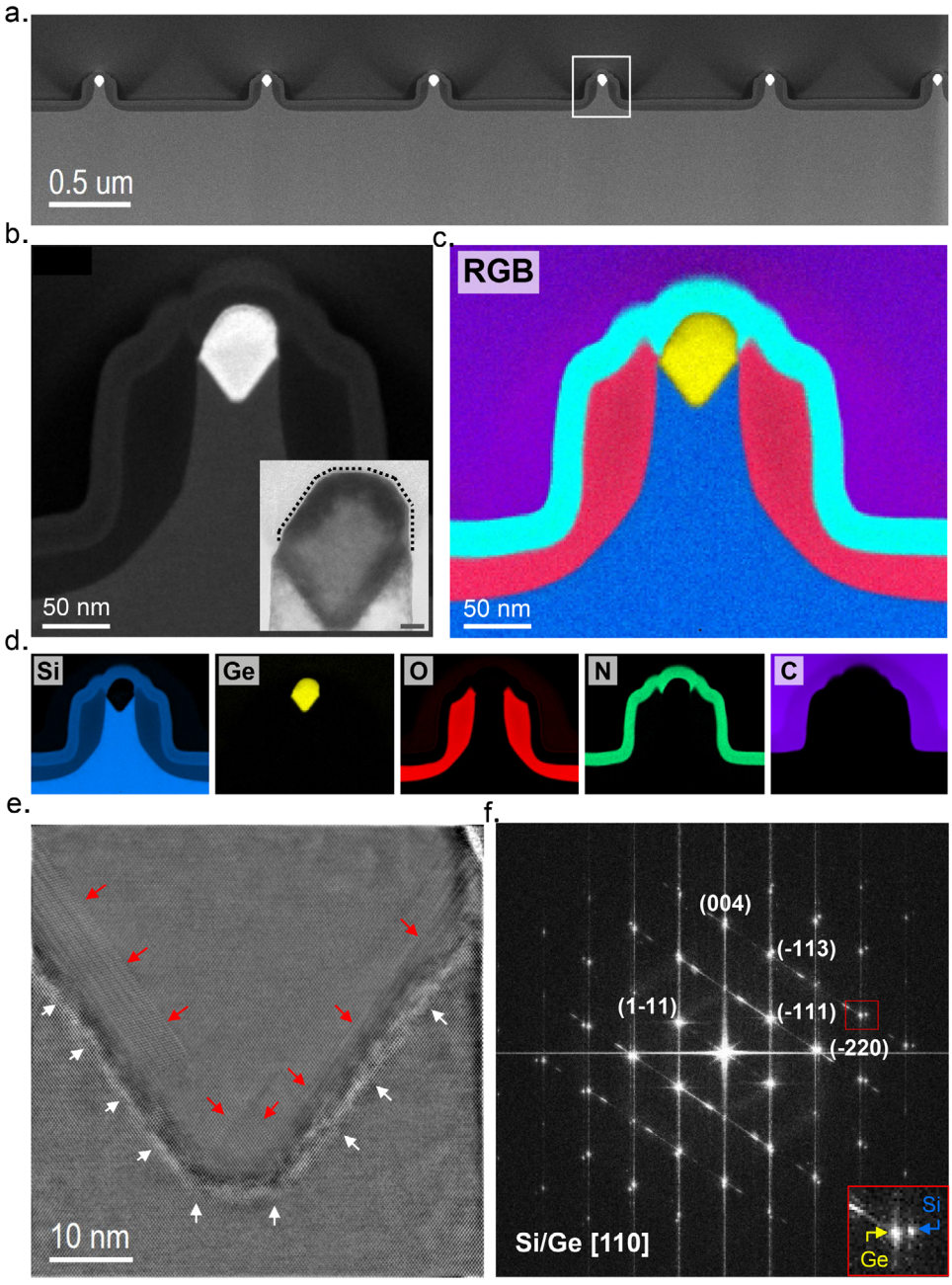

Figure 4. Crystal quality of Ge nanowires. a) HAADF-STEM micrograph of a cross-section cut made perpendicular to the in-plane orientation of six parallel nanowires. b) Atomic-resolution HAADF-STEM micrograph of the nanowire cross-section highlighted in (a). The inset presents a close-up image revealing the cross-sectional shape. The scale bar for the inset figure indicates 10 nm. c) STEM-EELS compositional map of the nanowire cross-section shown in (b). d) EELS maps displaying the distribution of Si, Ge, O, N, and C along the nanowire cross-section. e) Atomic resolution i-DPC image revealing twin defects along the Ge nanowire-Si (111) substrate interface. White arrows mark areas of white contrast observed at the interface, while red arrows highlight quasi-symmetrical twin regions. f) FFT of the image presented in (e).

deposited via atomic layer deposition (ALD) as the gate dielectric. Further details on the device fabrication are provided in the Supporting Information. Magnetotransport measurements were performed on the Hall bar device using a four-terminal voltage-bias setup in a ^{4}He cryostat. The device was operated in accumulation mode by applying a negative DC voltage (V_{TG}) to the top gate. A fixed DC voltage of 500 μV is applied to the source-drain contacts (V_{sd}). The current through the nanowire is measured using a current-to-voltage converter. A DC voltage amplifier and a multimeter are used to measure the four-terminal voltages (V_{xx} and V_{xy}). The Hall (R_{xy}) and longitudinal (R_{xx}) resistances were obtained from the four-terminal voltages and using Ohm's law ($R = V/I$). Hall measurements were conducted at 150, 72, and 15 K. In the following section, we summarize the results from

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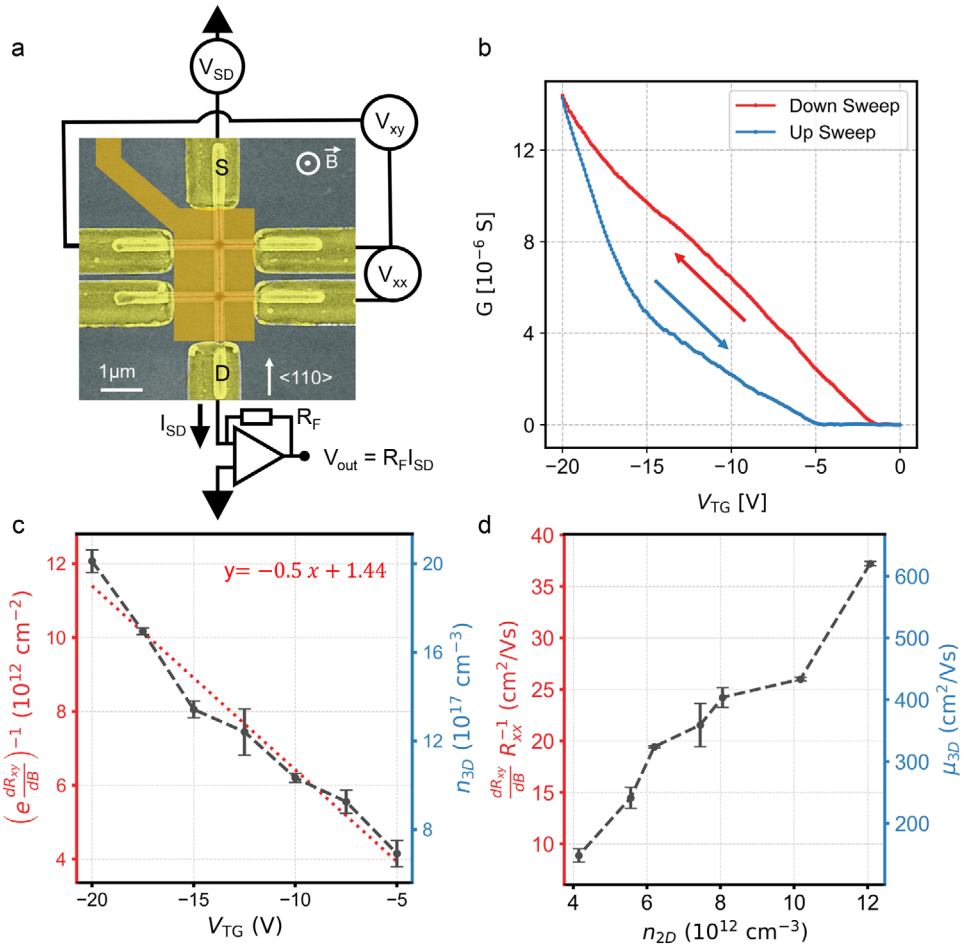

Figure 5. Electronic transport characteristics. a) False-color SEM image of the nanowire Hall bar device, with the contacts, oxide layer, and nanowire shown in gold, gray, and brown, respectively. b) Two terminal conductance (G) as a function of gate voltage (V_{TG}) measured at 150 K. c) Charge carrier density as a function of top gate voltage. The left y-axis (red) shows the factor $\left(e\frac{dR_{xy}}{dB}\right)^{-1}$, which does not rely on geometrical assumptions. The right y-axis shows the 3D charge carrier density, assuming a transport cross-section height of 60 nm. d) Mobility (μ) as a function of charge carrier density. The left y-axis (red) shows the geometrical assumption free factor $\left(R_{xx}^{-1}\frac{dR_{xy}}{dB}\right)$. The right y-axis shows the hole mobility, assuming a transport cross-section width of 60 nm. The reported carrier concentration and the mobility are obtained for a top gate voltage sweep from 0 to –20 V (down sweep) with a 60 s wait time after the voltage sweep.

150 K, measurement results from 72 and 15 K are provided in Supporting Information (Figure S14).

Figure 5b shows the two-terminal conductance (G) as a function of top gate voltage (V_{TG}). As expected for undoped structures, the nanowires are insulating at zero gate voltage. Finite conductance through the nanowire is achieved above a threshold voltage, which depends on the sweep direction of the top gate voltage. We attribute the observed gate hysteresis to the presence of charge traps at the interface between the Ge nanowire and the AlO_x. Further studies on the capacitance should be performed to quantify the interface trap density. Current begins to flow above a threshold voltage, allowing for Hall effect transport under an applied magnetic field. From Hall (R_{xy}) and longitudinal (R_{xx}) resistance measurements as functions of magnetic field (B), we extract charge carrier density, given by $n = \left(e\frac{dR_{xy}}{dB}\right)^{-1} H_{\text{eff}}^{-1}$, and the carrier mobility, given by $\mu = \left(R_{xx}^{-1}\frac{dR_{xy}}{dB}\right)\frac{L_x}{W}$. Here, e is the elementary charge. The voltage drop measured across different contact pairs showed a good correlation, indicating consistent electronic transport across different junctions within the device (Figure S13, Supporting Information). The most important physical characteristic to determine the transport properties is the area of the cross-section, which we have determined by performing a FIB cut on an equivalent device (Figure S12c, Supporting Information). We have used the maximum dimensions for height (60 nm) and width (60 nm). It is important to note that the nanowires do not have a rectangular cross-section, so the extracted mobility and 3D carrier concentration represent the lower limits of these values. In Figure 5c, we plot the carrier concentration as a function of the top gate voltage for a sweep from 0 to –20 V (down sweep) with a 60 s wait time after the

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voltage sweep. Electrical measurement results for the voltage sweep from –20 to 0 V (up sweep) are provided in Supporting Information (Figure S15). The left axis represents the 2D charge carrier density, independent of geometrical assumptions. The right axis shows the 3D charge carrier density, assuming a height (H) of 60 nm. The carrier concentration increases linearly with the applied negative gate voltage. From this linear trend, we extracted a gate capacitance of approximately 8×10^{-4} F/m^2, which is 50% lower than the value predicted by the parallel plate capacitance model, $\frac{\epsilon\epsilon_0}{d_{ALD}} \approx 1.5 \times 10^{-3}$ F/m^2. This deviation is likely due to immobile charge carriers trapped in interface states and disorder at the Ge nanowire–gate oxide interface,[73] which aligns with the presence of gate hysteresis. Since these trapped charges do not contribute to the Hall carrier concentration, the measured gate capacitance appears lower.[74]

Figure 5d presents the mobility data as a function of charge carrier density. Similar to Figure 5c, the assumption-free carrier density is shown on the left axis. The right axis represents the mobility values extracted assuming W = 60 nm. The carrier mobility increases with carrier concentration throughout the entire accessible density range. We measured mobility values starting at 200 cm^2/Vs at a carrier density of 4×10^{12} cm^{-2}, which increased to 600 cm^2/Vs at a density of 12×10^{12} cm^{-2}. These values are slightly higher than those reported in our previous work and are comparable to the mobility values observed in free-standing Ge nanowires. A power law fit, $\mu = n^{\alpha}$, applied to the mobility data as a function of carrier density, yielded an exponent $\alpha = 1.22$. This exponent suggests that mobility is primarily limited by scattering from remote impurities at the dielectric/semiconductor interface.[75,76] The increase in mobility with rising carrier density can be attributed to enhanced disorder screening. Improving the semiconductor/dielectric interface and introducing strain will further enhance the electronic transport properties. We further provide evidence for the influence of trapped charges on the transport properties in the Supporting Information.

4. Conclusion

In summary, we have developed a confined selective area epitaxy technique for in-plane nanowires. Ge nanowires and their networks were successfully grown on an oxidized Si nanopillar featuring a V-shaped groove as the growth substrate, where growth proceeds through the nucleation and coalescence of multiple Ge islands. Using Winterbottom-like constructions, we demonstrate that the coalescence process remains fully confined within the V-groove and is driven by surface energy minimization. This behavior is both fundamental and transferable to other material systems. A detailed analysis of nanowire morphology, chemical composition, and crystal quality is presented. Low-temperature magnetotransport measurements on Ge nanowire Hall bars showed a gate tunable hole density and peak mobility of approximately 600 cm^2/Vs at a density of 12×10^{12} cm^{-2}. These findings open new possibilities for precise control over nanowire shape and size through confined selective epitaxy.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The experimental data generated in this study have been deposited in the zenodo database.

Keywords

electronic transport, germanium, nanowire networks, selective area epitaxy, winterbottom construction

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