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On-Chip Microheater-Based Back-End-of-Line Compatible Synthesis of VO_2 Films for Reconfigurable Silicon Photonics

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ABSTRACT

We report a back-end-of-line (BEOL)-compatible approach for integrating high-quality vanadium dioxide (VO_2) into silicon photonic platforms using on-chip doped silicon microheaters as localized thermal processors. VO_2 is a promising material for reconfigurable photonics due to its large refractive index modulation and fast, energy-efficient metal-insulator transition (MIT). However, its integration is hindered by the high thermal budget required for crystallization and the difficulty of patterning. In this work, vanadium metal is deposited at room temperature and patterned via a lift-off process, followed by microheater-assisted local oxidation and crystallization to form VO_2 without exceeding the global BEOL temperature constraints. Structural and spectroscopic characterization confirms the formation of VO_2 with high crystallinity and accurate stoichiometry. Device-level integration is demonstrated using silicon racetrack resonators, where the measured switching contrast shows excellent agreement with simulations based on literature optical constants, indicating material quality comparable to that of high-temperature-grown films. The microheater platform enables both material synthesis and reversible MIT switching, and is inherently scalable via parallel electrical biasing for wafer-scale processing. Beyond VO_2, this approach provides a general pathway for integrating thermally demanding functional materials into complementary-metal-oxide-semiconductor (CMOS)-compatible systems.

1 | Introduction

Reconfigurable silicon photonics has emerged as a critical enabling technology for adaptive optical interconnects, programmable photonic circuits, and neuromorphic computing, where dynamic control of phase and amplitude must be achieved within a compact footprint and under tight power constraints [1]. Conventional thermo-optic and electro-optic tuning in silicon relies on weak index modulation and long interaction lengths, resulting in millimeter-scale devices and significant power consumption. Vanadium dioxide (VO_2), with its metal-insulator transition (MIT) near 68°C, offers a fundamentally different mechanism: a large and abrupt change in the complex refractive index arising from a monoclinic to tetragonal crystal phase transition, which enables strong optical modulation within submicrometer interaction lengths. The MIT is intrinsically fast, reversible, and energy-efficient, ideally suited for volatile photonic reconfiguration [2, 3]. These attributes make VO_2 uniquely attractive for dense, high-speed, and power-efficient reconfigurable photonic systems [4–7].

Khoi Phuong Dao and Siddharth Kumar contributed equally to this work.

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Despite these attractive attributes, thermal budget remains a central practical constraint for integrating high-quality VO_2 with silicon photonics. Numerous studies show that increasing growth or post-deposition annealing temperature to 450°C or above improves VO_2 crystallinity, grain size, and stoichiometric purity—factors that narrow the MIT hysteresis, sharpen the resistivity/optical contrast, and increase the resistivity ratio between insulating and metallic states [8–23]. However, such processing conditions are incompatible with standard back-end-of-line (BEOL) integration, which typically imposes an upper thermal limit below 450°C to avoid degradation of metal interconnects, dopant diffusion, and damage to underlying electronic circuitry.

Considerable efforts have focused on reducing the thermal budget or tailoring VO_2 properties through materials and process engineering. Strategies such as introducing dopants (e.g., W, Mo) [24], or adjusting oxygen partial pressure [12, 25] during deposition/annealing have been shown to influence crystallinity, defect concentrations, and phase transition behavior, enabling improved optical and electrical switching at reduced processing temperatures as low as 300°C. Likewise, buffer or seed layers have been used to enhance switching characteristics in VO_2 films grown at reduced temperatures [26–28]. While these approaches can partly mitigate high thermal budgets or extend the process window, they often introduce additional material complexity, process steps, or trade-offs in phase transition sharpness and film uniformity.

In addition to the thermal budget constraint, patterning VO_2 reliably presents several practical limitations that complicate integration with silicon photonic circuitry. Conventional plasma etches (Cl- or F-based RIE/ICP) suffer from low selectivity to Si/SiO_2, formation of low-volatility vanadium halides that promote redeposition and rough or tapered profiles, mask erosion, and potential contamination or damage to underlying waveguides; these effects make tight critical-dimension control and low optical loss difficult to achieve. Alternative removal methods (ion milling, focused ion beam etching, laser ablation, or thermal/atomic-layer etch variants) can produce higher fidelity patterns but require specialized equipment, risk surface damage or implantation, and generally lack the throughput or process maturity expected for foundry-scale BEOL flows. As a result, etch-free patterning strategies are strongly preferred for integrating VO_2 with silicon photonics [12], as they minimize substrate damage, preserve waveguide integrity, and better align with foundry-compatible fabrication workflows. To summarize, developing novel fabrication and patterning techniques for integration of functional oxides such as VO_2 into monolithic silicon platforms remains an important frontier problem.

Here, we present an alternative integration route that leverages on-chip microheaters as localized thermal sources. Our process begins with deposition of metallic vanadium with the substrate maintained near room temperature, which is fully compatible with standard resist lift-off patterning and therefore avoids the need for aggressive VO_2 dry etching. The same doped-silicon microheater serves a dual function: first, it provides the high local temperature required to crystallize and oxidize deposited vanadium into VO_2 with excellent crystallinity; second, it enables subsequent reversible heating to drive the MIT for device operation. By confining high temperatures to micrometer-scale regions, the microheater decouples the material synthesis temperature from the global wafer thermal budget, preserving BEOL compatibility. This localized heating strategy eliminates the need for global furnace or rapid thermal annealing (RTA) steps, avoids additional material complexity, and offers precise spatial and temporal control over both VO_2 formation and switching. As a result, it provides a streamlined, foundry-aligned pathway for integrating high-quality, reconfigurable VO_2 devices onto fully processed silicon photonic platforms.

2 | Results and Discussion

2.1 | Synthesis and Characterization of VO_2 via Oxidation of Vanadium Metal

We first investigated the synthesis of VO_2 via post-deposition oxidation of vanadium metal [20, 29–31]. In most prior studies, vanadium oxide precursors are deposited with the substrate maintained at elevated temperatures to ensure film continuity and phase formation, while the oxidation processes have also been explored under a range of temperatures and ambient conditions [32, 33]. In contrast, our approach employs room-temperature deposition of pure V thin films, followed by post-deposition annealing at 450°C in ambient air to convert V into VO_2 (see Experimental Section). Oxidation-based methods have been reported in the literature [34], indicating potential compatibility with low-thermal-budget processing and suggesting a viable pathway for CMOS back-end-of-line integration.

To verify the structural phase of VO_2 synthesized via post-deposition thermal oxidation, we performed X-ray diffraction (XRD) characterization on films prepared via ambient oxidation on a hot plate. The results are summarized in Figure 1. The wide-angle XRD pattern in Figure 1a shows a distinct diffraction peak near 28°, corresponding to the (011) plane of monoclinic VO_2 (ICSD 647610), confirming successful phase formation on the SiO_2/Si substrate. A strong Si substrate peak is observed near 70° with a Si K_β peak at around 63°, while no additional diffraction peaks are detected, indicating that VO_2 is the dominant crystalline phase with no detectable secondary phases in this out-of-plane scan.

The film composition and thickness were further analyzed using Rutherford backscattering spectrometry (RBS). As shown in Figure 1b, the measured spectrum agrees well with the simulated profile, yielding a film thickness of approximately 80 nm. The extracted composition corresponds to ~32% V and ~68% O, close to the stoichiometric ratio of VO_2. This result indicates that ambient oxidation of V can produce near-stoichiometric VO_2 films.

A key characteristic of VO_2 is its insulator-to-metal transition occurring near room temperature. To evaluate this behavior, resistance–temperature measurements were performed from room temperature to 100°C, as shown in Figure 1c. A sharp drop in resistance is observed near 70°C, indicating the transition from the insulating to the metallic phase. Upon cooling, the resistance recovers along a distinct trajectory, exhibiting the characteristic hysteresis associated with the first-order phase transition in

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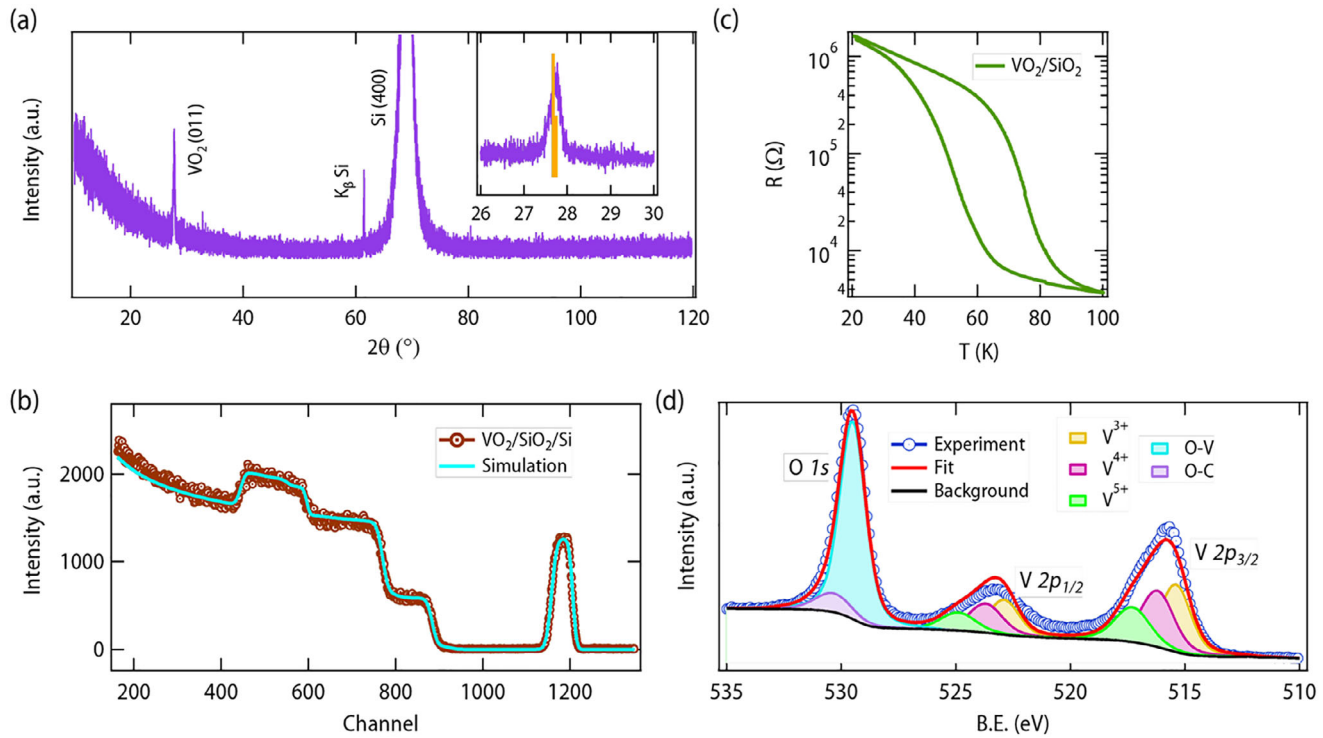


FIGURE 1 | Structural, compositional, and electrical characterization of VO_2 thin films formed on control Si/SiO_2 substrates via ambient oxidation on a hot plate: (a) wide-angle XRD pattern showing the VO_2 film peak and Si substrate peaks, inset shows the VO_2 (011) peak compared to film peak, (b) RBS spectrum showing observed and simulated statistics, (c) resistance vs temperature curve showing an insulator to metal transition, (d) XPS spectrum with fit and deconvoluted phases.

VO_2. This reversible switching behavior confirms the functional integrity of the thermally oxidized films.

X-ray photoelectron spectroscopy was performed to further examine the chemical states of the film, focusing on the V 2p and O 1s core levels. As shown in Figure 1d, the V 2p signal appears as a characteristic doublet consisting of the $2p_{3/2}$ and $2p_{1/2}$ components. The spectrum can be deconvolved into three contributions, corresponding to V^{3+}, V^{4+}, and V^{5+} oxidation states. The presence of multiple valence states is commonly observed in vanadium oxide systems grown by various methods and is likely influenced by surface effects, since XPS primarily probes only the top few nanometers of the film.

2.2 | Microheater-Assisted Synthesis and Processing of VO_2

Our integration strategy is built upon doped silicon microheaters that function as localized, programmable thermal platforms for on-chip material synthesis and reconfigurable device actuation. Compared to metallic heaters, doped Si heaters are thermally, mechanically, and chemically robust, leveraging the high melting point and structural integrity of single-crystalline silicon to sustain annealing temperatures exceeding 800°C without degradation [35]. They enable flash heating and rapid quenching with heating and cooling rates above 10^8°C/s, allowing access to metastable phases and kinetic regimes not attainable through conventional furnace annealing [36]. Since the doped regions are lithographically defined during ion implantation, the temperature distribution and lateral thermal gradients can be engineered through inverse-designed geometries, enabling spatially selective annealing with micron-scale precision and < 1°C temperature excursions [37]. The platform is fully compatible with standard CMOS manufacturing, relying exclusively on unit processes already established in silicon foundry flows. We have further demonstrated foundry-fabricated, individually addressable two-dimensional microheater arrays [38], providing a scalable architecture for high-throughput combinatorial screening of thermal processing conditions or parallel heat treatment of large numbers of on-wafer photonic components.

The process flow is schematically illustrated in Figure 2a. Fabrication begins with the definition of doped Si microheaters within the device layer of a silicon-on-insulator (SOI) wafer via ion implantation, followed by the formation of metal contacts and the dielectric passivation to electrically isolate the heater from subsequently deposited materials. The performance of our microheaters was characterized by extracting the temperature from the redshift of the Raman peak corresponding to the doped silicon layer at varying applied voltage (Figure 2b) [39]. This experimental calibration is further validated by a COMSOL Multiphysics simulation (Figure 2c), which also illustrates the highly confined temperature profile from the microheaters. A patterned resist layer is then defined on the heaters, and a vanadium metal film is deposited when keeping the substrate near room temperature, enabling a standard lift-off process to form precisely aligned V patches without exposing the underlying heater or photonic structures to plasma etching. Following lift-off of the V metal, conversion to VO_2 is achieved by electrically biasing the

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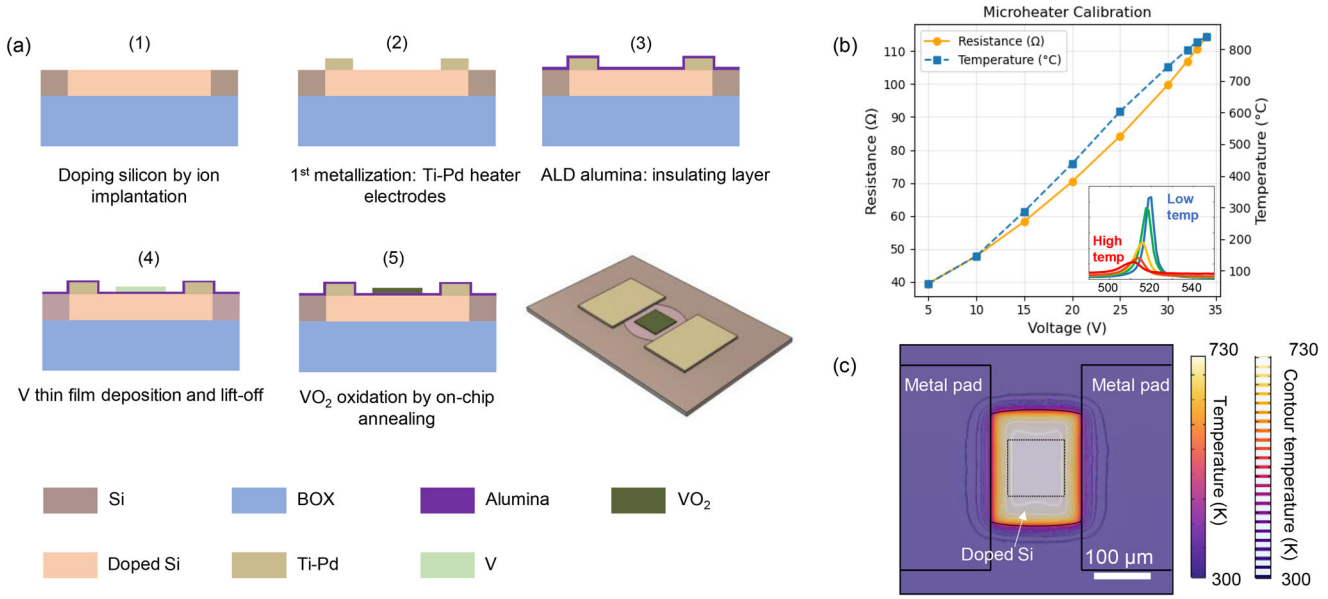


FIGURE 2 | Schematics of low-thermal-budget integration of VO_2 on silicon photonic platform with (a) fabrication process flow, BOX: buried oxide, ALD: atomic layer deposition, (b) microheater's performance: steady-state temperature vs.voltage with inset illustrating silicon's Raman peak redshift at different temperatures, and (c) microheater's temperature profile at 20 V predicted by COMSOL simulation.

microheater to 22 V, corresponding to a localized temperature of approximately 500°C, maintained for 90 s in ambient air. The thermal cycle includes 20 s ramp-up and 10 s ramp-down. The phase transformation is both visually and structurally evident: Figure 3a compares the metallic V patch before annealing with the converted VO_2 after annealing, revealing a clear optical contrast change. The transformation in film morphology was also recorded by scanning electron microscopy SEM (Section S1). This rapid and spatially confined transformation is further documented in Video S1. Different annealing conditions were also tested, and VO_2 formation can be observed with annealing temperatures ranging from 450°C to 500°C. 500°C annealing temperature results in VO_2 with stable and large visual contrast between the dielectric state and the metallic state (see Section S2).

The crystallinity and phase purity of the converted film were evaluated by Raman spectroscopy. High-quality VO_2 synthesized via conventional high-temperature routes such as reactive sputtering typically exhibits characteristic monoclinic (M1) phonon modes near 190, 220, and 610 cm^{-1} [40–43], which are highlighted by the blue arrows in Figure 3b and Figure 3c. These signature peaks are clearly observed in our reference VO_2 film deposited at elevated temperature using a VO_2 sputtering target (Figure 3b). As shown in Figure 3c, the microheater-annealed VO_2 exhibits the same dominant M1 phonon modes with sharp linewidths, indicating high crystallinity despite the absence of global high-temperature processing. In addition to the VO_2 peaks, weak features associated with V_2O_5—commonly present as a secondary phase in vanadium oxide films grown on non-lattice-matched templates—are detected and highlighted by red arrows in Figure 3b,c. Notably, the relative intensity of these V_2O_5-related peaks is lower in the microheater-annealed sample than in the conventionally deposited reference, while the three characteristic VO_2 modes remain dominant. This comparison indicates that the localized annealing process yields a high VO_2/V_2O_5 phase ratio comparable to, and in some cases exceeding, that achieved through traditional high-thermal-budget methods. By comparing the signature peak's intensity of the two phases: 190 cm^{-1} (V—V mode) and 610 cm^{-1} (V—O vibration) of VO_2, and 145 cm^{-1} (lattice vibration) and 990 cm^{-1} (V═O vibration) of V_2O_5 [42, 43], we can roughly estimate the VO_2/V_2O_5 phase ratio [44], which can reach as high as 9:1 in sample integrated by low-thermal-budget method, compared to approximately 1:2 in samples deposited by traditional methods. The combination of the rapid cooling enabled by the microheater and the presence of the ALD-deposited alumina buffer layer [45] may account for the improved VO_2 phase fraction in the film.

We further verified functional integrity through thermally induced switching measurements. Upon external heating by the microheater biased at 8.5 V, which corresponds to approximately 80°C, the film undergoes a pronounced metal–insulator transition accompanied by a distinct change in optical contrast [46], as shown in Figure 3d and Video S2. The darker appearance in the metallic state reflects the substantially higher extinction coefficient of VO_2 above the transition temperature, confirming that the locally synthesized film exhibits the optical contrast required for active silicon photonic modulation. The optical contrast of VO_2 between two states was then used to examine the cycling endurance of the material, demonstrating 100 million switching cycles without noticeable degradation (Section S3).

2.3 | Device Integration and Optical Switching Demonstration

To evaluate both the integration compatibility and optical properties of the locally synthesized VO_2, we incorporated the material into a silicon-on-insulator racetrack resonator. This experiment serves two purposes. First, it demonstrates seamless integration with a standard Si photonic device without degrading resonator performance. Second, it provides a practical route to extract the

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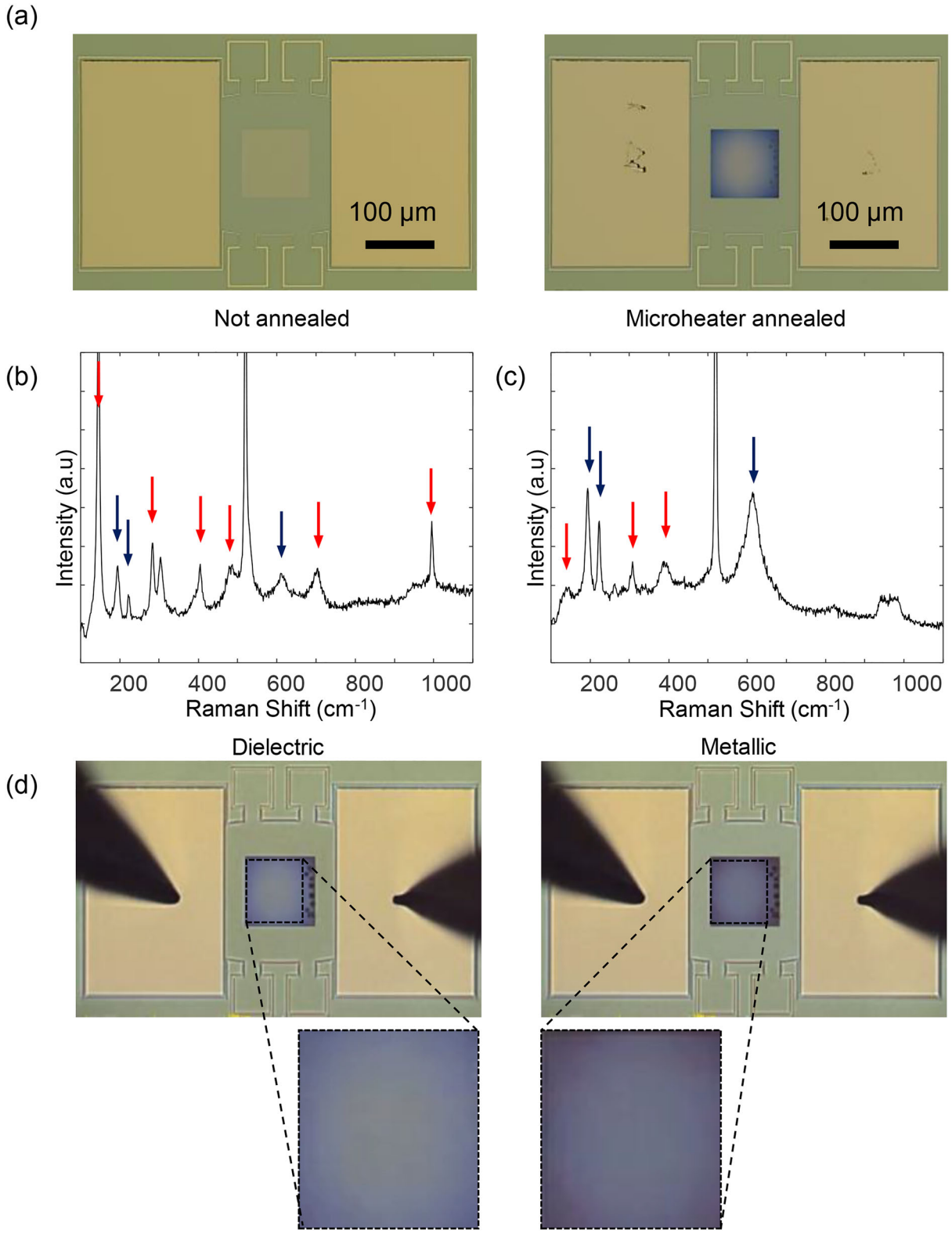


FIGURE 3 | (a) Microscopic pictures of the pure V sample before annealing and VO_2 sample after annealed by the microheater. Raman spectra of VO_2 thin film deposited by (b) high-thermal-budget magnetron sputtering and (c) low-thermal-budget method, with VO_2 signature peaks marked by blue arrows while V_2O_5 signature peaks are marked by red arrows [42]. (d) Visible change of VO_2 when being switched from dielectric to metallic phase.

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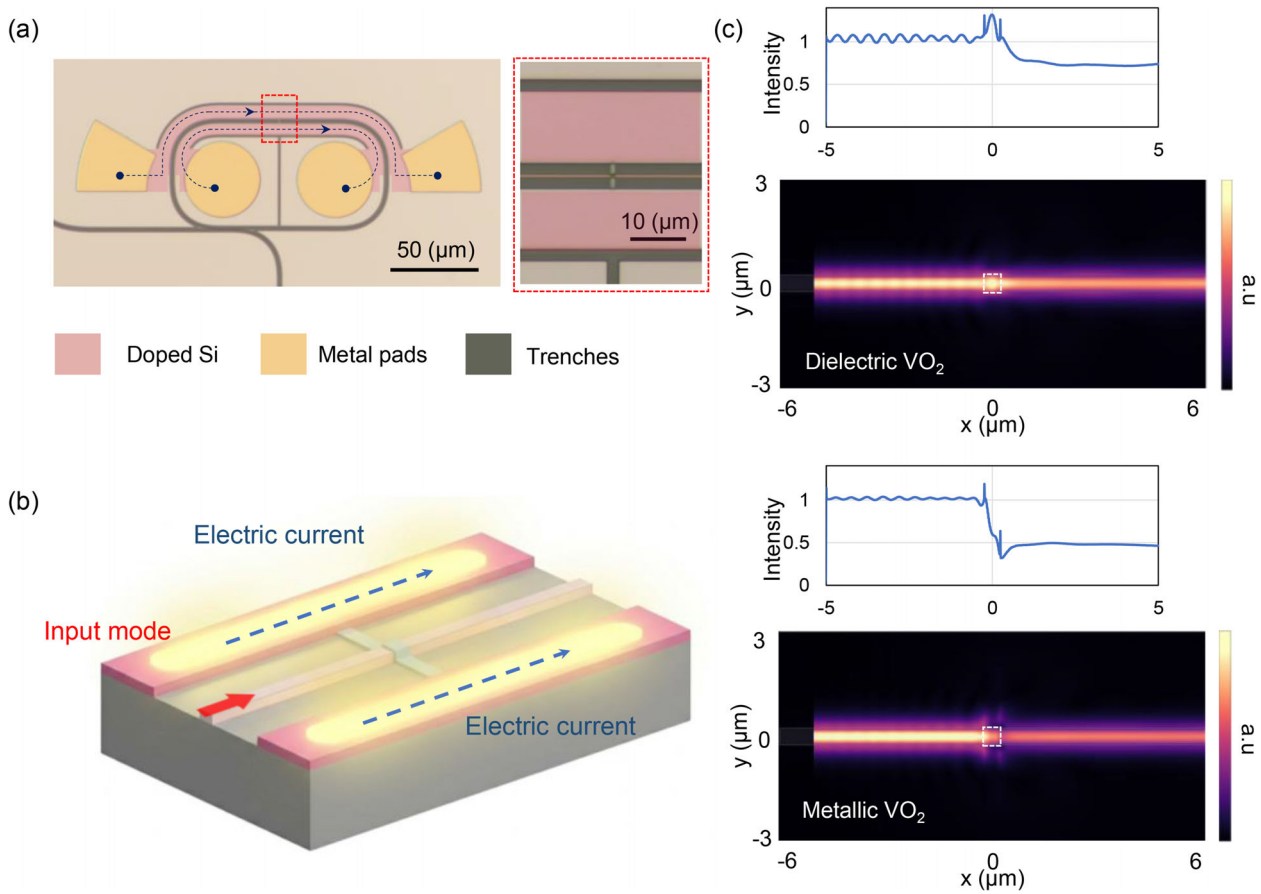


FIGURE 4 | (a) Microscopic view of racetrack resonator with integrated side heaters and VO_2 cladding. The doped silicon and metal pads are false-colored. (b) Schematic of FDTD simulation on strip waveguide with VO_2-active material cladding. (c) FDTD simulated electric field of the TM0 mode when VO_2 patch (highlighted by white dash lines) is in the dielectric and metallic states with the corresponding normalized field intensities along the propagation direction, clearly showing the elevated loss in the metallic state.

effective complex refractive index of VO_2 in both its insulating and metallic phases. Because of the small size of VO_2 patches defined by the microheaters, conventional thin-film metrology such as spectroscopic ellipsometry is not applicable. Instead, the resonator platform enables quantitative extraction of propagation loss and index shift through resonance wavelength, linewidth, and extinction analysis [47].

As shown in the false-colored optical micrograph in Figure 4a, the device consists of a fully etched 480-nm-wide silicon waveguide forming a racetrack cavity, flanked by two doped-Si side heaters positioned laterally to the waveguide core. The heaters are electrically driven through metal contacts, with current flowing roughly parallel to the waveguide, indicated by dashed arrows in Figure 4a. This side-heater configuration provides efficient thermal coupling to the VO_2 cladding while minimizing optical overlap between the guided mode and free carriers in the doped Si, thereby reducing parasitic absorption loss. The thermal effect of side heaters during operation is illustrated in Figure 4b and Section S4. A 500-nm-long and 30-nm-thick vanadium patch was deposited directly atop the waveguide using room-temperature sputtering and lift-off, forming a discrete cladding segment. The same integrated heaters were first used to locally anneal the V metal patch into polycrystalline VO_2 and subsequently employed to reversibly drive the MIT during optical measurements, enabling in situ characterization of both phases within the operating photonic device.

Prior to measurement, we carried out full-wave electromagnetic simulations using the Tidy3D FDTD solver [48] to predict the modal confinement and loss characteristics of the VO_2-cladded Si waveguide. The simulation geometry is shown in Figure 4b. The complex refractive indices (n, k) of VO_2 in both insulating and metallic phases was taken from well-established literature datasets obtained from high-quality VO_2 films [49, 50], ensuring that the modeling reflects intrinsic material properties rather than fitted device parameters. Figure 4c shows the simulated TM-mode field profiles and the corresponding absorption-induced attenuation. Owing to the large extinction coefficient in the metallic phase, a pronounced reduction in resonator Q-factor is expected upon transition. The simulations predict additional insertion losses of 1.2 ± 0.1 and 3.3 ± 0.2 dB for the dielectric and metallic states, respectively, arising from the VO_2 cladding segment. The reported uncertainties correspond to the fabrication variations in the VO_2 cladding thickness, assumed to be within 2 nm.

The measured transmission spectra of the racetrack resonator are presented in Figure 5 for both phases. In the insulating state at room temperature, the resonator exhibits sharp resonances

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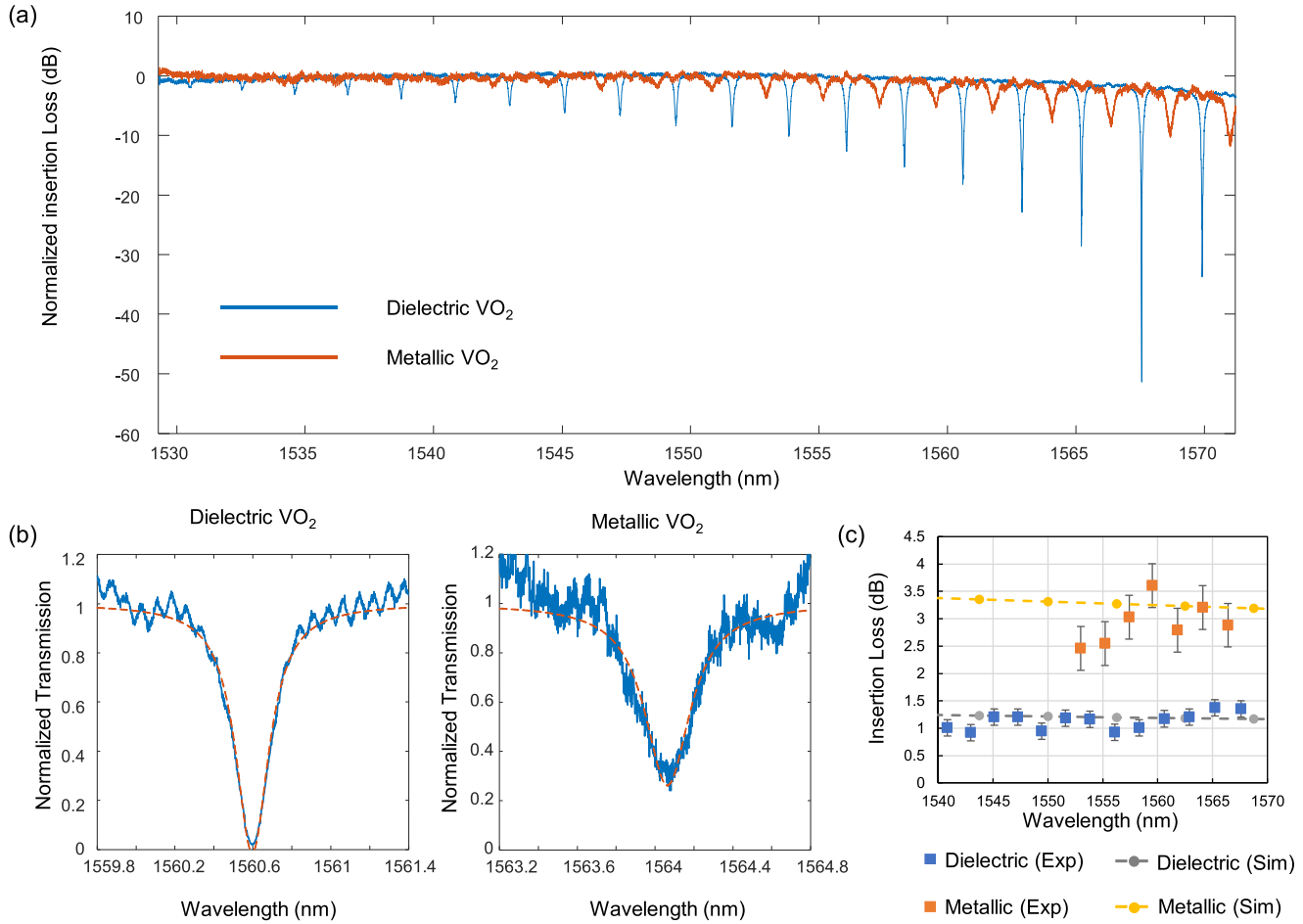


FIGURE 5 | (a) Transmission spectra of racetrack resonators with integrated VO_2 cladding. (b) Resonant peaks corresponding to dielectric VO_2 and metallic VO_2 were Lorentzian fitted. (c) Measured insertion losses are compared with predictions from FDTD simulations.

with high Q-factors, consistent with weak absorption in dielectric VO_2. When the integrated heaters are biased to induce the MIT, the resonances broaden significantly, reflecting enhanced modal absorption in the metallic phase. Each Lorentzian-fitted resonant peak is fitted to the racetrack resonator transmission function (Figure 5b), enabling extraction of the propagation losses and the coupling coefficient via [51]:

$$T = \left| \frac{t - e^{-\frac{\alpha L}{2}} e^{i\beta L}}{1 - t e^{-\frac{\alpha L}{2}} e^{i\beta L}} \right|^2 \quad (1)$$

where T is the transmittance, t is the self-coupling coefficient within the bus waveguide (through-port transmission), α is the amplitude attenuation coefficient inside the racetrack, β is the propagation constant of the mode, and L is the racetrack's length. The experimentally derived insertion losses due to the VO_2 using this approach average approximately 1.1 ± 0.2 and 2.9 ± 0.5 dB in the dielectric and metallic states, respectively, in excellent agreement with the FDTD predictions (Figure 5c). This close quantitative correspondence, achieved without fitting the optical constants, strongly indicates that the microheater-annealed VO_2 possesses optical properties comparable to high-quality reference films and retains the large index contrast required for efficient silicon photonic modulation [52, 53].

3 | Discussion and Conclusion

This study demonstrates that microheater-assisted processing enables synthesis of vanadium dioxide films with structural and optical quality comparable to those obtained through conventional high-temperature deposition and annealing, without the performance penalties often associated with globally low-temperature-processed VO_2. Raman spectroscopy confirms dominant M1-phase signatures with suppressed secondary phases, and device-level measurements show quantitative agreement with simulations based on optical constants from high-quality reference films. The extracted insertion losses in both insulating and metallic states closely match theoretical predictions using a well-established VO_2 database, indicating that the locally crystallized VO_2 retains intrinsic optical contrast and sharp metal–insulator transition characteristics. These results suggest that high local synthesis temperature—not necessarily global wafer temperature—is a suitable determinant of VO_2 quality, and that confining thermal processing spatially can preserve material performance while maintaining BEOL compatibility.

The microheater platform is inherently scalable to wafer-level manufacturing. Large arrays of heaters can be electrically interconnected and biased concurrently using a single constant-voltage source, for example, through a multi-site probe card.

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Such uniform parallel biasing allows hundreds or thousands of sites to undergo identical thermal cycles simultaneously, enabling high-throughput processing that can potentially rival or exceed bulk furnace annealing in effective throughput per wafer. Importantly, this parallelism distinguishes the approach from laser annealing, which is typically implemented in a raster-scanning configuration optimized for ultrafast, localized treatment. While laser processing is effective for rapid surface modification, it becomes throughput-limited when thermal steps require sustained heating for crystallization, phase stabilization, or defect annihilation—as is the case for VO_2 formation (which lasts over 1 min). In contrast, microheater-driven annealing naturally supports longer dwell times without sacrificing scalability.

The platform can, in the future, support high-throughput combinatorial exploration of thermal processing conditions for such functional materials. Individually addressable heater arrays allow systematic variation of temperature, ramp rate, dwell time, and cooling profile across a single wafer, generating multidimensional process maps within one experimental run [54]. For complex oxide systems where phase stability and functional properties are highly sensitive to thermal history, such spatially resolved programmability offers a powerful tool for rapid discovery and process refinement.

Finally, the implications of this approach extend well beyond VO_2. Many functional materials are considered incompatible with BEOL integration primarily because their optimal phase formation or activation requires temperatures exceeding typical back-end limits. Localized microheater processing provides a pathway to integrate correlated oxide materials, transparent conducting oxides, electro-optic, magneto-optic, and ferroelectric compounds, as well as wide-bandgap nitride semiconductors, without exposing the full wafer to elevated temperatures. By decoupling synthesis temperature from global thermal budget, the microheater strategy redefines the practical boundaries of BEOL compatibility and opens a broadly applicable route toward heterogeneous integration of high-performance functional materials on silicon photonic platforms.

In conclusion, we have demonstrated a silicon back-end-of-line (BEOL) compatible strategy for integrating high-quality VO_2 into silicon photonic platforms by leveraging doped Si microheaters as localized thermal processors. This approach decouples the high temperatures required for VO_2 crystallization from the global wafer thermal budget, enabling room-temperature deposition, lift-off patterning, and confined post-deposition annealing within BEOL limits. Device-level characterization confirms that the resulting VO_2 exhibits optical properties and switching performance comparable to films produced by conventional high-temperature methods, as evidenced by the good agreement between measured resonator losses and simulations based on literature optical constants. The scalability of electrically biased microheater arrays further supports wafer-scale, parallel processing and high-throughput optimization. Beyond VO_2, this framework provides a general pathway for integrating a broad class of thermally demanding functional materials into CMOS-compatible silicon photonics, expanding the design space for reconfigurable and heterogeneous photonic systems.

4 | Experimental Section

The fabrication of the integrated VO_2 photonic devices was performed on a standard silicon-on-insulator (SOI) platform with a 220 nm thick silicon device layer and a 2 μm thick buried oxide (BOX) layer. The process flow was designed to ensure full compatibility with back-end-of-line (BEOL) thermal budget constraints.

4.1 | Device Fabrication

4.1.1 | Microheater Realization

The localized heaters were formed by selective ion implantation of the silicon layer. Doping windows were patterned via electron beam lithography (EBL-Elionix-F125) using PMMA resist (PMMA A6 950K). Phosphorus ions were implanted to achieve the desired carrier concentration for efficient resistive heating. The dopants were activated by Rapid Thermal Annealing to achieve an active doping concentration close to 10^{20} cm^{-3}. Electrical metal pad contacts to the doped Si heaters were fabricated using a Ti/Pd (20 nm/200 nm) stack. The electrodes were deposited via an AJA e-beam evaporator and patterned through a lift-off process with AZ nLOF 2020 photoresist and lithography (Heidelberg DirectWrite-MLA150). A 20 nm thick conformal layer of alumina (Al_2O_3) was deposited over the entire chip using Atomic Layer Deposition (ALD) (Veeco Savannah 200) at a substrate temperature of 150°C.

4.1.2 | Waveguide Pattering

On complete chips with built-in microheaters, silicon waveguides and racetrack resonators were defined using electron-beam lithography (EBL-Elionix-F125) with ZEP 520A positive resist. The patterns were transferred to the silicon layer via reactive ion etching (SAMCO RIE-200iP) using a Cl_2-based chemistry to achieve vertical sidewalls and low propagation loss.

4.1.3 | Vanadium Deposition and Lift-Off

A double layer of PMMA (PMMA A4 495K and PMMA A6 950K) was patterned using EBL (EBL-Elionix-F125). VO_2 films were grown by post-deposition annealing of V deposited on microheater chips for the demonstration of the low-thermal-budget integration, and on SiO_2/Si substrates for characterization. Both substrates were cleaned with isopropyl alcohol and blow-dried with nitrogen gas. A 99.9% pure V target (AJA International) maintained at 100 W of RF power was used to sputter a thin V film onto the desired substrates for 30 min. During deposition, the chamber was supplied with Ar at a partial pressure of 25 mTorr. Further, the substrates were held at ambient temperature during the deposition. The microheater chips were then submerged in N-methyl-2-pyrrolidone at 70°C to perform the lift-off.

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4.2 | Material Synthesis and Simulation

4.2.1 | Annealing

For the characterization chips, after deposition, the films were annealed on a hot plate at 450°C for 90 s under ambient air conditions. The films were then immediately transferred to a cold metal plate to quench oxidation and lock in the desired phase. For the microheater chips, the conversion of V to VO_2 was executed by applying a controlled voltage to the Ti/Pd pads, driving the doped Si heaters to temperatures between 450°C and 500°C for 90 s in air ambient. The annealing process includes 10 s ramping up and 10 s ramping down, which are realized by dynamically controlling the applied voltage.

4.2.2 | Numerical Modeling

Optical simulations were performed using the Tidy3D FDTD (Finite-Difference Time-Domain) [48] solver to estimate transmission loss due to VO_2 cladding at both phases. The refractive indices of two phases of VO_2 were referenced from refractiveindex.info [49]. Thermal profiles and power consumption were modeled using COMSOL Multiphysics, coupling electromagnetic heating with heat transfer in solids.

4.3 | Characterization

Full-range XRD measurements (10°–120°) of the films were performed on an Xpert Empyrean with a Cu source. Resistance vs. temperature measurements were performed on an Instec high-temperature probe station equipped with a Keithley 2450 SMU in a 2-probe configuration. For RBS measurements, a 2.3 MeV He^{2+} ion beam from a 1.7 MV IONEC tandem accelerator was utilized. For the analysis of observed statistics, the SIMNRA program was used. For XPS measurements, a ThermoFisher K-alpha XPS system with a monochromated Al Kα-source. The recorded core levels were fitted using the Thermo Avantage application. The crystal structure of VO_2 patches on the microheater was identified by Raman spectroscopy (Renishaw Invia Reflex Micro Raman with laser wavelength of 532 nm).

Author Contributions

K.P.D. and S.K. conceived and designed the experiments. K.P.D., Z.X., and R.C. fabricated the microheater and photonic devices. S.K. developed the VO2 thin-film synthesis process and deposited the VO2 films. K.P.D., J.Z., and Q.X. performed the in situ annealing experiments. K.P.D., J.Z., and Z.X. carried out the material characterization and photonic device measurements. K.P.D. and S.K. prepared the manuscript under the supervision of J.H. and S.R.

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Conflicts of Interest

The authors declare no conflicts of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding authors upon reasonable request.

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