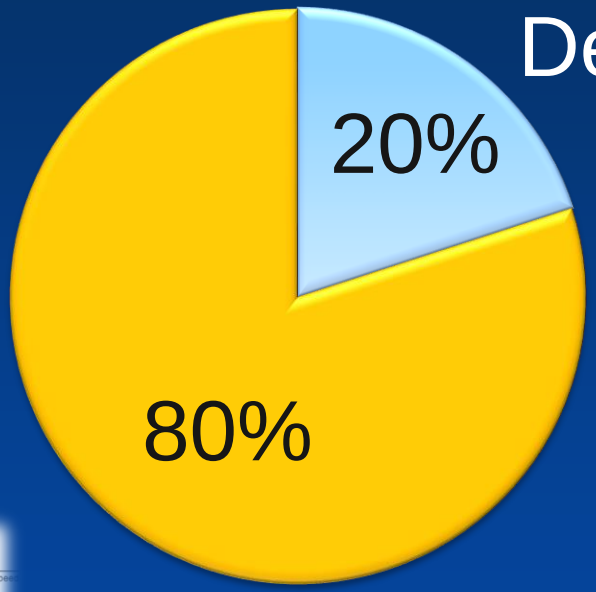
Quick & Thorough Verification of Processors and Hardware Accelerators

Saranyu Chattopadhyay, Caroline Trippel, Clark Barrett, Subhasish Mitra

Stanford University

Current Design Verification

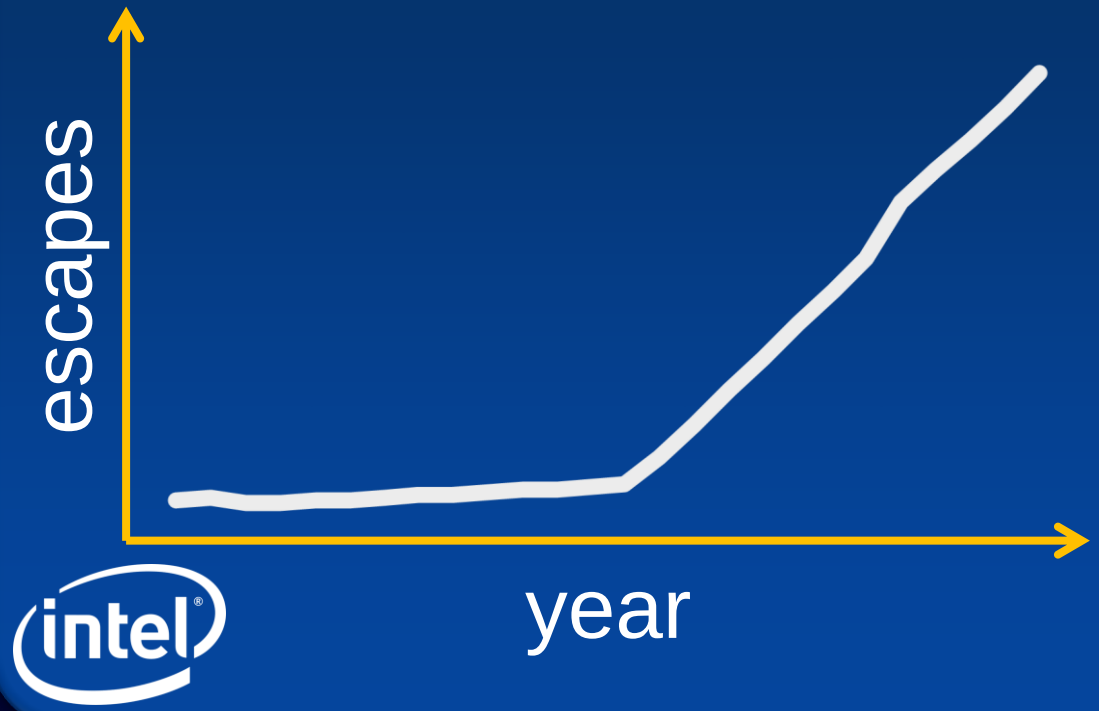
Major bottleneck



Wilson Research Group
Market research at market speed

Mentor®
A Siemens Business

Bug escapes increasing



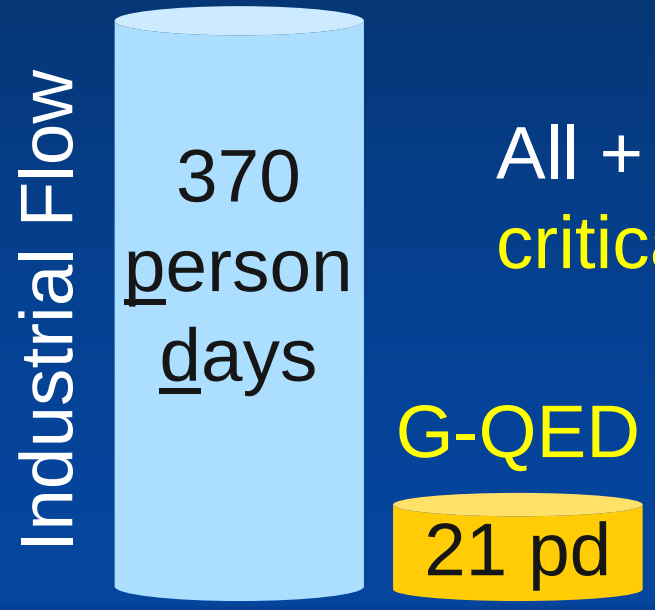
intel®

Need design internal know-hows

Generalized Quick Error Detection

18X Productivity

Production Ready Designs



Solid Theory

Hardware Accelerators + Processors

G-QED Properties

Functional Consistency	Response Bound	Single Action Correct
'Hard' Bugs		Rest
Total Correctness		

NO grubby internal know-hows

Future Scope

G-QED for large (Millions of gate) designs
(G-QED thorough for 0.5M gate designs)

G-QED for deep (Trillion cycle) bugs
(G-QED thorough up to ~100 cycles)

G-QED for side-channel security bugs
(G-QED thorough for pre-silicon logic bugs)