TO: MSPM Distribution
FROM: J. H. Saltzer
SUBJ: BC.1.04
DATE: 11/21/67

BC.1.04 contains the following changes:

1. The "rule of 32" is now assumed by the Interrupt
    Interceptor.

2. A drum interrupt assignment restriction is
    documented.

3. GIOC's now have only four status channels;
    the example is fixed accordingly.

Identification

Interrupt Cell Assignment
J. H. Saltzer, H. Frick

Purpose

When an active module (drum, GIOC, or CPU) needs to generate
an interrupt, it sets one of 32 numbered interrupt cells
in some system controller. The particular interrupt cell
set, in the case of the drum and GIOC, is determined by
a plug board in the active module. The system controller
in which the cell is set is determined by switch settings
(namely, the base address) in the active module. A CPU,
under program control, can set any interrupt cell in any
system controller. This section describes interrupt cell
assignment conventions used on Multics systems.

The "Rule of 32"

As mentioned above, the GIOC and drum determine which
interrupt cell number to set by a plug board located inside
the active module cabinet. The interrupt cell number
assigned, say for a GIOC Status Channel 3 interrupt, is
independent of which system controller will receive the
-set interrupt cell- request. (In the case of the GIOC,
the system controller is chosen on the basis of the GIOC
base address switches.) Thus, if at reconfiguration time
it is deemed necessary to direct GIOC interrupts to a
different system controller, by changing the GIOC base
address, the GIOC will set the same numbered interrupt
cells in the new system controller as it did in the old
one.

In a system which may generate more than 32 distinct interrupts
(e.g., a system with 3 drums, 4 GIOC's, 3 Clocks, and
1 CPU) it is necessary to assign some of the 32 interrupt
cell numbers twice, to different active devices. This
technique will work, as long as any two devices with overlapping
interrupt cell assignments are controlled by different
system controllers and, therefore, cause distinguishable
interrupts. On the other hand, a fixed, overlapped interrupt
cell assignment tends to restrict possible reconfigurations
of the system. This is because for two devices with fixed,
overlapping cell assignments to be controlled by a single
processor, two system controllers must be used and the
relative priority of individual interrupts from the two
devices is probably incorrect.

There are three ways of avoiding this problem:

1. Assume that there are always two system controllers
    for each CPU. This technique effectively provides
    64 interrupt numbers to be assigned among active
    modules. On the other hand, it limits severely the
    number of possible reconfigurations a given system
    can attain, and increases the amount of equipment
    which must be working to support a given load.

2. Provide two or more sets of interrupt cell assignment
    patch boards for some active modules, and plan to
    replace boards in order to achieve certain reconfigura-
    tions. This technique has the difficulty that board
    replacement is not intended to be a routine operation
    performed by system operators. The boards are typically
    accessible only by opening a cabinet door and
    swinging out a card rack.

3. Limit the total number of different kinds of
    interrupts to a number 32 or less. Then, a fixed
    interrupt cell assignment can be made which will
    remain valid under any reconfiguration. The easiest
    way to reduce the number of interrupts is to abandon
    some of the GIOC status channels, or else combine
    them, for example so that status channel 2 and 3 from
    a given GIOC set the same interrupt cell. As long
    as the configuration list presented to the system
    initializer or reconfigurer accurately describes the
    number of status channels to be used and the interrupt
    cells they set, Multics will operate correctly.

In the remainder of this document, we will assume that the third
alternative is taken, and a specific interrupt cell assignment
rule is given. Note that the Multics Interrupt Interceptor
Module also makes this assumption.

Interrupt Cell Assignment Rule

When the total number of interrupts which can be generated by
the system is 32 or less (either because the system is
small or because the technique suggested in 3, above,
is used) the following interrupt cell assignment order
is used:

GIOC1, Status Channel 0 ⎫
GIOC2, Status Channel 0 ⎬   all GIOC channel 0 interrupts,
    etc. ⎭   in order by GIOC#.

Clock 1, trouble ⎫
Clock 2, trouble ⎬   all Clock trouble interrupts,
    etc. ⎭   in order.

drum 1, Control ⎫
drum 1, Data   ⎪
drum 1, Programmed ⎬   all EMM interrupts, in order.
drum 2, Control ⎪
    etc. ⎭

GIOC 1, Status Channel 1 ⎫
GIOC 2, Status Channel 1 ⎪
    etc. ⎪   remaining GIOC channels, in
GIOC 1, Status Channel 2 ⎬ order first by channel#, then
GIOC 2, Status Channel 2 ⎪ the GIOC#.
    etc. ⎭

Clock 1, Wakeup ⎫
Clock 2, Wakeup ⎬   all Clock Wakeup interrupts.
    etc. ⎭

Processor initialize ⎫
Processor pre-empt   ⎬   All Traffic Controller generated
Processor time out   ⎪   interrupts.
Processor Quit ⎭

Trouble   A reserved cell, never masked,
                            which allows manual intervention.

There are two restrictions on the above general assignment pattern.

1.   The design of the GIOC Bootload adapter requires that status channel 1 of any GIOC containing a bootload *must* be assigned to interrupt cell 11 or less. The only practical way to handle this restriction in a large system is to assign the same interrupt cell for status channel 1 as is assigned for status channel 0 and abandon status channel 1.

2.   The drum controller design requires that all interrupt cells set by a single drum controller fall in the range 0-15 or else in the range 16-31.

Example

Table I shows the interrupt cell assigmnents devised according to the above rule for a system consisting of 2 CPU's, 2 GIOC's, 2 Clocks, and 1 drum. Note that the number of CPU's has no effect on the interrupt cell assignments.

```
0      GIOC 1 status channel 0
1      GIOC 2 status channel 0
2      Clock 1 trouble
3      Clock 2 trouble
4      drum control
5      drum data
6      drum programmed
7      GIOC 1 status channel 1
8       "    2    "         "    1
9       "    1    "         "    2
10      "    2    "         "    2
11      "    1    "         "    3
12      "    2    "         "    3
13     Clock 1 wakeup
14     Clock 2 wakeup
15     Processor initialize
16     Processor pre-empt
17     Processor time out
18     Processor quit
19     unassigned
20           "
21           "
22           "
23           "
24           "
25           "
26           "
27           "
28           "
29           "
30           "
31     trouble
```

Interrupt Cell
Assignment for

1 drum
2 GIOC's
2 Clocks
2 CPU's

Table 1