Identification

Slave mode control field loading
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Discussion

The 645 processor instructions LDB (load bases) and LBRn
(load base register n) will load not only the address
fields of unlocked base registers but also the control
field bits of the base registers. The control field bits
determine the pattern of linking of base register pairs.
Thus the instruction:

> EAPbp   A

specifies a potential loading of a <u>pair</u> of base registers,
even though only one base register, <u>bp</u>, is given. The
control field bits of the <u>bp</u> base register specify the
number of the corresponding register of the pair, in this
case register <u>bb</u>.

Since the Multics supervisor is written using standard
CALL, SAVE, and RETURN sequences, it therefore assumes
a standard linking among the base registers. To insure
that this standard linking is always in effect when in
the supervisor, a sequence of four LDCF (load control
field) instructions must be executed on every entry to
the supervisor. This sequence is done most easily by
the Fault Interceptor and Interrupt Interceptor modules,
since all entries to the supervisor are funneled through
them. This sequence adds approximately 15 microseconds
to the time required to process every fault and interrupt.

An appropriate hardware modification to eliminate the
need for constant reloading of the control field registers
is to make the LDB and LBRn instructions load only the
base register address fields, not the control fields,
when executed in slave mode. In Master Mode, the LDB
and LBRn instructions should reload the bases <u>and</u> the
control fields. Similarly, the LDCF instruction should
be restricted to operate in master mode only.