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Identification

Interrupt Cell Assignment Assumed by Multics
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Discussion

Multics, as currently initialized, assumes an interrupt cell assignment slightly different from that derived from the rules given in MSPM Section BC.1.04. The assignment Multics assumes is as follows:

Interrupt Cell	Interrupt Meaning	Swpt$int. hlr index	Handler called
0	GIOC A Status Channel 0	1	gioc_stat $int
1	GIOC B Status Channel 0	1	gioc_stat $int
2	Clock A Trouble	8	clock_handler $clock_handler
3	Clock B Trouble	8	clock_handler $clock_handler
4	Drum Trouble	5	drum_handler $drum_handler
5	Drum Data	6	drum_handler $drum_handler
6	Drum Program	7	drum_handler $drum_handler
7	GIOC A Status Channel 1	2	gioc_stat $int
8	GIOC B Status Channel 1	2	gioc_stat $int
9	GIOC A Status Channel 2	3	gioc_stat $int
10	GIOC B Status Channel 2	3	gioc_stat $int

Interrupt Cell	Interrupt Meaning	Swpt$int. hlr index	Handler called
11	GIOC A Status Channel 3	4	gioc_stat $int
12	GIOC B Status Channel 3	4	gioc_stat $int
13-20	Unassigned	-	panic$panic (See note 4)
21	Clock A Time Match	9	clock_handler $clock_handler
22	Clock B Time Match	9	clock_handler $clock_handler
23	Processor initialization	10	panic$panic (See note 5)
24	Pre-emption	11	proc_int $pre_empt
25	Time-out	12	proc_int $time_out
26	Quit	13	proc_int $quit
27-30	Unassigned	-	panic$panic
31	Trouble	14	panic$panic

Several special features should also be noted.

1. Both CPU's at the M.I.T. installation have been field modified to force all interrupts through the first 32 SCU-TRA pairs of the interrupt vector. Thus Multics cannot determine from the interception point fan-out which memory controller was the source of the interrupt. Since Multics does not care anyway (see discussion of the "rule of 32" in BC.1.04), this change is of no significance; in fact it has the effect of simplifying initialization.

2. The calendar clocks set interrupt cells different from those presumed by Multics. Their assignment is actually as follows:

Cell	Meaning
0	Trouble
16	Time Match

Note that both the Phase A (Prototype) and Phase B calendar clocks use the same interrupt cell assignment. The cell 0 conflict with the GIOC is of little consequence for the moment since clock trouble interrupts should be rare.

3. For unknown reasons, interrupt cells 3, 4, 5, 6, and 7 are considered by Multics to be of the same priority, and the same interrupt mask is used in response to any one of of those interrupts. The result is that any two of these interrupts will be handled serially in the order of occurrence. For the particular interrupts in question, this constraint happens to be of no consequence.

4. The module which initializes system metering sets up a special intercept for interrupt cell 16, forcing clock time match interrupts directly to itself and bypassing the Interrupt Interceptor.

5. The intercept for interrupt cell 23 is modified with a special processor initialization sequence whenever a new processor is brought into the system. After initialization of the processor, the standard intercept (panic$panic) is restored, for safety.