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Identification

Hard-Core Supervisor entry points
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Purpose

The innermost protection ring of the Multics supervisor is known as the hard-core supervisor ring. As a general rule, procedures and data bases are located in the hard-core ring if their correctness is needed in order to guarantee inter-user protection and privacy. For example, the procedures and data bases of the Basic File System, the GIOC interface module, and the Traffic Controller are located in the hard-core ring. This section lists all permitted entry points to the hard-core ring.

Discussion

The hard-core ring of the supervisor is entered by the standard ring-crossing mechanism described in BD.9.01. From outside the hard-core ring, it appears that all entry points are located in one of two segments named "hcs_" and "hcs1_". These segments are merely transfer vectors which pass the call to the appropriate segment entry point in the hard-core ring. This extra indirection is inserted on the assumption that the position of entry points of segment hcs_ and hcs1_ will change only rarely--when an old hard-core entry point is deleted, for example--and that therefore the caller can rely on his linkage to the entry point remaining correct even though the hard-core supervisor changes. If the caller were linked directly to an entry point of some hard-core supervisor procedure, his link becomes useless if a trivial change to the hard-core supervisor procedure should move its entry point. (In general, it is not practical for one user to run with an "old" version of a hard-core supervisor segment. Security is difficult to check and the segment may have to be "wired-down" to operate. It might also contain a serious bug.)

Whenever the system is initialized or reconfigured, the segments hcs_ and hcs1_, being part of the hard-core ring, are correctly linked to the real hard-core entry points by the same pre-linking mechanism which links all hard-core modules together. Pre-linking of the hard-core ring is described in section BL.7.02.

Segment hcs_ contains entries to all unrestricted hard-core entry points. Segment hcs1_ contains all entries which may be called only from the administrative ring.

Entry points

Below is an exhaustive list of all legal entry points to the hard-core ring. For further information on any entry point including arguments, see the MSPM sections indicated.

| entry | MSPM section |
|-----------------------------|--------------|
| Traffic Controller | |
| <hcs1_> [wakeup] | BJ.3.00 |
| <hcs1_> [block] | BJ.3.00 |
| <hcs1_> [create_process] | BJ.1.00 |
| <hcs1_> [destroy_process] | BJ.1.00 |
| Basic File System | |
| <hcs1_> [makeunknown] | BG.3.01 |
| <hcs1_> [transuse] | " |
| <hcs1_> [get_ring] | " |
| <hcs1_> [moveseg] | " |
| <hcs_> [free_core] | BG.3.02 |
| <hcs_> [read_seg] | " |
| <hcs_> [write_seg] | " |
| <hcs_> [truncate_seg] | " |
| <hcs_> [core_test] | " |
| <hcs_> [check_access] | " |
| <hcs_> [check_ring] | " |
| <hcs_> [list_dir] | BG.8.02 |
| <hcs_> [status] | " |

| | |
|--------------------------|----------|
| <hcs_> [chname] | BG.8.02 |
| <hcs_> [delentry] | " |
| <hcs_> [readac1] | " |
| <hcs_> [writeac1] | " |
| <hcs_> [setbc] | " |
| <hcs_> [setconsistsw] | " |
| <hcs_> [setm1] | " |
| <hcs_> [setcopysw] | " |
| <hcs_> [setrelatesw] | " |
| <hcs_> [setrd] | " |
| <hcs_> [appendb] | " |
| <hcs_> [append1] | " |
| <hcs_> [movefile] | " |
| <hcs1_> [estblseg] | BG.8.04 |
| <hcs1_> [setlimits] | BG.8.03 |
| <hcs1_> [setsystrap] | " |
| <hcs1_> [setretrieve] | " |
| <hcs1_> [setdtd] | " |
| <hcs1_> [getentry] | " |
| <hcs1_> [putentry] | " |
| <hcs1_> [setusage] | BG.8.04 |
| <hcs1_> [set_base_dir] | " |
| GIOC Interface Module | |
| <hcs_> [define_class] | BF.20.02 |
| <hcs_> [define_list] | " |

| | |
|-------------------------------|----------|
| <hcs_> [change_list] | BF.20.02 |
| <hcs_> [change_global] | " |
| <hcs_> [copy_list] | BF.20.02 |
| <hcs_> [connect_list] | " |
| <hcs_> [request_status] | " |
| <hcs_> [release_list] | " |
| <hcs1_> [assign_channel] | " |
| <hcs1_> [define_assign] | " |
| <hcs1_> [define_channel] | " |
| Media Management Module | |
| <hcs_> [load] | BT.2 |
| <hcs_> [unload] | BT.2 |
| <hcs_> [locate] | BT.2 |
| <hcs_> [return] | BT.2 |
| Resource Assignment Module | |
| <hcs1_> [assign] | BT.1 |
| <hcs1_> [unassign] | BT.1 |
| Interprocess Communication | |
| <hcs1_> [get_device_signal] | BQ.6 |
| Miscellaneous entry points | |
| <hcs_> [set_timer] | BD.10.04 |
| <hcs1_> [set_alarm] | BD.10.03 |