M.I.T. Laboratory for Computer Science

Network Implementation Note
No. 27
April 30, 1980

Version 2 Local network status report and development plan update

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1. Transmission system

Status: Ken Pogran and Joe Ricchio have set up a copy of the V2.LNI transmitter/receiver system at L.C.S. for the purpose of checking out the transmission system design in an operational environment. The current design provides strong, noise-free signals at 8 mb/sec. over a test cable run of 240 meters when using Belden 9182 150 ohm twinax. It appears that the 300 meter specification can be met easily with this cable. A simple shielded twisted pair (Belden 8761) of length about 100 meters operates almost as well, producing a slight loss of symmetry in the received data which is thought to be of little consequence to the performance of the data communication system. However, the attenuation of this cheaper cable seems to prevent its use on a 300 meter test run.

Plans: 1) Test to determine the longest usable run of the cheaper cable. 2) Test of cable installed in actual building runs at 545 Technology Square by using V1.ring cable installation with repeaters bypassed, to learn more about noise performance. 3) Test to insure that adding D.C. bias currents to the twisted pair (for relay control) does not impair signal transmission. 4) Integration of minor circuit changes suggested by these tests with documentation and wire lists. 5) Integration with modem to learn if residual timing jitter on long cable runs is below the level that affects the modems.

2. Modem

Status: A basic frequency-locked, closed-loop modem was demonstrated with two copies in a ring in November, 1979, but that basic design operates only over a narrow range of cable lengths. The phase-offset stage that permits the modem to work with any cable length has been added and is in final check out by Greg Koss. Four copies of the phase-offset modem have been constructed for testing. An alternative all-digital, phase-locked, open-loop modem design that uses a fixed oscillator frequency was developed on paper by D. Reed.

Plans: 1) The frequency-locked modem will be used in the prototype ring, at least until time is available to try out the phase-locked design. 2) A four-node ring of modems will be brought up in the Proteon laboratory to check out stability and noise performance.

3. Ring control module

Status: A pair of 40-chip control modules using the frequency-locked modem was demonstrated to circulate tokens in November, 1979, by Greg Koss using a fixed delay register to provide space for the tokens. Circuit changes developed during the debugging of those two prototypes have been integrated into the documentation and wire lists, and four new clean copies of the control module have been constructed from that documentation.

Plans: 1) The four new control modules are being checked out in preparation for integration. 2) The four modules will be connected in a 4-node ring. 3) An automatically inserted delay register for short rings and loop-around testing may be added. 4) Relay control circuitry must be added. 5) The two original modules will be stripped down and

reworked, together with two more, to provide a total of eight ring control modules.

4. Ring control module--buffer module interface specification

Status: The interface between these two cards has been more carefully specified so as to allow several versions of the buffer module to be developed, specific to different host computers.

5. Buffer module for UNIBUS machines

Status: A 110-chip module containing a full-duplex DMA interface for the UNIBUS, control and status registers suitable for the ring network, and input and output packet buffers has been constructed by Henry Arbour. Checkout has proceeded across the board starting with the DMA, and is now nearly complete. A number of non-critical loose ends have been noted for later study rather than being fixed on the spot, so as to expedite the start of integration of the buffer module with the ring control module. A second copy of the buffer module has been constructed and it is being modified to keep it identical to the one being checked out.

Plans: 1) Finish checkout of packet buffer circuitry. 2) Integration with control module. 3) Cleanup of loose ends uncovered in earlier checkout:

- generate UNIBUS interrupt cycles
- use correct UNIBUS address
- define interrupt vector
- fix bus grant passing
- allow retransmit of packet buffer contents without reloading them.

4) Place second LNI on same UNIBUS to circulate messages. 5) Place second LNI on a different UNIBUS. 6) Publish Chiappa's programming

specification for the UNIBUS. 7) Construction of three more, using wire wrap facility at L.C.S.

6. Buffer module for nu-bus

Status: no recent progress. A draft programming specification was written by D. Clark in November, 1979.

Plans: When checkout of disk DMA for nu-bus is complete, adapt that design to the requirements of the V2.ring by using the same status register design as in the UNIBUS buffer module and by changing the disk DMA from half-duplex to full-duplex and installing FIFO buffers.

7. Buffer module for S-100 bus

Status: Undergraduate student project. A programming specification is being prepared.

Plans: Still being discussed.

8. Buffer module for Q-bus

Status: Under discussion as a desirable extension. Programming interface is same as for UNIBUS.

9. Maintenance control center

Status: Manual control center for V1.ring is operational. Design of automatic control center deferred till manpower available.

Plans: Use copy of manual control center at first.